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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 15x12b SAR
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8006vwl

  - 1/16 bit-time noise detection
- One serial peripheral interface (SPI)
  - Full-duplex operation
  - Master and slave modes
  - Programmable length transactions (2 to 16 bits)
  - Programmable transmit and receive shift order (MSB as first or last bit transmitted)
  - Maximum slave module frequency = module clock frequency/2
- One inter-integrated Circuit (I^2C) port
  - Operates up to 400 kbps
  - Supports master and slave operation
  - Supports 10-bit address mode and broadcasting mode
  - Supports SMBus, Version 2
- One 16-bit programmable interval timer (PIT)
  - 16 bit counter with programmable counter modulo
  - Interrupt capability
- One 16-bit programmable delay block (PDB)
  - 16 bit counter with programmable counter modulo and delay time
  - Counter is initiated by positive transition of internal or external trigger pulse
  - Supports two independently controlled delay pulses used to synchronize PGA and ADC conversions with input trigger event
  - Two PDB outputs can be ORed together to schedule two conversions from one input trigger event
  - PDB outputs can be can be used to schedule precise edge placement for a pulsed output that generates the control signal for the CMP windowing comparison
  - Supports continuous or single shot mode
  - Bypass mode supported
- Computer operating properly (COP)/watchdog timer capable of selecting different clock sources
  - Programmable prescaler and timeout period
  - Programmable wait, stop, and partial powerdown mode operation
  - Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
  - Choice of clock sources from four sources in support of EN60730 and IEC61508:
    - On-chip relaxation oscillator
    - External crystal oscillator/external clock source
    - System clock (IPBus up to 32 MHz)
    - On-chip low power 1 kHz oscillator
- Real-timer counter (RTC)
  - 8-bit up-counter
  - Three software selectable clock sources
    - External crystal oscillator/external clock source
    - On-chip low-power 1 kHz oscillator
    - System bus (IPBus up to 32 MHz)
  - Can signal the device to exit power down mode
- Phase lock loop (PLL) provides a high-speed clock to the core and peripherals
  - Provides 3x system clock to PWM and dual timer and SCI
  - Loss of lock interrupt
  - Loss of reference clock interrupt

3.3 Architecture Block Diagram

The 56F8006/56F8002's architecture is shown in Figure 2 and Figure 3. Figure 2 illustrates how the 56800E system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800E core. Figure 3 shows the peripherals and control blocks connected to the IPBus bridge. Please see the system integration module (SIM) section in the *MC56F8006 Reference Manual* for information about which signals are multiplexed with those of other peripherals.

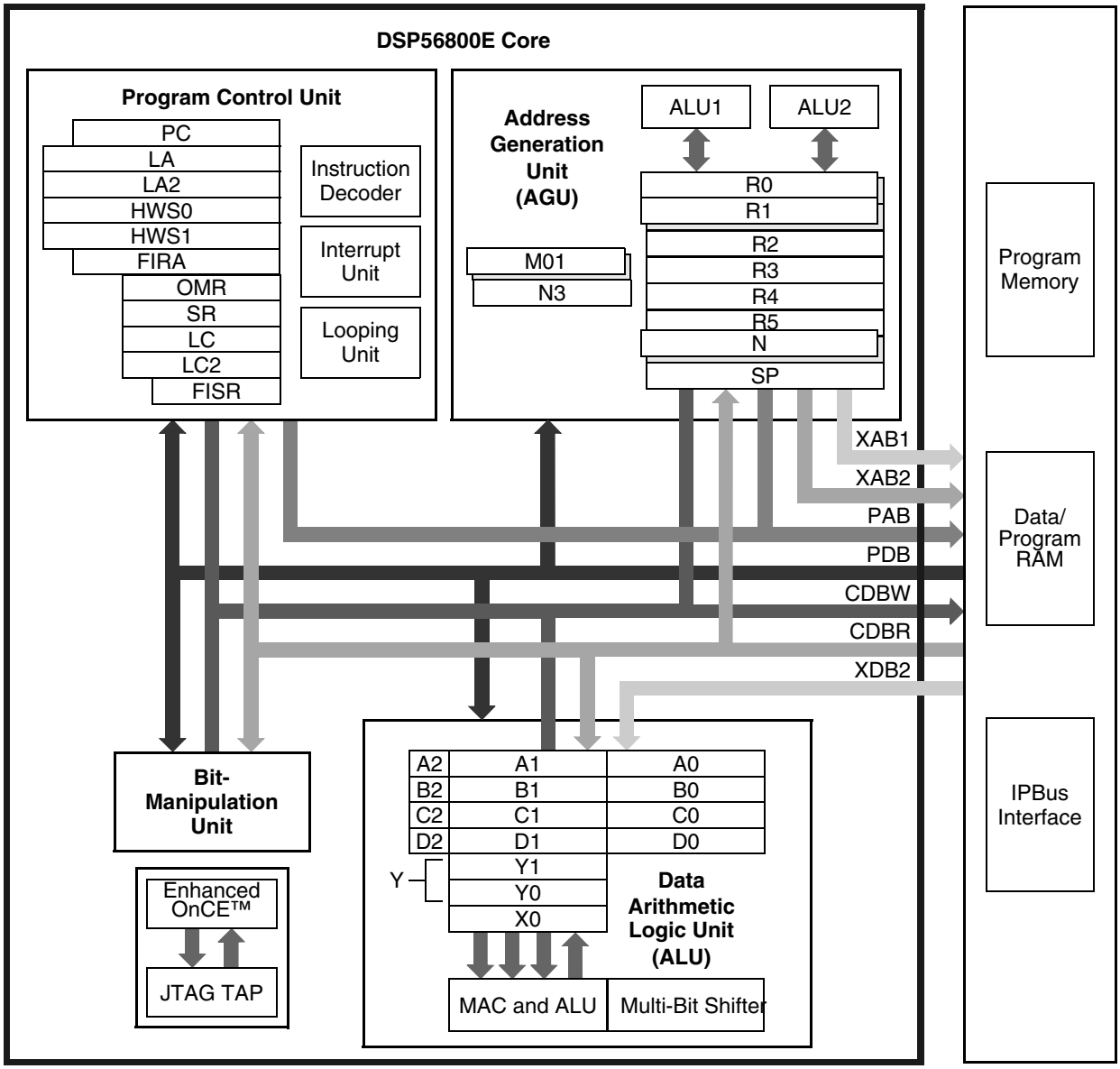


Figure 2. 56800E Core Block Diagram

3.4 Product Documentation

The documents listed in Table 2 are required for a complete description and proper design with the 56F8006/56F8002. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at http://www.freescale.com.

Table 2. 56F8006/56F8002 Device Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit digital signal controller core processor, and the instruction set	DSP56800ERM
56F800x Peripheral Reference Manual	Detailed description of peripherals of the 56F8006 and 56F8002 devices	MC56F8006RM
56F80x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F800x family of devices	TBD
56F8006/56F8002 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8006
56F8006/56F8002 Errata	Details any chip issues that might be present	MC56F8006E

4 Signal/Connection Descriptions

4.1 Introduction

The input and output signals of the 56F8006/56F8002 are organized into functional groups, as detailed in Table 3. Table 4 summarizes all device pins. In Table 4, each table row describes the signal or signals present on a pin, sorted by pin number.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins in 28 SOIC	Number of Pins in 32 LQFP	Number of Pins in 32 PSDIP	Number of Pins in 48 LQFP
Power Inputs (V_{DD}, V_{DDA})	2	2	2	4
Ground (V_{SS}, V_{SSA})	3	3	3	4
Reset[1]	1	1	1	1
Pulse Width Modulator (PWM) Ports[1]	10	12	12	12
Serial Peripheral Interface (SPI) Ports[1]	5	7	7	7
Serial Communications Interface 0 (SCI) Ports[1]	4	5	5	5
Inter-Integrated Circuit Interface (I^2C) Ports[1]	6	7	7	7
Analog-to-Digital Converter (ADC) Inputs[1]	16	18	18	24
High Speed Analog Comparator Inputs[1]	13	15	15	25
Programmable Gain Amplifiers (PGA)[1]	4	4	4	4
Dual Timer Module (TMR) Ports[1]	8	10	10	10
Programmable Delay Block (PDB)[1]	—	—	—	1
Clock[1]	5	5	5	5
JTAG/Enhanced On-Chip Emulation (EOnCE[1])	4	4	4	4

[1] Pins may be shared with other peripherals. See Table 4.

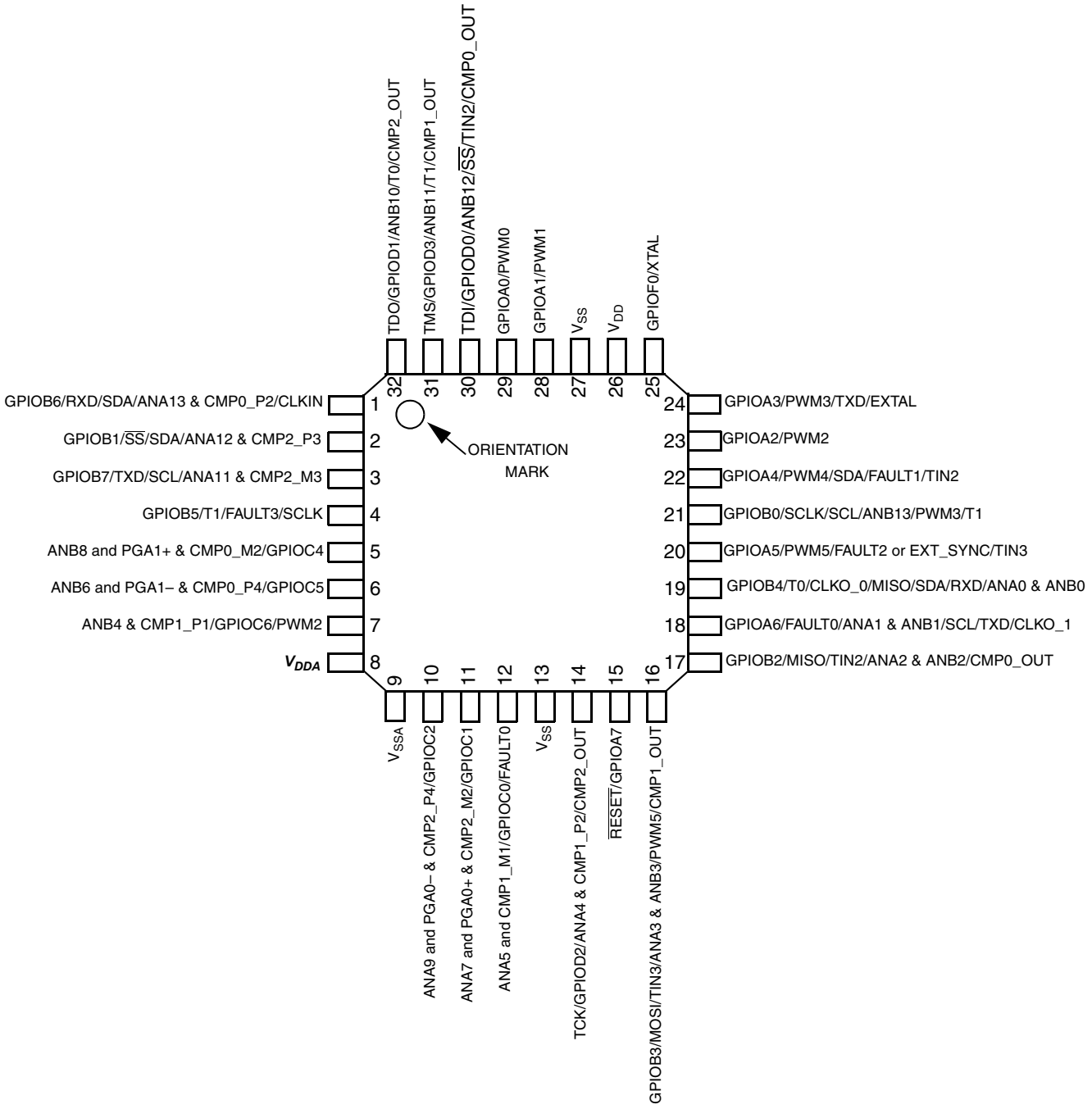


Figure 5. Top View, MC56F8006 32-Pin LQFP Package

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOB3	11	16	12	24	Input/ Output	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.
(MOSI)					Input/ Output		MOSI — Master out/slave in. In master mode, this pin serves as the data output. In slave mode, this pin serves as the data input.
(TIN3)					Input/ Output		TIN3 — Dual timer module channel 3 input.
(ANA3 and ANB3)					Input		ANA3 and ANB3 — Analog input to channel 3 of ADCA and ADCB.
(PWM5)					Output		PWM5 — The PWM channel 5.
(CMP1_ OUT					Output		CMP1_OUT— Analog comparator 1 output. When used as an analog input, the signal goes to the ANA3 and ANB3. After reset, the default state is GPIOB3.
GPIOB4	13	19	15	27	Input/ Output	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin.
(T0)					Input/ Output		T0 — Dual timer module channel 0 input/output.
(CLKO_0)					Output		CLKO_0 — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(MISO)					Input/ Output		MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
(SDA)					Input/Open-drain Output		SDA — The I^2C serial data line.
(RXD)					Input		RXD — The SCI receive data input.
(ANA0 and ANB0)					Analog Input		ANA0 and ANB0 — Analog input to channel 0 of ADCA and ADCB. When used as an analog input, the signal goes to the ANA0 and ANB0. After reset, the default state is GPIOB4.

Table 8. Program Memory Map[1] for 56F8002 at Reset (continued)

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 83FF P: 0x00 8000	On-Chip RAM[2]: 2 KB
P: 0x00 7FFF P: 0x00 2000	RESERVED
P: 0x00 1FFF P: 0x00 0800	• Internal program flash: 12 KB • Interrupt vector table locates from 0x00 0800 to 0x00 0865 • COP reset address = 0x00 0802 • Boot location = 0x00 0800
P: 0x00 07FF P: 0x00 0000	RESERVED

1 All addresses are 16-bit word addresses.

2 This RAM is shared with data space starting at address X: 0x00 0000; see Figure 9.

5.3 Data Map

The 56F8006/56F8002 series contain a dual access memory. It can be accessed from core primary data buses (XAB1; CDBW; CDBR) and secondary data buses (XAB2; XDB2). Addresses in data memory are selected on the XAB1 and XAB2 buses. Byte, word, and long data transfers occur on the 32-bit CDBR and CDBW buses. A second 16-bit read operation can be performed in parallel on the XDB2 bus.

Peripheral registers and on-chip JTAG/EOnCE controller registers are memory-mapped into data memory access. A special direct address mode is supported for accessing a first 64-location in data memory by using a single word instruction.

The data memory map is shown in Table 9.

Table 9. Data Memory Map[1]

Begin/End Address	Memory Allocation
X:0xFF FFFF X:0xFF FF00	EOnCE 256 locations allocated
X:0xFF FEFF X:0x01 0000	RESERVED
X:0x00 FFFF X:0x00 F000	On-Chip Peripherals 4096 locations allocated
X:0x00 EFFF X:0x00 8800	RESERVED
X:0x00 87FF X:0x00 8000	RESERVED
X:0x00 7FFF X:0x00 0400	RESERVED
X:0x00 03FF X:0x00 0000	On-Chip Data RAM 2 KB[2]

1 All addresses are 16-bit word addresses.

2 This RAM is shared with Program space starting at P: 0x00 8000. See Figure 8 and Figure 9.

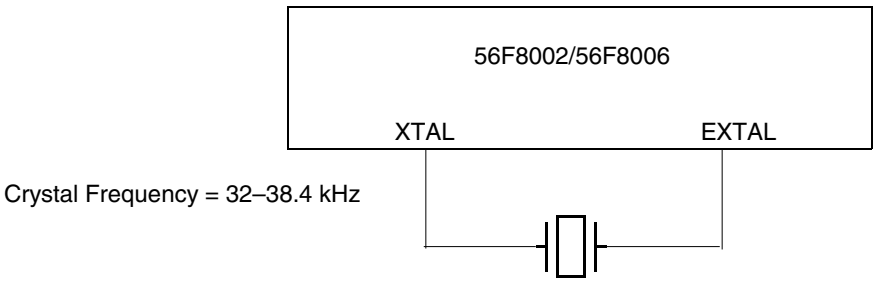


Figure 10. Typical Crystal Oscillator Circuit: Low-Range, Low-Power Mode

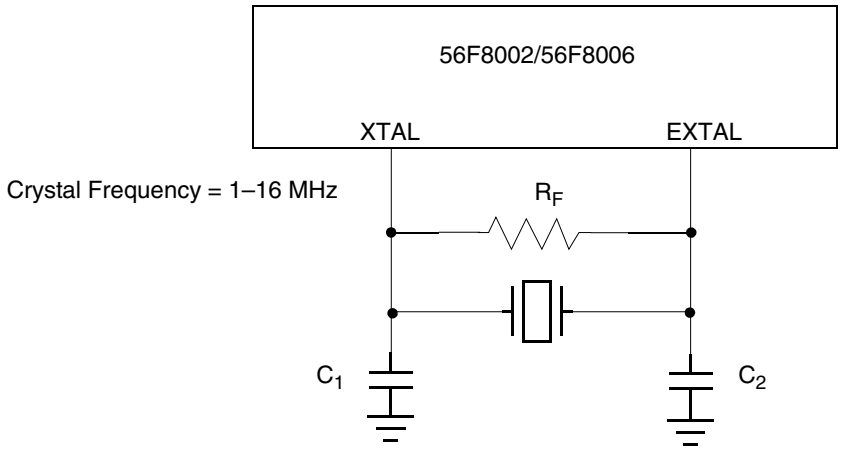


Figure 11. Typical Crystal or Ceramic Resonator Circuit: High-Range, Low-Power Mode

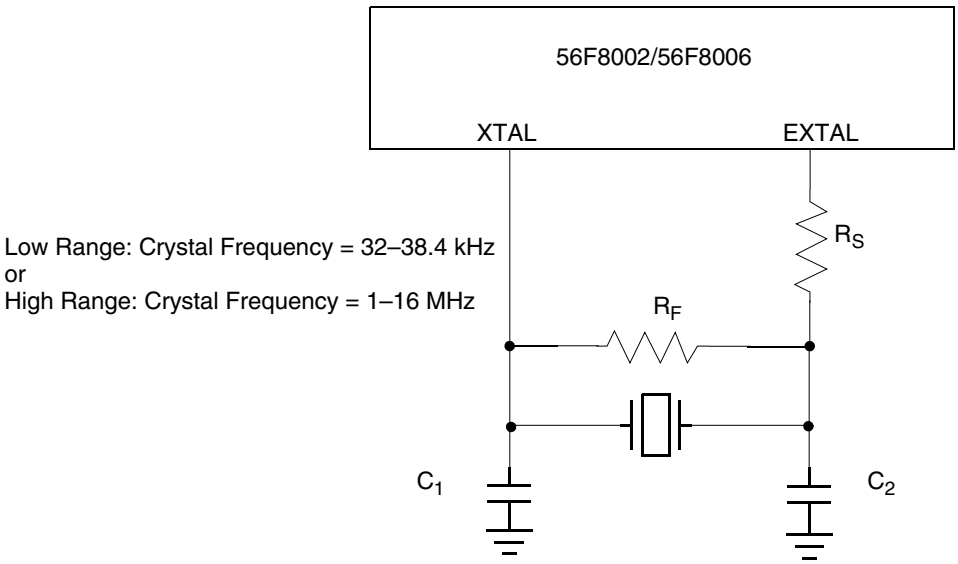


Figure 12. Typical Crystal or Ceramic Resonator Circuit: Low Range and High Range, High-Gain Mode

6.4.3 External Clock Input — Crystal Oscillator Option

The recommended method of connecting an external clock is illustrated in Figure 13. The external clock source is connected to XTAL and the EXTAL pin is grounded or configured as GPIO while CLK_MOD bit in OSCTL register is set. The external clock input must be generated using a relatively low impedance driver with maximum frequency less than 8 MHz.

Each ADC contains a temperature sensor. Outputs of temperature sensors, PGAs, on-chip regulators and VDDA are internally routed to ADC inputs.

- Internal PGA0 output available on ANA15
- Internal PGA0 positive input calibration voltage available on ANA16
- Internal PGA0 negative input calibration voltage available on ANA17
- Internal PGA1 output available on ANB15
- Internal PGA1 positive input calibration voltage available on ANB16
- Internal PGA1 negative input calibration voltage available on ANB17
- ADCA temperature sensor available on ANA26
- ADCB temperature sensor available on ANB26
- Output of on-chip digital voltage regulator is routed to ANA24
- Output of on-chip analog voltage regulator is routed to ANA25
- Output of on-chip small voltage regulator for ROSC is routed to ANB24
- Output of on-chip small voltage regulator for PLL is routed to ANB25
- VDDA is routed to ANA27 and ANB27

6.8 Joint Test Action Group (JTAG)/Enhanced On-Chip Emulator (EOnCE)

The DSP56800E Family includes extensive integrated support for application software development and real-time debugging. Two modules, the Enhanced On-Chip Emulation module (EOnCE) and the core test access port (TAP, commonly called the JTAG port), work together to provide these capabilities. Both are accessed through a common 4-pin JTAG/EOnCE interface. These modules allow you to insert the 56F8006/56F8002 into a target system while retaining debug control. This capability is especially important for devices without an external bus, because it eliminates the need for a costly cable to bring out the footprint of the chip, as is required by a traditional emulator system.

The DSP56800E EOnCE module is a Freescale-designed module used to develop and debug application software used with the chip. This module allows non-intrusive interaction with the CPU and is accessible through the pins of the JTAG interface or by software program control of the DSP56800E core. Among the many features of the EOnCE module is the support for data communication between the controller and the host software development and debug systems in real-time program execution. Other features allow for hardware breakpoints, the monitoring and tracking of program execution, and the ability to examine and modify the contents of registers, memory, and on-chip peripherals, all in a special debug environment. No user-accessible resources need to be sacrificed to perform debugging operations.

The DSP56800E JTAG port is used to provide an interface for the EOnCE module to the DSP JTAG pins. Joint Test Action Group (JTAG) boundary scan is an IEEE 1149.1 standard methodology enabling access to test features using a test access port (TAP). A JTAG boundary scan consists of a TAP controller and boundary scan registers. Please contact your Freescale sales representative or authorized distributor for device-specific BSDL information.

NOTE

In normal operation, an external pullup on the TMS pin is highly recommend to place the JTAG state machine in reset state if this pin is not configured as GPIO.

7 Security Features

The 56F8006/56F8002 offers security features intended to prevent unauthorized users from reading the contents of the flash memory (FM) array. The 56F8006/56F8002's flash security consists of several hardware interlocks that prevent unauthorized users from gaining access to the flash array.

After flash security is set, an authorized user can be enabled to access on-chip memory if a user-defined software subroutine, which reads and transfers the contents of internal memory via peripherals, is included in the application software. This

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 13. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulses per Pin	—	3	
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulses per Pin	—	3	
Latch-up	Minimum inpUt Voltage Limit		–2.5	V
	Maximum Input Voltage Limit		7.5	V

Table 14. 56F8006/56F8002 ESD Protection

Characteristic [1]	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	750	—	—	V
Latch-up current at T_A= 85°C (I_{LAT})	± 100			mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

8.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 15. 28SOIC Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	70	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	47	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	55	°C/W

Table 18. 48LQFP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	79	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	55	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	66	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	48	°C/W
Junction to board		$R_{\theta JB}$	34	°C/W
Junction to case		$R_{\theta JC}$	20	°C/W
Junction to package top	Natural Convection	Ψ_{JT}	4	°C/W

NOTE

Junction-to-ambient thermal resistance determined per JEDEC JESD51–3 and JESD51–6. Thermal test board meets JEDEC specification for this package.

Junction-to-board thermal resistance determined per JEDEC JESD51–8. Thermal test board meets JEDEC specification for the specified package.

Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51–2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

See Section 9.1, “Thermal Design Considerations,” for more detail on thermal design considerations.

8.4 Recommended Operating Conditions

This section includes information about recommended operating conditions.

8.9 Phase Locked Loop Timing

Table 25. Phase Locked Loop Timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	4	8	—	MHz
PLL output frequency[2]	f_{op}	120	192	—	MHz
PLL lock time[3] [4]	t_{plls}	—	40	100	µs
Accumulated jitter using an 8 MHz external crystal as the PLL source[5]	J_A	—	—	0.37	%
Cycle-to-cycle jitter	$t_{jitterpll}$	—	350	—	ps

1 An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.

2 The core system clock operates at 1/6 of the PLL output frequency.

3 This is the time required after the PLL is enabled to ensure reliable operation.

4 From powerdown to powerup state at 32 MHz system clock state.

5 This is measured on the CLKO signal (programmed as system clock) over 264 system clocks at 32 MHz system clock frequency and using an 8 MHz oscillator frequency.

8.10 Relaxation Oscillator Timing

Table 26. Relaxation Oscillator Timing

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
Relaxation oscillator output frequency[1] Normal Mode Standby Mode	f_{op}	—	 8.05 400	—	 MHz kHz
Relaxation oscillator stabilization time[2]	t_{roscs}	—	1	3	ms
Cycle-to-cycle jitter. This is measured on the CLKO signal (programmed prescaler_clock) over 264 clocks[3]	$t_{jitterrosc}$	—	400	—	ps
Variation over temperature –40 °C to 105 °C[4]		—	—	–3.0 to +2.0	%
Variation over temperature 0 °C to 105 °C[5]		—	—	–2.0 to +2.0	%
Variation over temperature –40 °C to 125 °C[4]		—	—	–3.5 to +3.0	%

1 Output frequency after factory trim.

2 This is the time required from standby to normal mode transition.

3 J_A is required to meet QSCI requirements.

4 See Figure 22. The power supply VDD must be greater than or equal to 2.6 V. Below 2.6 V, the maximum variation over the whole temperature and whole voltage range from 1.8 V to 2.6 V will be +/-16%.

5 This data is only applied to devices with temperature range from –40 °C to 105 °C.

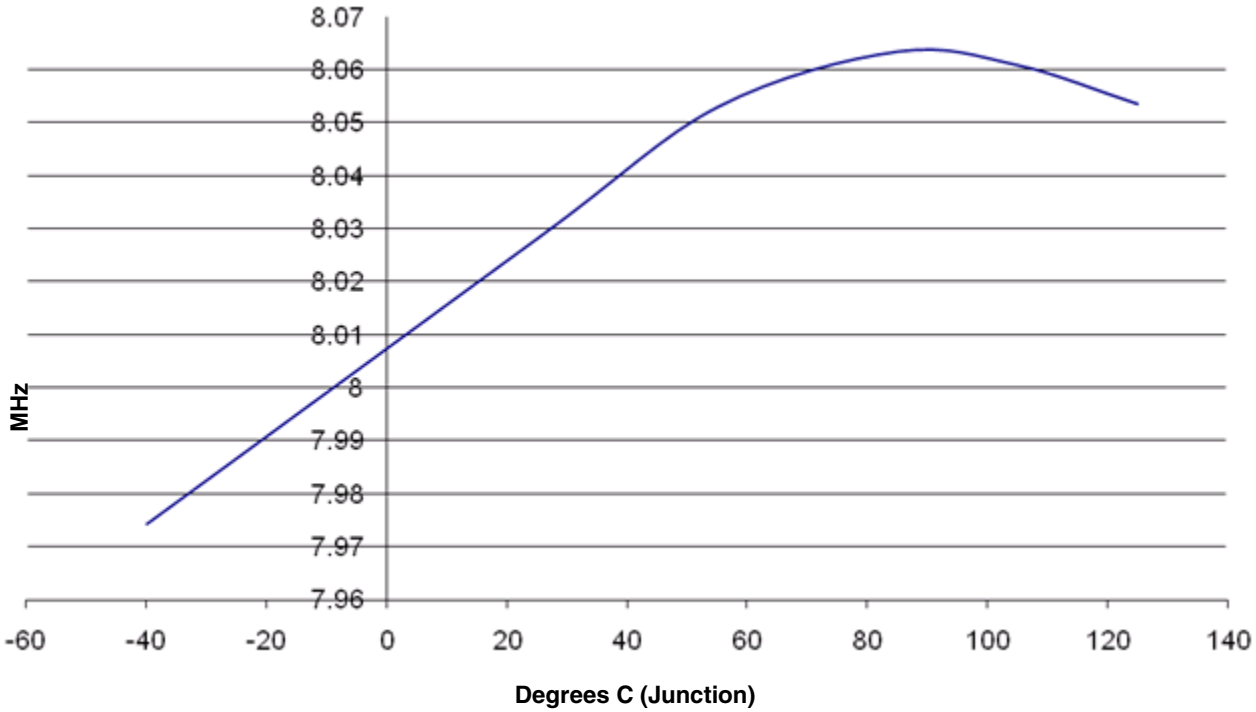


Figure 22. Relaxation Oscillator Temperature Variation (Typical) After Trim for devices with temperature operating range from –40 °C to 105 °C

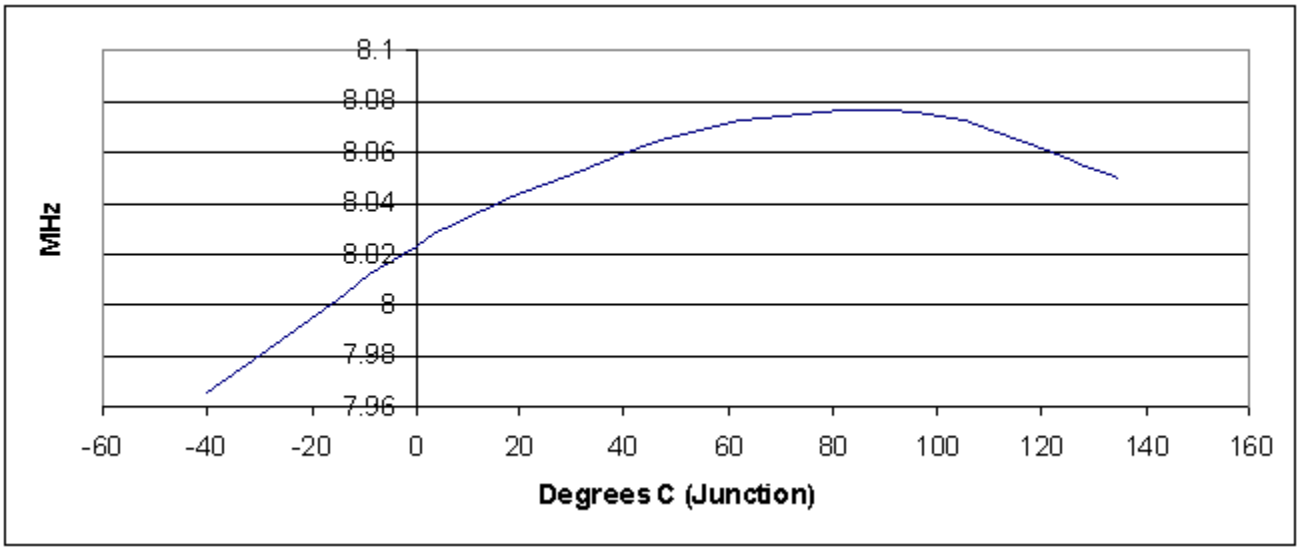


Figure 23. Relaxation Oscillator Temperature Variation (Typical) After Trim for devices with temperature operating range from –40 °C to 125 °C

8.11 Reset, Stop, Wait, Mode Select, and Interrupt Timing

NOTE

All address and data buses described here are internal.

Table 27. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	4T	—	ns	—
Minimum GPIO pin Assertion for Interrupt	t_{IW}	2T	—	ns	Figure 24
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	$96T_{OSC}$ + 64T	$97T_{OSC}$ + 65T	ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	—	6T	ns	—

1 In the formulas, T = system clock cycle and T_{osc} = oscillator clock cycle. For an operating frequency of 32 MHz, T = 31.25 ns. At 4 MHz (used coming out of reset and stop modes), T = 250 ns.

2 Parameters listed are guaranteed by design.

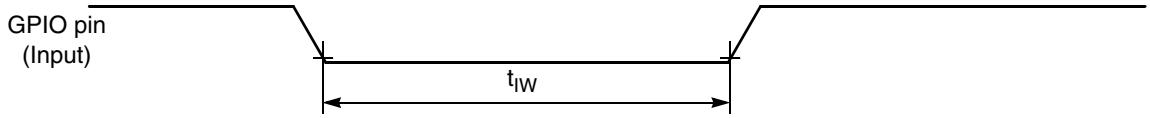


Figure 24. GPIO Interrupt Timing (Negative Edge-Sensitive)

8.12 External Oscillator (XOSC) Characteristics

Reference Figure 10, and Figure 11, and Figure 12 for crystal or resonator circuits.

Figure 31. RXD Pulse Width

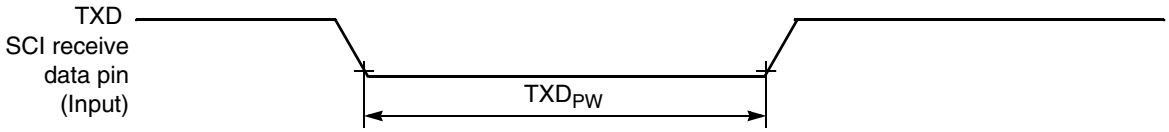


Figure 32. TXD Pulse Width

8.13.3 Inter-Integrated Circuit Interface (I^2C) Timing

Table 31. I^2C Timing

Characteristic	Symbol	Standard Mode		Unit
		Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7	—	µs
Data hold time for I^2C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	ns
Fall time of SDA and SCL signals	t_f	—	300	ns
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	ns

1 The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

2 The maximum $t_{HD;\ DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

8.16 ADC Specifications

Table 36. ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
Input voltage		V_{ADIN}	V_{REFL}[2]	—	V_{REFH}[3]	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	5	7	kΩ	
Analog source resistance	12-bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10-bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz		 — —	 — —	 5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock freq.	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 $V_{REFL} = V_{SSA}$

3 $V_{REFH} = V_{DDA}$

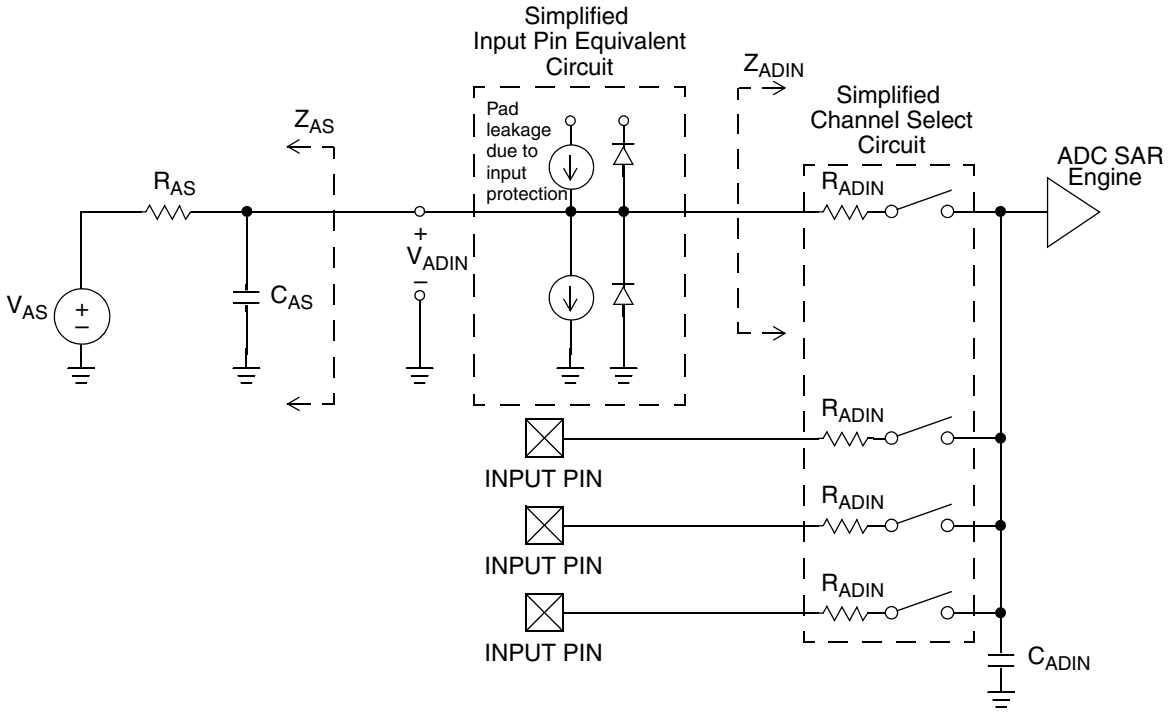
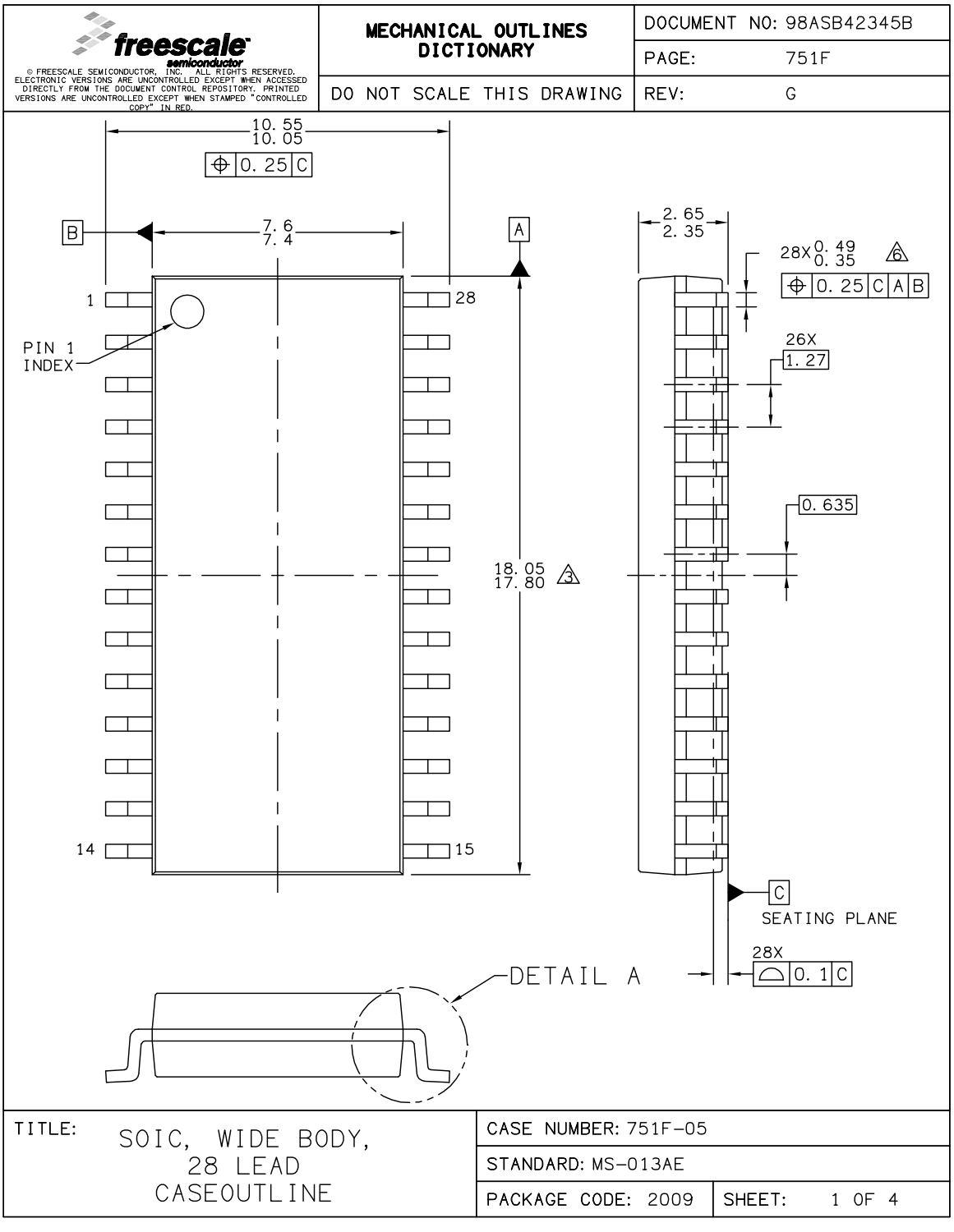


Figure 37. ADC Input Impedance Equivalency Diagram

10 Package Mechanical Outline Drawings

10.1 28-pin SOIC Package



10.2 32-pin LQFP

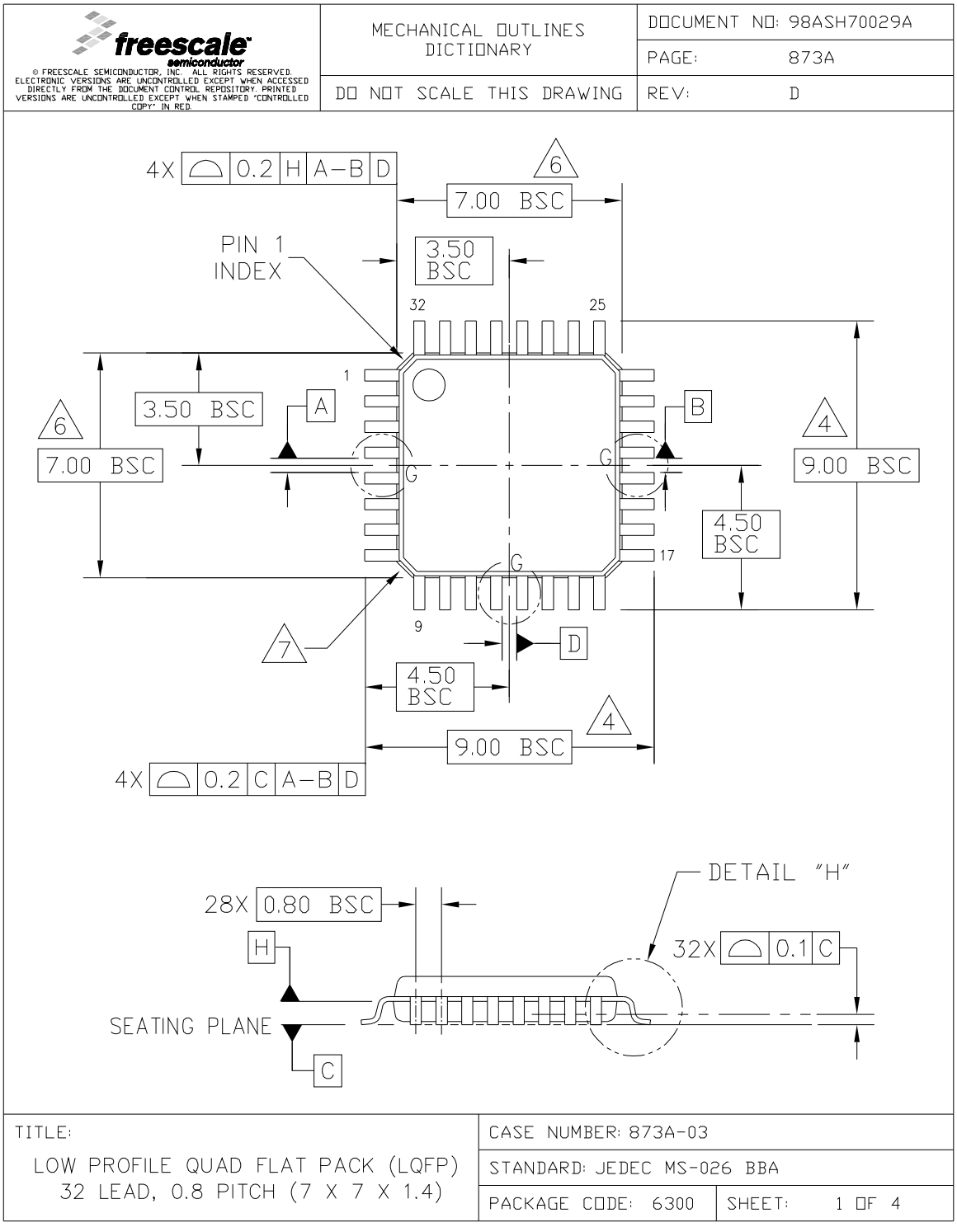


Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
0A	0000	TMR0	TMR0_ CSCTRL	DBG_EN		FAULT	ALT_LOAD	0	0	0	0	TCF2EN	TCF1EN	TCF2	TCF1	CL2		CL1	
0B	0000	TMR0	TMR0_ FILT	0	0	0	0	0	FILT_CNT			FILT_PER							
0C–0E	—	TMR0	Reserved	RESERVED															
0F	000F	TMR0	TMR_ ENBL	0	0	0	0	0	0	0	0	0	0	0	0	ENBL			
10	0000	TMR1	TMR1_ COMP1	COMPARISON_1															
11	0000	TMR1	TMR1_ COMP2	COMPARISON_2															
12	0000	TMR1	TMR1_ CAPT	CAPTURE															
13	0000	TMR1	TMR1_ LOAD	LOAD															
14	0000	TMR1	TMR1_ HOLD	HOLD															
15	0000	TMR1	TMR1_ CNTR	COUNTER															
16	0000	TMR1	TMR1_ CTRL	CM			PCS				SCS		ONCE	LENGTH	DIR	COINIT	OM		
17	0000	TMR1	TMR1_ SCTRL	TCF	TCFIE	TOF	TOFIE	IEF	IEFIE	IPS	INPUT	CAPTURE_ MODE		MSTR	EEOF	VAL	FORCE	OPS	OEN
18	0000	TMR1	TMR1_ CMPLD1	COMPARATOR_LOAD_1															
19	0000	TMR1	TMR1_ CMPLD2	COMPARATOR_LOAD_2															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
4E	0000	SIM	SIM_GPSC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPS_C6	GPS_C0
4F	0000	SIM	SIM_GPSD	0	0	0	0	0	0	0	GPS_D3		GPS_D2		GPS_D1		GPS_D0		
50	0000	SIM	SIM_IPS0	0	0	0	0	IPS_FAULT3	IPS_FAULT2	IPS_FAULT1	IPS_PSRC2		IPS_PSRC1		IPS_PSRC0				
51	0000	SIM	SIM_IPS1	0	IPS_C2_WS			IPS_C1_WS			IPS_C0_WS		IPS_T1		IPS_T0				
52–5F	—	SIM	Reserved	RESERVED															
60	0208	PMC	PMC_SCR	OORF	LVDF	PPDF	PORF	OORIE	LVDIE	LVDRE	PPDE	LPR	LPRS	LPWUI	BGBE	LVDE	LVLS	PROT	
61	00--[2]	PMC	PMC_CR2	0	0	0	0	0	0	0	LPO_EN	LPO_TRIM			TRIM				
7F	—	PMC	Reserved	RESERVED															
80	0000	CMP0	CMP0_ CR0	0	0	0	0	0	0	0	0	0	FILTER_CNT			PMC		MMC	
81	0000	CMP0	CMP0_ CR1	0	0	0	0	0	0	0	0	SE	WE	0	PMODE	INV	COS	OPE	EN
82	0000	CMP0	CMP0_ FPR	0	0	0	0	0	0	0	0	FILT_PER							
83	0000	CMP0	CMP0_ SCR	0	0	0	0	0	0	0	0	0	0	0	IER	IEF	CFR	CFF	COUT
84–9F	—	CMP0	Reserved	RESERVED															
A0	0000	CMP1	CMP1_ CR0	0	0	0	0	0	0	0	0	0	FILTER_CNT			PMC		MMC	

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
A1	0000	CMP1	CMP1_ CR1	0	0	0	0	0	0	0	0	SE	WE	0	PMODE	INV	COS	OPE	EN
A2	0000	CMP1	CMP1_ FPR	0	0	0	0	0	0	0	0	FILT_PER							
A3	0000	CMP1	CMP1_ SCR	0	0	0	0	0	0	0	0	0	0	0	IER	IEF	CFR	CFF	COUT
A4–BF	—	CMP1	Reserved	RESERVED															
C0	0000	CMP2	CMP2_ CR0	0	0	0	0	0	0	0	0	0	FILTER_CNT			PMC		MMC	
C1	0000	CMP2	CMP2_ CR1	0	0	0	0	0	0	0	0	SE	WE	0	PMODE	INV	COS	OPE	EN
C2	0000	CMP2	CMP2_ FPR	0	0	0	0	0	0	0	0	FILT_PER							
C3	0000	CMP2	CMP2_ SCR	0	0	0	0	0	0	0	0	0	0	0	IER	IEF	CFR	CFF	COUT
C4–DF	—	CMP2	Reserved	RESERVED															
E0	0000	PIT	PIT_CTRL	0	0	0	0	0	0	0	0	0	PRESCALER				PRF	PRIE	CNT_EN
E1	0000	PIT	PIT_MOD	MODULO_VALUE															
E2	0000	PIT	PIT_CNTR	COUNTER_VALUE															
E3–FF	—	PIT	Reserved	RESERVED															
00	0000	PDB	PDB_SCR	PRESCALER			0	AOS		0	BOS		CONT	SWTRIG	TRIGSEL			ENA	ENB
01	0000	PDB	PDB_ DELAYA	DELAYA															