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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8006vwlr

  - Four programmable fault inputs with programmable digital filter
  - Double-buffered PWM registers
  - Separate deadtime insertions for rising and falling edges
  - Separate top and bottom pulse-width correction by means of software
  - Asymmetric PWM output within both Center Aligned and Edge Aligned operation
  - Separate top and bottom polarity control
  - Each complementary PWM signal pair allows selection of a PWM supply source from:
    - PWM generator
    - Internal timers
    - Analog comparator outputs
- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 14 channel external inputs plus seven internal inputs
  - Support simultaneous and software triggering conversions
  - ADC conversions can be synchronized by PWM and PDB modules
  - Sampling rate up to 400 KSPS for 10- or 12-bit conversion result; 470 KSPS for 8-bit conversion result
  - Two 16-word result registers
- Two programmable gain amplifier (PGAs)
  - Each PGA is designed to amplify and convert differential signals to a single-ended value fed to one of the ADC inputs
  - 1X, 2X, 4X, 8X, 16X, or 32X gain
  - Software and hardware triggers are available
  - Integrated sample/hold circuit
  - Includes additional calibration features:
    - Offset calibration eliminates any errors in the internal reference used to generate the VDDA/2 output center point
    - Gain calibration can be used to verify the gain of the overall datapath
    - Both features require software correction of the ADC result
- Three analog comparators (CMPs)
  - Selectable input source includes external pins, internal DACs
  - Programmable output polarity
  - Output can drive timer input, PWM fault input, PWM source, external pin output, and trigger ADCs
  - Output falling and rising edge detection able to generate interrupts
- One dual channel 16-bit multi-purpose timer module (TMR)
  - Two independent 16-bit counter/timers with cascading capability
  - Up to 96 MHz operating clock
  - Each timer has capture and compare and quadrature decoder capability
  - Up to 12 operating modes
  - Four external inputs and two external outputs
- One serial communication interface (SCI) with LIN slave functionality
  - Up to 96 MHz operating clock
  - Full-duplex or single-wire operation
  - Programmable 8- or 9- bit data format
  - Two receiver wakeup methods:
    - Idle line
    - Address mark

3.4 Product Documentation

The documents listed in Table 2 are required for a complete description and proper design with the 56F8006/56F8002. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at http://www.freescale.com.

Table 2. 56F8006/56F8002 Device Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit digital signal controller core processor, and the instruction set	DSP56800ERM
56F800x Peripheral Reference Manual	Detailed description of peripherals of the 56F8006 and 56F8002 devices	MC56F8006RM
56F80x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F800x family of devices	TBD
56F8006/56F8002 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F8006
56F8006/56F8002 Errata	Details any chip issues that might be present	MC56F8006E

4 Signal/Connection Descriptions

4.1 Introduction

The input and output signals of the 56F8006/56F8002 are organized into functional groups, as detailed in Table 3. Table 4 summarizes all device pins. In Table 4, each table row describes the signal or signals present on a pin, sorted by pin number.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins in 28 SOIC	Number of Pins in 32 LQFP	Number of Pins in 32 PSDIP	Number of Pins in 48 LQFP
Power Inputs (V_{DD}, V_{DDA})	2	2	2	4
Ground (V_{SS}, V_{SSA})	3	3	3	4
Reset[1]	1	1	1	1
Pulse Width Modulator (PWM) Ports[1]	10	12	12	12
Serial Peripheral Interface (SPI) Ports[1]	5	7	7	7
Serial Communications Interface 0 (SCI) Ports[1]	4	5	5	5
Inter-Integrated Circuit Interface (I^2C) Ports[1]	6	7	7	7
Analog-to-Digital Converter (ADC) Inputs[1]	16	18	18	24
High Speed Analog Comparator Inputs[1]	13	15	15	25
Programmable Gain Amplifiers (PGA)[1]	4	4	4	4
Dual Timer Module (TMR) Ports[1]	8	10	10	10
Programmable Delay Block (PDB)[1]	—	—	—	1
Clock[1]	5	5	5	5
JTAG/Enhanced On-Chip Emulation (EOnCE[1])	4	4	4	4

[1] Pins may be shared with other peripherals. See Table 4.

Table 4. 56F8006/56F8002 Pins (continued)

Pin Number				Pin Name	Peripherals												
28 SOIC	32 LQFP	32 PSDIP	48 LQFP		GPIO	I^2C	SCI	SPI	ADC	PGA	COMP	Dual Timer	PWM	Power and Ground	JTAG	Misc.
			28	GPIOE6	E6											
14	20	16	29	GPIOA5/*PWM5/FAULT2 or EXT_SYNC/TIN3*	A5							TIN3	PWM5, FAULT2 or EXT_ SYNC			
			30	V_{SS}										V_{SS}		
			31	V_{DD}										V_{DD}		
15	21	17	32	GPIOB0/*SCLK/SCL/ANB13/ PWM3/T1*	B0	SCL		SCLK	ANB13			T1	PWM3			
16	22	18	33	GPIOA4/*PWM4/SDA/FAULT1 /TIN2*	A4	SDA						TIN2	PWM4, FAULT1			
			34	GPIOE7/*CMP1_M3*	E7						CMP1_M3					
	23	19	35	GPIOA2/*PWM2*	A2								PWM2			
17	24	20	36	GPIOA3/*PWM3/TXD/EXTAL*	A3		TXD						PWM3			EXTAL
18	25	21	37	GPIOF0/*XTAL*	F0											XTAL
19	26	22	38	V_{DD}										V_{DD}		
20	27	23	39	V_{SS}										V_{SS}		
			40	GPIOF1/*CMP1_P3*	F1						CMP1_P3					
			41	GPIOF2/*CMP0_M3*	F2						CMP0_M3					
			42	GPIOF3/*CMP0_P3*	F3						CMP0_P3					
21	28	24	43	GPIOA1/*PWM1*	A1								PWM1			
22	29	25	44	GPIOA0/*PWM0*	A0								PWM0			
23	30	26	45	TDI/*GPIOD0/ANB12/$\overline{SS}$/ TIN2/CMP0_OUT*	D0			$\overline{SS}$	ANB12		CMP0_OUT	TIN2			TDI	
			46	GPIOC3/*EXT_TRIGGER*	C3											EXT_ TRGGER
24	31	27	47	TMS/*GPIOD3/ANB11/T1/ CMP1_OUT*	D3				ANB11		CMP1_OUT	T1			TMS	
25	32	28	48	**TDO**/*GPIOD1/ANB10/T0/ CMP2_OUT*	D1				ANB10		CMP2_OUT	T0			TDO	

1 Shielded ADC input.

4.2 Pin Assignment

MC56F8006 and MC56F8002 28-pin small outline IC (28SOIC) assignment is shown in Figure 4; MC56F8006 32-pin low-profile quad flat pack (32LQFP) is shown in Figure 5; MC56F8006 32-pin plastic shrink dual in-line package (PSDIP) is shown in Figure 6; MC56F8006 48-pin low-profile quad flat pack (48LQFP) is shown in Figure 7.

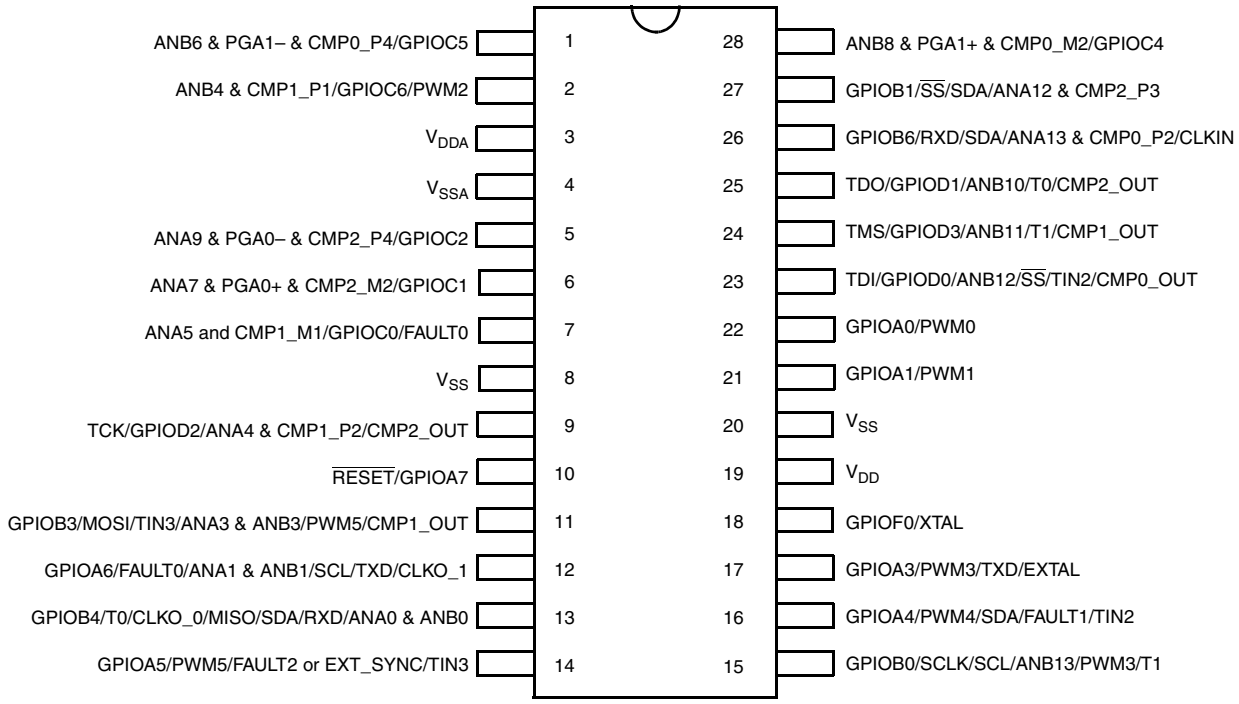

Figure 4. Top View, MC56F8006/MC56F8002 28-Pin SOIC Package

Table 5. 56F8006/56F8002 Signal and Package Information (continued)

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
GPIOE5 (ANA8 and CMP2_P1)				16	Input/ Output Analog Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA8 and CMP2_P1— Analog input to channel 8 of ADCA and positive input 1 of analog comparator 2. After reset, the default state is GPIOE5.
GPIOE6				28	Input/ Output	Input, internal pullup enable	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is GPIOE6.
GPIOE7 (CMP1_M3)				34	Input/ Output Analog Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin CMP1_M3 — Analog input to both negative input 3 of analog comparator 1. After reset, the default state is GPIOE7.
GPIOF0 (XTAL)	18	25	21	37	Input/ Output Analog Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. XTAL — External Crystal Oscillator Output. This output connects the internal crystal oscillator output to an external crystal or ceramic resonator. After reset, the default state is GPIOF0.
GPIOF1 (CMP1_P3)				40	Input/ Output Analog Input	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin CMP1_P3 — Analog input to both positive input 3 of analog comparator 1. After reset, the default state is GPIOF1
GPIOF2 (CMP0_M3)				41	Input/ Output Analog Input	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. CMP0_M3 — Analog input to both negative input 3 of analog comparator 0. After reset, the default state is GPIOF2.
GPIOF3 (CMP0_P3)				42	Input/ Output Analog Input	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. CMP0_P3 — Analog input to both positive input 3 of analog comparator 0. After reset, the default state is GPIOF3.

5 Memory Maps

5.1 Introduction

The 56F8006/56F8002 device is based on the 56800E core. It uses a dual Harvard-style architecture with two independent memory spaces for Data and Program. On-chip RAM is shared by both data and program spaces and flash memory is used only in program space.

This section provides memory maps for:

- Program address space, including the interrupt vector table
- Data address space, including the EOnCE memory and peripheral memory maps

On-chip memory sizes for the device are summarized in Table 6. Flash memories' restrictions are identified in the "Use Restrictions" column of Table 6.

Table 6. Chip Memory Configurations

On-Chip Memory	56F8006	56F8002	Use Restrictions
Program Flash (PFLASH)	8K x 16 or 16 KB	6K x 16 or 12 KB	Erase/program via flash interface unit and word writes to CDBW
Unified RAM (RAM)	1K x 16 or 2 KB	1K x 16 or 2 KB	Usable by the program and data memory spaces

5.2 Program Map

The 56F8006/56F8002 series provide up to 16 KB on-chip flash memory. It primarily accesses through the program memory buses (PAB; PDB). PAB is used to select program memory addresses; instruction fetches are performed over PDB. Data can be read and written to program memory space through primary data memory buses: CDBW for data write and CDBR for data read. Accessing program memory space over the data memory buses takes longer access time compared to accessing data memory space. The special MOVE instructions are provided to support these accesses. The benefit is that non time critical constants or tables can be stored and accessed in program memory.

The program memory map is shown in Table 7 and Table 8.

Table 7. Program Memory Map[1] for 56F8006 at Reset

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 83FF P: 0x00 8000	On-Chip RAM[2]: 2 KB
P: 0x00 7FFF P: 0x00 2000	RESERVED
P: 0x00 1FFF P: 0x00 0000	• Internal program flash: 16 KB • Interrupt vector table locates from 0x00 0000 to 0x00 0065 • COP reset address = 0x00 0002 • Boot location = 0x00 0000

1 All addresses are 16-bit word addresses.

2 This RAM is shared with data space starting at address X: 0x00 0000; see Figure 8.

Table 8. Program Memory Map[1] for 56F8002 at Reset (continued)

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 83FF P: 0x00 8000	On-Chip RAM[2]: 2 KB
P: 0x00 7FFF P: 0x00 2000	RESERVED
P: 0x00 1FFF P: 0x00 0800	• Internal program flash: 12 KB • Interrupt vector table locates from 0x00 0800 to 0x00 0865 • COP reset address = 0x00 0802 • Boot location = 0x00 0800
P: 0x00 07FF P: 0x00 0000	RESERVED

1 All addresses are 16-bit word addresses.

2 This RAM is shared with data space starting at address X: 0x00 0000; see Figure 9.

5.3 Data Map

The 56F8006/56F8002 series contain a dual access memory. It can be accessed from core primary data buses (XAB1; CDBW; CDBR) and secondary data buses (XAB2; XDB2). Addresses in data memory are selected on the XAB1 and XAB2 buses. Byte, word, and long data transfers occur on the 32-bit CDBR and CDBW buses. A second 16-bit read operation can be performed in parallel on the XDB2 bus.

Peripheral registers and on-chip JTAG/EOnCE controller registers are memory-mapped into data memory access. A special direct address mode is supported for accessing a first 64-location in data memory by using a single word instruction.

The data memory map is shown in Table 9.

Table 9. Data Memory Map[1]

Begin/End Address	Memory Allocation
X:0xFF FFFF X:0xFF FF00	EOnCE 256 locations allocated
X:0xFF FEFF X:0x01 0000	RESERVED
X:0x00 FFFF X:0x00 F000	On-Chip Peripherals 4096 locations allocated
X:0x00 EFFF X:0x00 8800	RESERVED
X:0x00 87FF X:0x00 8000	RESERVED
X:0x00 7FFF X:0x00 0400	RESERVED
X:0x00 03FF X:0x00 0000	On-Chip Data RAM 2 KB[2]

1 All addresses are 16-bit word addresses.

2 This RAM is shared with Program space starting at P: 0x00 8000. See Figure 8 and Figure 9.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 13. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulses per Pin	—	3	
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulses per Pin	—	3	
Latch-up	Minimum inpUt Voltage Limit		–2.5	V
	Maximum Input Voltage Limit		7.5	V

Table 14. 56F8006/56F8002 ESD Protection

Characteristic [1]	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	750	—	—	V
Latch-up current at T_A= 85°C (I_{LAT})	± 100			mA

1 Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

8.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 15. 28SOIC Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	70	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	47	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	55	°C/W

8.6 Supply Current Characteristics

Table 22. Supply Current Consumption

Mode	Conditions	Typical @ 3.3 V, 25 °C		Maximum @ 3.6 V, 105 °C		Maximum @ 3.6 V, 125 °C	
		I_{DD} [1]	I_{DDA}	I_{DD} [1]	I_{DDA}	I_{DD} [1]	I_{DDA}
Run	32 MHz device clock; relaxation oscillator (ROSC) in high speed mode; PLL engaged; All peripheral modules enabled. TMR and PWM using 1X clock; continuous MAC instructions with fetches from program flash; ADC/DAC powered on and clocked; comparator powered on.	41.52 mA	1.71 mA	53 mA	2.7 mA	53 mA	2.9 mA
LSrun [2]	200 kHz device clock; relaxation oscillator (ROSC) in standby mode; PLL disabled All peripheral modules disabled and clock gated off; simple loop with fetches from program flash;	340.75 µA	1.70 mA	480 µA	2.5 mA	495 µA	2.6 mA
LPrun [3]	32.768 kHz device clock; Clocked by a 32.768 kHz external crystal relaxation oscillator (ROSC) in power down; PLL disabled All peripheral modules disabled and clock gated off; simple loop with fetches from program flash;	166.30 µA	1.74 mA	390 µA	3.4 mA	399 µA	3.8 mA
Wait	32 MHz device clock relaxation oscillator (ROSC) in high speed mode PLL engaged; All non-communication peripherals enabled and running; all communication peripherals disabled but clocked; processor core in wait state	19.3 mA	1.78 mA	28 mA	2.7 mA	28 mA	2.8 mA
LSwait [2]	200 kHz device clock; relaxation oscillator (ROSC) in standby mode; PLL disabled; All peripheral modules disabled and clock gated off; processor core in wait state	265.42 µA	1.70 mA	380 µA	2.5 mA	398 µA	2.6 mA

- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

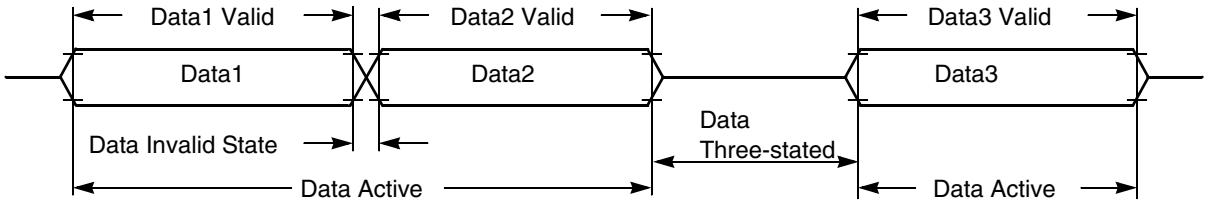

Figure 26. Signal States

8.13.1 Serial Peripheral Interface (SPI) Timing

Table 29. SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 125 62.5	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Enable lead time Master Slave	t_{ELD}	 — 31	 — —	 ns ns	Figure 30
Enable lag time Master Slave	t_{ELG}	 — 125	 — —	 ns ns	Figure 30
Clock (SCK) high time Master Slave	t_{CH}	 50 31	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Clock (SCK) low time Master Slave	t_{CL}	 50 31	 — —	 ns ns	Figure 30
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	Figure 30
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	Figure 30

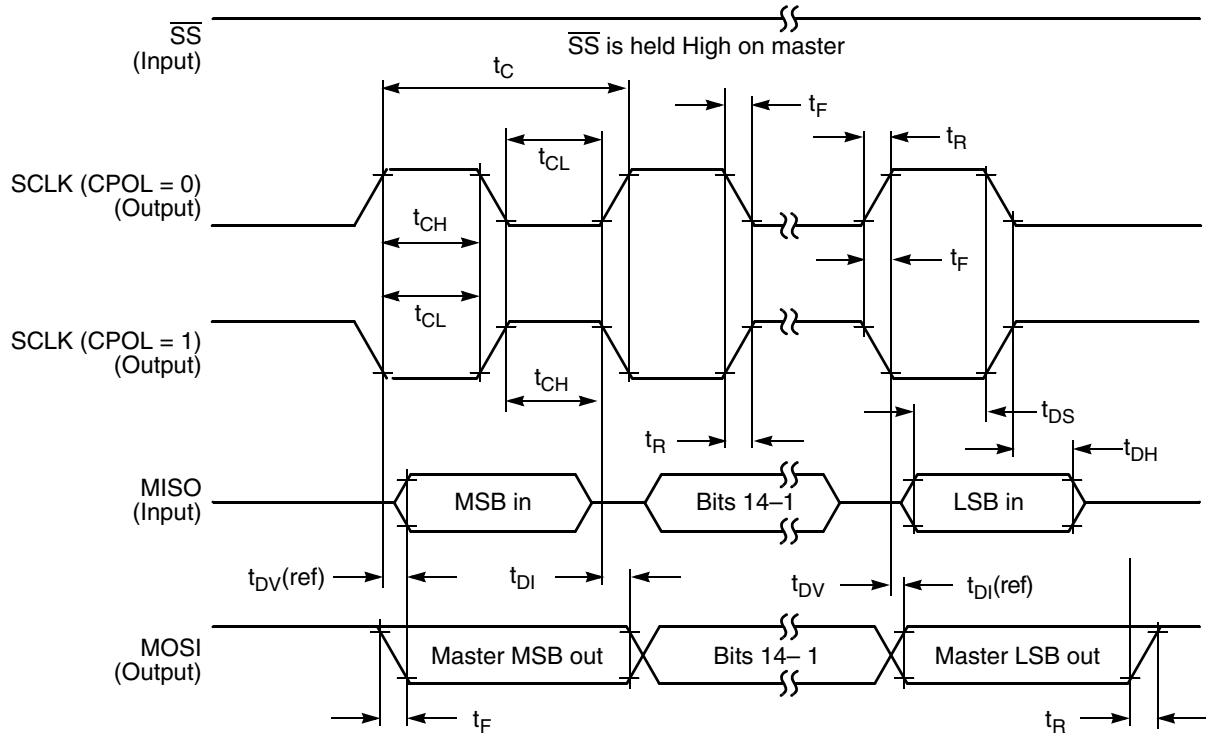

Figure 28. SPI Master Timing (CPHA = 1)

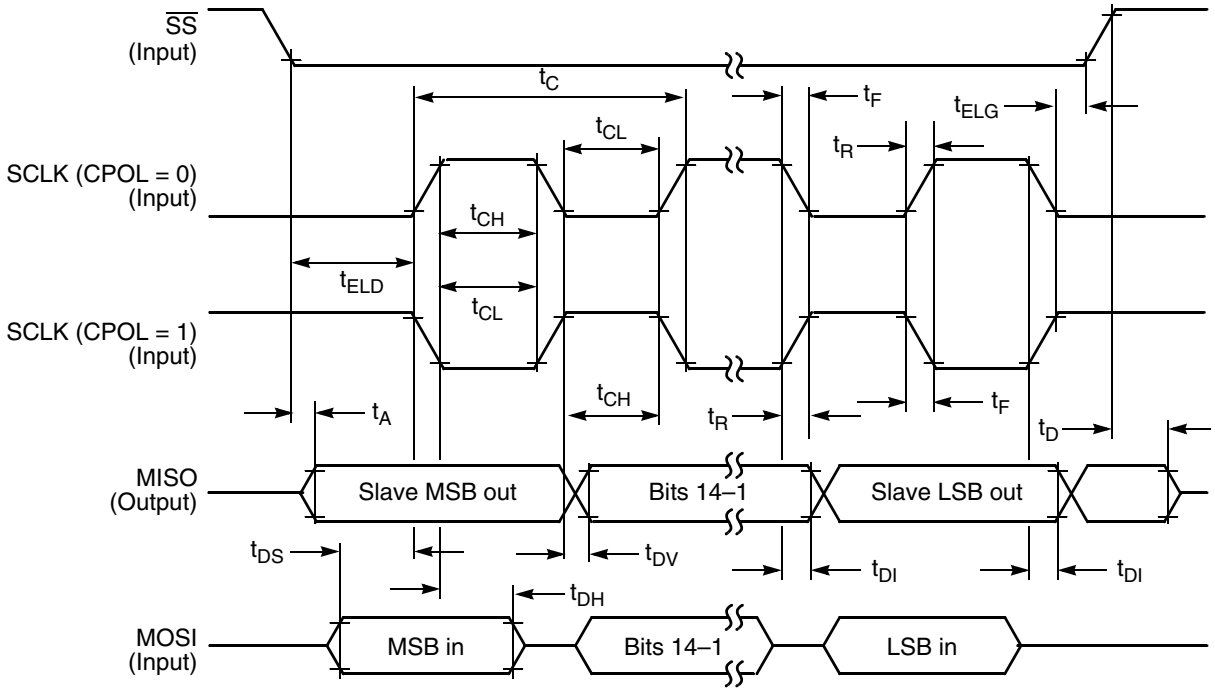

Figure 29. SPI Slave Timing (CPHA = 0)

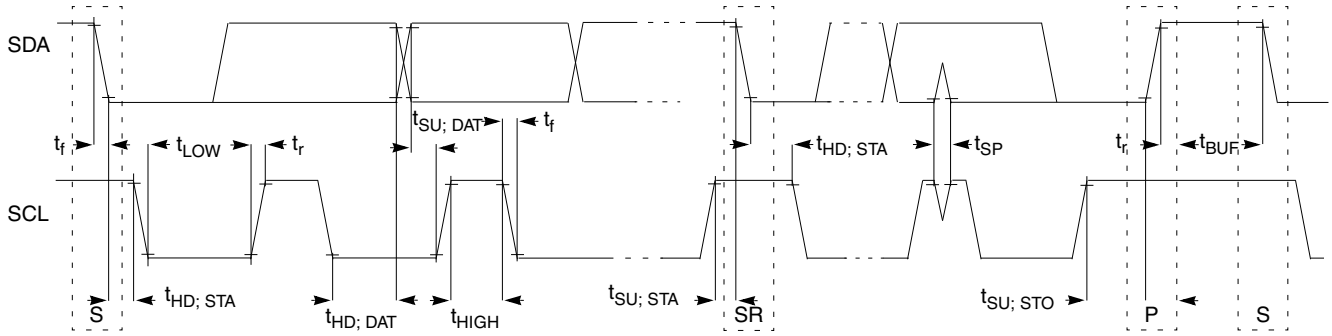

Figure 33. Timing Definition for Standard Mode Devices on the I^2C Bus

8.13.4 JTAG Timing

Table 32. JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation[1]	f_{OP}	DC	SYS_CLK/8	MHz	Figure 34
TCK clock pulse width	t_{PW}	50	—	ns	Figure 34
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 35
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 35
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 35
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 35

1 TCK frequency of operation must be less than 1/8 the processor rate.

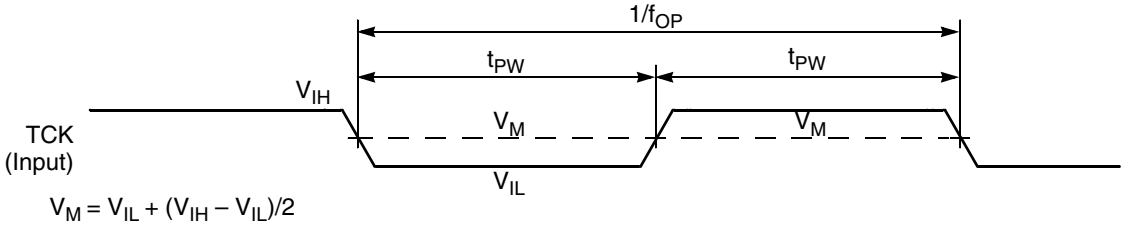

Figure 34. Test Clock Input Timing Diagram

junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

9.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the 56F8006/56F8002:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the 56F8006/56F8002 and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with V_{DDA} and V_{SSA} traces.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.22 µF–4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input state with internal pullup enabled. The typical value of internal pullup is around 33 kΩ. These internal pullups can be disabled by software.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10 Ω RC filter.
- External clamp diodes on analog input pins are recommended.

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. 751F–01 THRU –04 OBSOLETE. NEW STANDARD: 751F–05
6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	CASE NUMBER: 751F–05	
	STANDARD: MS–013AE	
	PACKAGE CODE: 2009	SHEET: 3 OF 4

Figure 38. 56F8006/56F8002 28-Pin SOIC Mechanical Information

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		PAGE: 932
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NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	CASE NUMBER: 932-03	
	STANDARD: JEDEC MS-026-BBC	
	PACKAGE CODE: 6089	SHEET: 2 OF 3

Figure 40. 56F8006/56F8002 48-Pin LQFP Mechanical Information

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
61	0000	ADC0	ADC0_ ADCSC2	0	0	0	0	0	0	0	0	ADACT	ADTRG	0	0	0	ECC	REFSEL	
62–65	—	ADC0	Reserved	RESERVED															
66	0000	ADC0	ADC0_ ADCCFG	0	0	0	0	0	0	0	0	ADLPC	ADIV		ADLSMP	MODE		ADICLK	
67–69	—	ADC0	Reserved	RESERVED															
6A	001F	ADC0	ADC0_ ADCSC1B	0	0	0	0	0	0	0	0	COCO	AIEN	ADCO	ADCH				
6B	0000	ADC0	ADC0_ ADCRA	0	ADR11	ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	0	0	0
6C	0000	ADC0	ADC0_ ADCRB	0	ADR11	ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	0	0	0
6D–6F	—	ADC0	Reserved	RESERVED															
80	001F	ADC1	ADC1_ ADCSC1A	0	0	0	0	0	0	0	0	COCO	AIEN	ADCO	ADCH				
81	0000	ADC1	ADC1_ ADCSC2	0	0	0	0	0	0	0	0	ADACT	ADTRG	0	0	0	ECC	REFSEL	
82–85	—	ADC1	Reserved	RESERVED															
86	0000	ADC1	ADC1_ ADCCFG	0	0	0	0	0	0	0	0	ADLPC	ADIV		ADLSMP	MODE		ADICLK	
87–89	—	ADC1	Reserved	RESERVED															
8A	001F	ADC1	ADC1_ ADCSC1B	0	0	0	0	0	0	0	0	COCO	AIEN	ADCO	ADCH				

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
C3	0000	PGA1	PGA1_STS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNNING	STCOMP
C4–DF	—	PGA1	Reserved	RESERVED															
E0	0200	SCI	SCI_RATE	SBR													FRAC_SBR		
E1	0000	SCI	SCI_CTRL1	LOOP	SWAI	RSRC	M	WAKE	POL	PE	PT	TEIE	TIIE	RFIE	REIE	TE	RE	RWU	SBK
E2	0000	SCI	SCI_CTRL2	0	0	0	0	0	0	0	0	0	0	0	0	LIN_MODE	0	0	0
E3	C000	SCI	SCI_STAT	TDRE	TIDLE	RDRF	RIDLE	OR	NF	FE	PF	0	0	0	0	LSE	0	0	RAF
E4	0000	SCI	SCI_DATA	0	0	0	0	0	0	0	RECEIVE_TRANSMIT_DATA								
E5–FF	—	SCI	Reserved	RESERVED															
00	6141	SPI	SPI_SCTRL	SPR			DSO	ERRIE	MODFEN	SPRIE	SPMSTR	CPOL	CPHA	SPE	SPTIE	SPRF	OVRF	MODF	SPTE
01	000F	SPI	SPI_DSCTRL	WOM	0	0	BD2X	SSB_IN	SSB_DATA	SSB_ODM	SSB_AUTO	SSB_DDR	SSB_STRB	SSB_OVER	SPR3	DS			
02	0000	SPI	SPI_DRCV	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
03	0000	SPI	SPI_DXMIT	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
04–1F	—	SPI	Reserved	RESERVED															
20	0000	I2C	I2C_ADDR	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	0
21	0000	I2C	I2C_FREQDIV	0	0	0	0	0	0	0	0	MULT		ICR					

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
60	0011	OCCS	OCCS_ CTRL	PLLIE1		PLLIE0		LOCIE	0	0	0	LCKON	0	0	PLLPD	0	PRECS	ZSRC	
61	2000	OCCS	OCCS_ DIVBY	LORTP				COD				0	0	0	0	0	0	0	0
62	0015	OCCS	OCCS_ STAT	LOLI1	LOLI0	LOCI	0	0	0	0	0	0	LCK1	LCK0	PLLPDN	0	COSC_RDY	ZSRC	
64	1611	OCCS	OCCS_ OCTRL	ROPD	ROSB	COHL	CLK_MODE	RANGE	EXT_SEL	TRIM									
65	0000	OCCS	OCCS_ CLKCHKR	CHK_ENA	REFERENCE_CNT														
66	0000	OCCS	OCCS_ CLKCHKT	0	0	0	0	0	0	0	0	0	TARGET_CNT						
67	0000	OCCS	OCCS_ PROT	0	0	0	0	0	0	0	0	0	0	FRQEP		OSCEP		PLLEP	
68–7F	—	OCCS	Reserved	RESERVED															
80	00FF	GPIOA	GPIOA_ PUR	0	0	0	0	0	0	0	0	PU							
81	0000	GPIOA	GPIOA_DR	0	0	0	0	0	0	0	0	D							
82	0000	GPIOA	GPIOA_ DDR	0	0	0	0	0	0	0	0	DD							
83	0080	GPIOA	GPIOA_ PER	0	0	0	0	0	0	0	0	PE							
84	—	GPIOA	Reserved	RESERVED															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
A7	0000	GPIOB	GPIOB_ IPR	0	0	0	0	0	0	0	0	IPR							
A8	0000	GPIOB	GPIOB_ IESR	0	0	0	0	0	0	0	0	IESR							
A9	—	GPIOB	Reserved	RESERVED															
AA	0000	GPIOB	GPIOB_ RAWDATA	0	0	0	0	0	0	0	0	RAWDATA							
AB	0000	GPIOB	GPIOB_ DRIVE	0	0	0	0	0	0	0	0	DRIVE							
AC	00FF	GPIOB	GPIOB_IFE	0	0	0	0	0	0	0	0	IFE							
AD	0000	GPIOB	GPIOB_ SLEW	0	0	0	0	0	0	0	0	SLEW							
AE–BF	—	GPIOB	Reserved	RESERVED															
C0	00FF	GPIOC	GPIOC_ PUR	0	0	0	0	0	0	0	0	PUR							
C1	0000	GPIOC	GPIOC_DR	0	0	0	0	0	0	0	0	DR							
C2	0000	GPIOC	GPIOC_ DDR	0	0	0	0	0	0	0	0	DDR							
C3	0080	GPIOC	GPIOC_ PER	0	0	0	0	0	0	0	0	PER							
C4	—	GPIOC	Reserved	RESERVED															
C5	0000	GPIOC	GPIOC_ IENR	0	0	0	0	0	0	0	0	IENR							
C6	0000	GPIOC	GPIOC_ IPOLR	0	0	0	0	0	0	0	0	IPOLR							
C7	0000	GPIOC	GPIOC_ IPR	0	0	0	0	0	0	0	0	IPR							
C8	0000	GPIOC	GPIOC_ IESR	0	0	0	0	0	0	0	0	IESR							

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
4E	0000	SIM	SIM_GPSC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPS_C6	GPS_C0
4F	0000	SIM	SIM_GPSD	0	0	0	0	0	0	0	GPS_D3		GPS_D2		GPS_D1		GPS_D0		
50	0000	SIM	SIM_IPS0	0	0	0	0	IPS_FAULT3	IPS_FAULT2	IPS_FAULT1	IPS_PSRC2		IPS_PSRC1		IPS_PSRC0				
51	0000	SIM	SIM_IPS1	0	IPS_C2_WS			IPS_C1_WS			IPS_C0_WS		IPS_T1		IPS_T0				
52–5F	—	SIM	Reserved	RESERVED															
60	0208	PMC	PMC_SCR	OORF	LVDF	PPDF	PORF	OORIE	LVDIE	LVDRE	PPDE	LPR	LPRS	LPWUI	BGBE	LVDE	LVLS	PROT	
61	00--[2]	PMC	PMC_CR2	0	0	0	0	0	0	0	LPO_EN	LPO_TRIM			TRIM				
7F	—	PMC	Reserved	RESERVED															
80	0000	CMP0	CMP0_ CR0	0	0	0	0	0	0	0	0	0	FILTER_CNT			PMC		MMC	
81	0000	CMP0	CMP0_ CR1	0	0	0	0	0	0	0	0	SE	WE	0	PMODE	INV	COS	OPE	EN
82	0000	CMP0	CMP0_ FPR	0	0	0	0	0	0	0	0	FILT_PER							
83	0000	CMP0	CMP0_ SCR	0	0	0	0	0	0	0	0	0	0	0	IER	IEF	CFR	CFF	COUT
84–9F	—	CMP0	Reserved	RESERVED															
A0	0000	CMP1	CMP1_ CR0	0	0	0	0	0	0	0	0	0	FILTER_CNT			PMC		MMC	