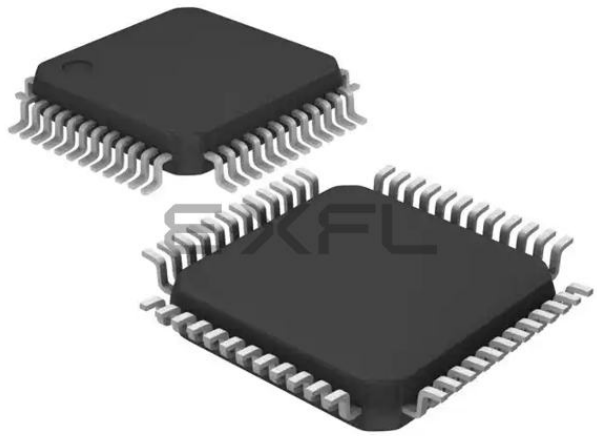

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pc56f8006vlf

1 MC56F8006/MC56F8002 Family Configuration

MC56F8006/MC56F8002 device comparison in Table 1.

Table 1. MC56F8006 Series Device Comparison

Feature	MC56F8006			MC56F8002
	28-pin	32-pin	48-pin	28-pin
Flash memory size (Kbytes)	16			12
RAM size (Kbytes)	2			
Analog comparators (ACMP)	3			
Analog-to-digital converters (ADC)	2			
Unshielded ADC inputs	6	7	7	6
Shielded ADC inputs	9	11	17	9
Total number of ADC input pins[1]	15	18	24	15
Programmable gain amplifiers (PGA)	2			
Pulse-width modulator (PWM) outputs	6			
PWM fault inputs	3	4	4	3
Inter-integrated circuit (IIC)	1			
Serial peripheral interface (SPI)	1			
High speed serial communications interface (SCI)	1			
Programmable interrupt timer (PIT)	1			
Programmable delay block (PDB)	1			
16-bit multi-purpose timers (TMR)	2			
Real-time counter (RTC)	1			
Computer operating properly (COP) timer	Yes			
Phase-locked loop (PLL)	Yes			
1 kHz on-chip oscillator	Yes			
8 MHz (400 kHz at standby mode) on-chip ROSC	Yes			
Crystal oscillator	Yes			
Power management controller (PMC)	Yes			
IEEE 1149.1 Joint Test Action Group (JTAG) interface	Yes			
Enhanced on-chip emulator (EOnCE) IEEE 1149.1 Joint Test Action Group (JTAG) interface	Yes			

[1] Some ADC inputs share the same pin. See Table 4.

- Clock sources
  - On-chip relaxation oscillator with two user selectable frequencies: 400 kHz for low speed mode, 8 MHz for normal operation
  - On-chip low-power 1 kHz oscillator can be selected as clock source to the RTC and/or COP
  - External clock: crystal oscillator, ceramic resonator, and external clock source
- Power management controller (PMC)
  - On-chip regulator for digital and analog circuitry to lower cost and reduce noise
  - Integrated power-on reset (POR)
  - Low-voltage interrupt with a user selectable trip voltage of 1.81 V or 2.31 V
  - User selectable brown-out reset
  - Run, wait, and stop modes
  - Low-power run, wait, and stop modes
  - Partial power down mode
- Up to 40 general-purpose I/O (GPIO) pins
  - Individual control for each pin to be in peripheral or GPIO mode
  - Individual input/output direction control for each pin in GPIO mode
  - Hysteresis and configurable pullup device on all input pins
  - Configurable slew rate and drive strength and optional input low pass filters on all output pins
  - 20 mA sink/source current
- JTAG/EOnCE debug programming interface for real-time debugging
  - IEEE 1149.1 Joint Test Action Group (JTAG) interface
  - EOnCE interface for real-time debugging

3.1.6 Power Saving Features

- Three low power modes
  - Low-speed run, wait, and stop modes: 200 kHz IP bus clock provided by ROSC
  - Low-power run, wait, and stop modes: clock provided by external 32–38.4 kHz crystal
  - Partial power down mode
- Low power external oscillator can be used in any low-power mode to provide accurate clock to active peripherals
- Low power real time counter for use in run, wait, and stop modes with internal and external clock sources
- 32 µs typical wakeup time from partial power down modes
- Each peripheral can be individually disabled to save power

3.2 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit, and development system cards support concurrent engineering. Together, PE, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

A full set of programmable peripherals — PWM, PGAs, ADCs, SCI, SPI, I^2C, PIT, timers, and analog comparators — supports various applications. Each peripheral can be independently shut down to save power. Any pin in these peripherals can also be used as general-purpose input/outputs (GPIOs).

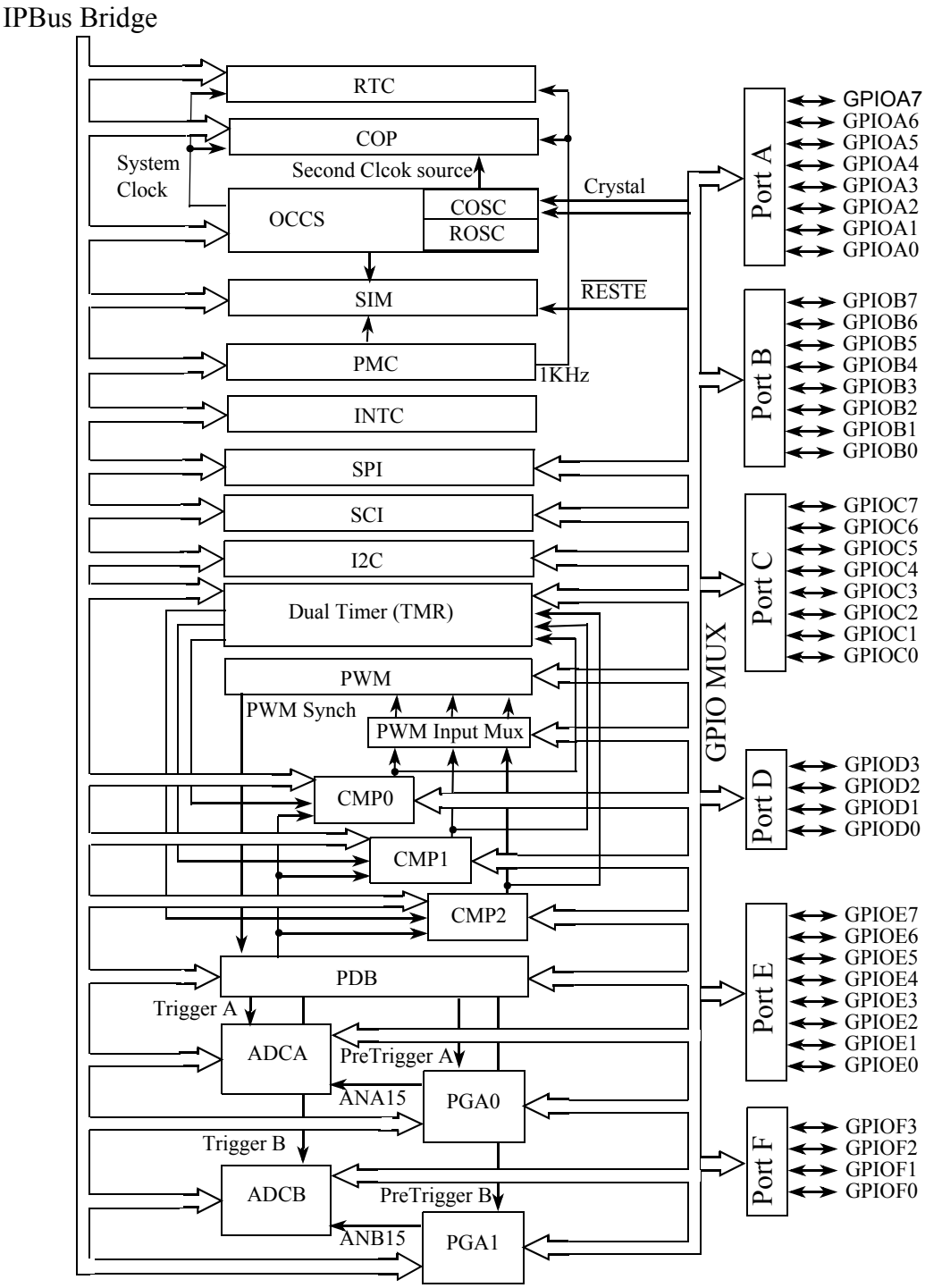

Figure 3. Peripheral Subsystem

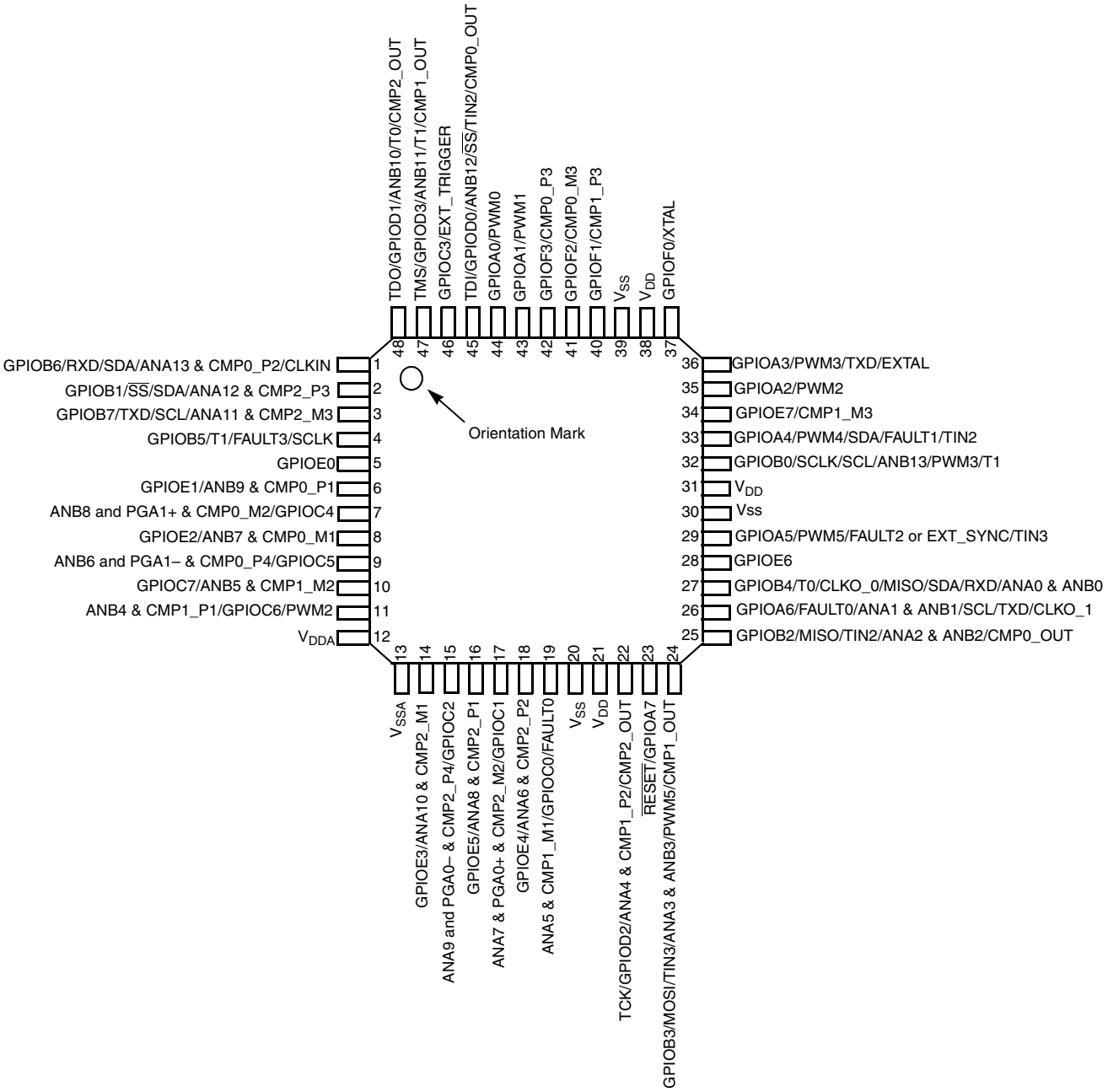

Figure 7. Top View, MC56F8006 48-Pin LQFP Package

4.3 56F8006/56F8002 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed via the GPIO module's peripheral enable registers (GPIO_x_PER) and SIM module's (GPS_xn) GPIO peripheral select registers. If CLKIN or XTAL is selected as device external clock input, the CLK_MOD bit in the OCCS oscillator control register (OSCTL) needs to be set too. EXT_SEL bit in OSCTL selects CLKIN or XTAL.

Table 5. 56F8006/56F8002 Signal and Package Information

Signal Name	28 SOIC	32 LQFP	32 PSDIP	48 LQFP	Type	State During Reset	Signal Description
V_{DD}				21	Supply	Supply	I/O Power — This pin supplies 3.3 V power to the chip I/O interface.
V_{DD}				31			
V_{DD}	19	26	22	38			
V_{SS}	8	13	9	20	Supply	Supply	I/O Ground — These pins provide ground for chip I/O interface.
V_{SS}				30			
V_{SS}	20	27	23	39			
V_{DDA}	3	8	4	12	Supply	Supply	Analog Power — This pin supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	4	9	5	13	Supply	Supply	Analog Ground — This pin supplies an analog ground to the analog modules. It must be connected to a clean power supply.
$\overline{\text{RESET}}$ (GPIOA7)	10	15	11	23	Input Input/ Output	Input, internal pullup enabled	Reset — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can be reset only via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOA0 (PWM0)	22	29	25	44	Input/ Output Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM0 — The PWM channel 0. After reset, the default state is GPIOA0.
GPIOA1 (PWM1)	21	28	24	43	Input/ Output Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM1 — The PWM channel 1. After reset, the default state is GPIOA1.
GPIOA2 (PWM2)		23	19	35	Input/ Output Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM2 — The PWM channel 2. After reset, the default state is GPIOA2.

On-chip RAM is also mapped into program space starting at P: 0x00 8000. This makes for easier online reprogramming of on-chip flash.

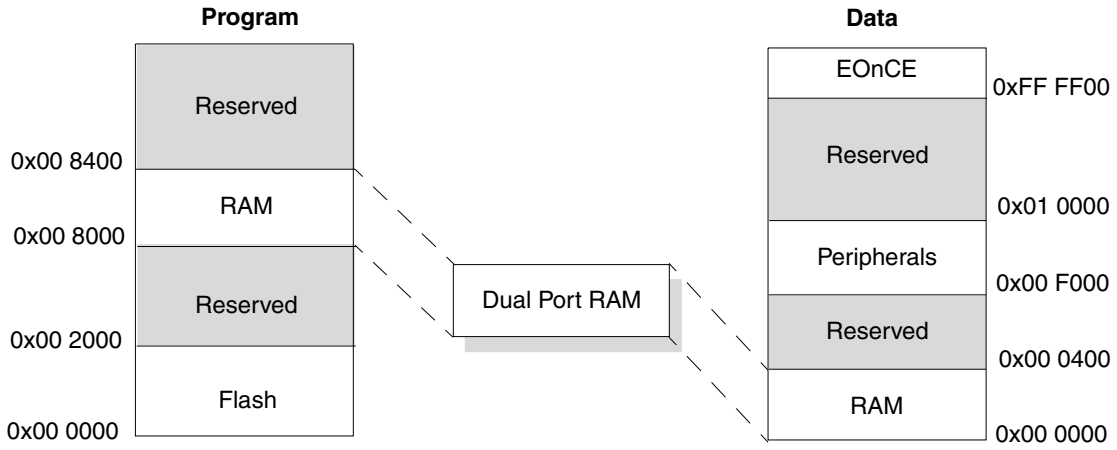

Figure 8. 56F8006 Dual Port RAM Map

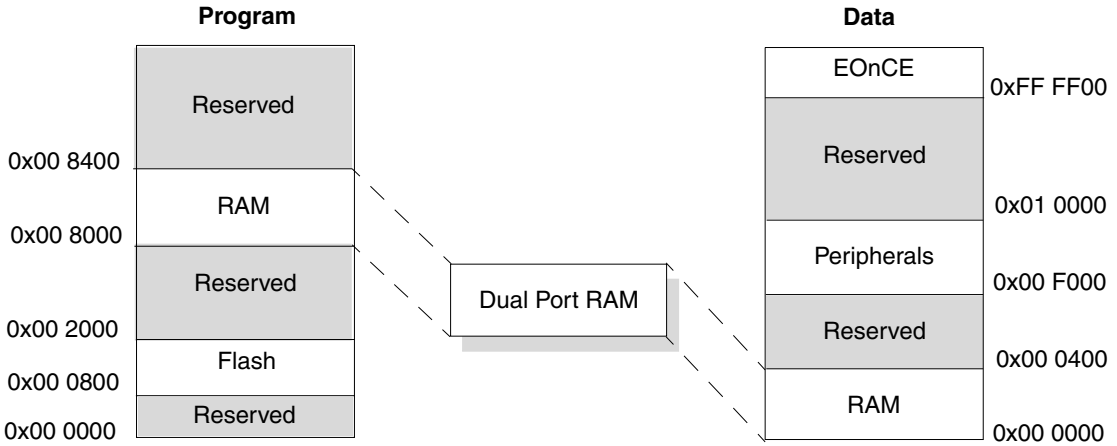

Figure 9. 56F8002 Dual Port RAM Map

5.4 Interrupt Vector Table and Reset Vector

The location of the vector table is determined by the vector base address register (VBA). The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower seven bits are determined based on the highest priority interrupt and are then appended onto VBA before presenting the full VAB to the core. Please see the *MC56F8006 Peripheral Reference Manual* for detail. The reset startup addresses of 56F8002 and 56F8006 are different.

- 56F8006 startup address is located at 0x00 0000. The reset value of VBA is reset to a value of 0x0000 that corresponds to address 0x00 0000
- 56F8002 startup address is located at 0x00 0800. The reset value of VBA is reset to a value of 0x0010 that corresponds to address 0x00 0800

By default, the chip reset address and COP reset address correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

The highest number vector, a user assignable vector USER6 (vector 50), can be defined as a fast interrupt if the instruction located in this vector location is not a JSR or BSR instruction. Please see section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for detail.

6 General System Control Information

6.1 Overview

This section discusses power pins, reset sources, interrupt sources, clock sources, the system integration module (SIM), ADC synchronization, and JTAG/EOnCE interfaces.

6.2 Power Pins

V_{DD}, V_{SS} and V_{DDA}, V_{SSA} are the primary power supply pins for the devices. This voltage source supplies power to all on-chip peripherals, I/O buffer circuitry and to internal voltage regulators. Device has multiple internal voltages provide regulated lower-voltage source for the peripherals, core, memory, and on-chip relaxation oscillators.

Typically, there are at least two separate capacitors across the power pins to bypass the glitches and provide bulk charge storage. In this case, there should be a bulk electrolytic or tantalum capacitor, such as a 10 µF tantalum capacitor, to provide bulk charge storage for the overall system and a 0.1 µF ceramic bypass capacitor located as near to the device power pins as practical to suppress high-frequency noise. Each pin must have a bypass capacitor for best noise suppression.

V_{DDA} and $V_{SSA}$are the analog power supply pins for the device. This voltage source supplies power to the ADC, PGA, and CMP modules. A 0.1 µF ceramic bypass capacitor should be located as near to the device V_{DDA} and V_{SSA} pins as practical to suppress high-frequency noise. V_{DDA} and V_{SSA} are also the voltage reference high and voltage reference low inputs, respectively, for the ADC module.

6.3 Reset

Resetting the device provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values and the program counter is loaded from the reset vector. On-chip peripheral modules are disabled and I/O pins are initially configured as the reset status shown in Table 5. The 56F8006/56F8002 has the following sources for reset:

- Power-on reset (POR)
- Partial power down reset (PPD)
- Low-voltage detect (LVD)
- External pin reset (EXTR)
- Computer operating properly loss of reference reset (COP_LOR)
- Computer operating properly time-out reset (COP_CPU)
- Software Reset (SWR)

Each of these sources has an associated bit in the reset status register (RSTAT) in the system integration module (SIM).

The external pin reset function is shared with an GPIO port A7 on the $\overline{\text{RESET}}$/GPIOA7 pin. The reset function is enabled following any reset of the device. Bit 7 of GPIOA_PER register must be cleared to use this pin as an GPIO port pin. When enabled as the $\overline{\text{RESET}}$ pin, an internal pullup device is automatically enabled.

6.4 On-chip Clock Synthesis

The on-chip clock synthesis (OCCS) module allows designers using an internal relaxation oscillator, an external crystal, or an external clock to run 56F8000 family devices at user-selectable frequencies up to 32 MHz.

The features of OCCS module include:

- Ability to power down the internal relaxation oscillator or crystal oscillator
- Ability to put the internal relaxation oscillator into standby mode
- Ability to power down the PLL

- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

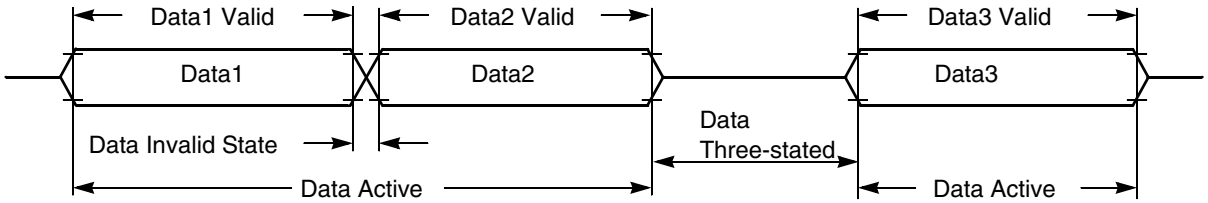

Figure 26. Signal States

8.13.1 Serial Peripheral Interface (SPI) Timing

Table 29. SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 125 62.5	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Enable lead time Master Slave	t_{ELD}	 — 31	 — —	 ns ns	Figure 30
Enable lag time Master Slave	t_{ELG}	 — 125	 — —	 ns ns	Figure 30
Clock (SCK) high time Master Slave	t_{CH}	 50 31	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Clock (SCK) low time Master Slave	t_{CL}	 50 31	 — —	 ns ns	Figure 30
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	Figure 30
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	Figure 30

Table 29. SPI Timing[1] (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Data valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30

1 Parameters listed are guaranteed by design.

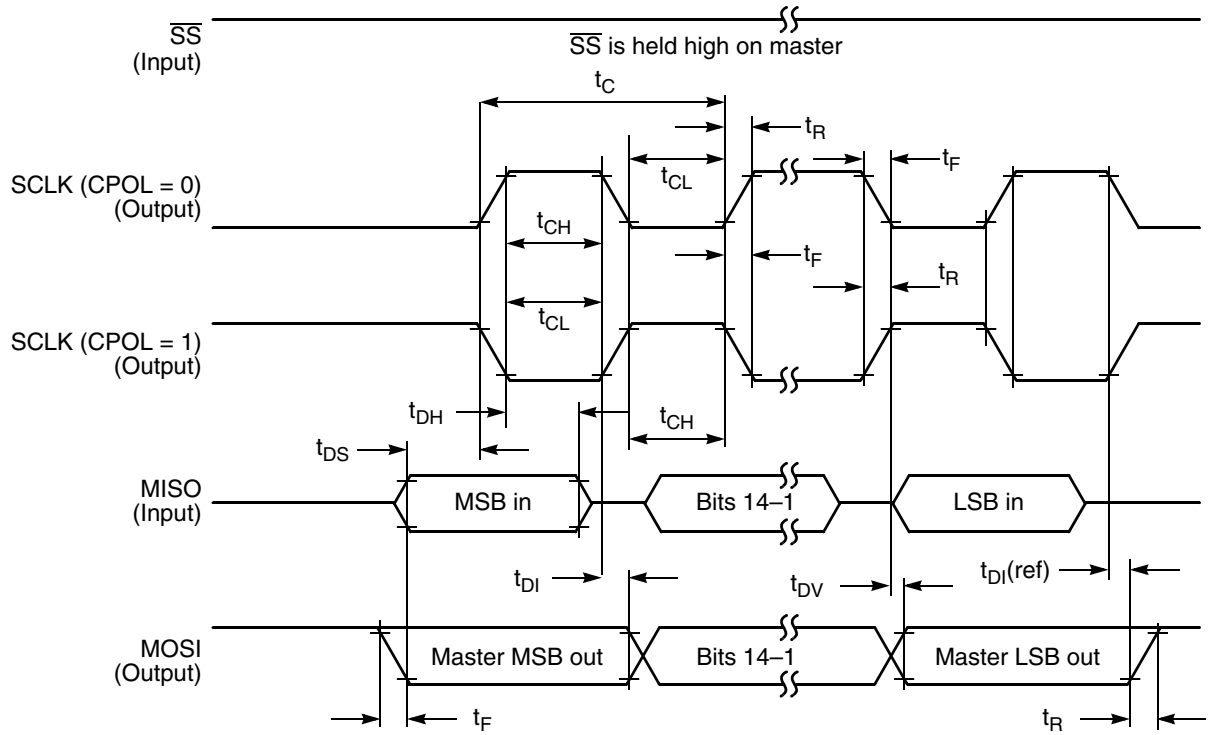

Figure 27. SPI Master Timing (CPHA = 0)

8.14 COP Specifications

Table 34. COP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Oscillator output frequency	LPFosc	500	1000	1500	Hz
Oscillator current consumption in partial power down mode	IDD		TBD		nA

8.15 PGA Specifications

Table 35. PGA Specifications

Parameter	Symbol	Min	Max	Unit
Digital logic inputs amplitude (_2p5 signal)	V_{2p5}		2.75	V
DC analog input level (@ V_{DD} = avdd3p3) PGA S/H stage enabled (BP=0) PGA S/H stage disabled (BP=1)	V_{IL}	0	 V_{DD} V_{DD} – 0.5	V
Max differential input voltage (@ Gain and V_{DD} = avdd3p3)	$V_{DIFFMAX}$		(V_{DD} – 1) x 0.5/gain	V
Linearity (@ voltage gain) 1x 2x 4x 8x 16x 32x	L_V	 1 – 1/2 LSB 2 – 1/2 LSB 4 – 1 LSB 8 – 1 LSB 16 – 4 LSB 32 – 4 LSB	 1 + 1/2 LSB 2 + 1/2 LSB 4 + 1 LSB 8 + 1 LSB 16 + 4 LSB 32 + 4 LSB	V/V
Gain error (@ voltage gain) 1x 2x 4x 8x 16x 32x	A_V		1%	V/V
Sampling frequency (pga_clk_2p5) normal mode (pga_lp_2p5 asserted) low power mode (pga_lp_2p5 negated)	SF_{max}		 8 4	 MHz
Input signal bandwidth Motor Control mode (BP=0) General Purpose mode (BP=1)	BW_{max}		 PGA sampling rate/2 PGA sampling rate/8	Hz
Internal voltage doubler clock frequency(pga_clk_doubler_2p5)	VD_{clk}	100	2000	kHz
Operating temperature	T	–40	125	°C

1 Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
3 Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
4 Based on input pad leakage current. Refer to pad electricals.

8.17 HSCMP Specifications

Table 38. HSCMP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{PWR}	1.8		3.6	V
Supply current, high speed mode (EN=1, PMODE=1, $V_{DDA} \geq V_{LVI\_trip}$)	I_{DDAHS}		150		μA
Supply current, low speed mode (EN=1, PMODE=0)	I_{DDALS}		10		μA
Supply current, off mode (EN=0,)	I_{DDAOFF}			100	nA
Analog input voltage	V_{AIN}	V_{SSA} – 0.01		V_{DDA} + 0.01	V
Analog input offset voltage	V_{AIO}			40	mV
Analog comparator hysteresis	V_H	3.0		20.0	mV
Propagation Delay, high speed mode (EN=1, PMODE=1), 2.4 V < V_{DDA} < 3.6 V	t_{DHSN}[1]		70	140	ns
Propagation Delay, High Speed Mode (EN=1, PMODE=1), 1.8 V < V_{DDA} < 2.4 V	t_{DHSB}[2]		70	249	ns
Propagation Delay, Low Speed Mode (EN=1, PMODE=0), 2.4 V < V_{DDA} < 3.6 V	t_{AINIT}[3]		400	600	ns
Propagation Delay, Low Speed Mode (EN=1, PMODE=0), 1.8 V < V_{DDA} < 2.4 V	t_{AINIT}[4]		400	600	ns

1 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.
2 Measured with an input waveform that switches 30mV above and below the reference, to the CMPO output pin. V_{DDA} < $V_{LVI\_WARNING}$ => LVI_WARNING ASSERTED.
3 Measured with an input waveform that switches 30mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI\_WARNING}$ => LVI_WARNING NOT ASSERTED.
4 Measured with an input waveform that switches 30mV above and below the reference, to the CMPO output pin. V_{DDA} < $V_{LVI\_WARNING}$ => LVI_WARNING ASSERTED.

8.18 Optimize Power Consumption

See Section 8.6, "Supply Current Characteristics," for a list of I_{DD} requirements for the 56F8006/56F8002. This section provides additional detail that can be used to optimize power consumption for a given application.

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		PAGE: 873A
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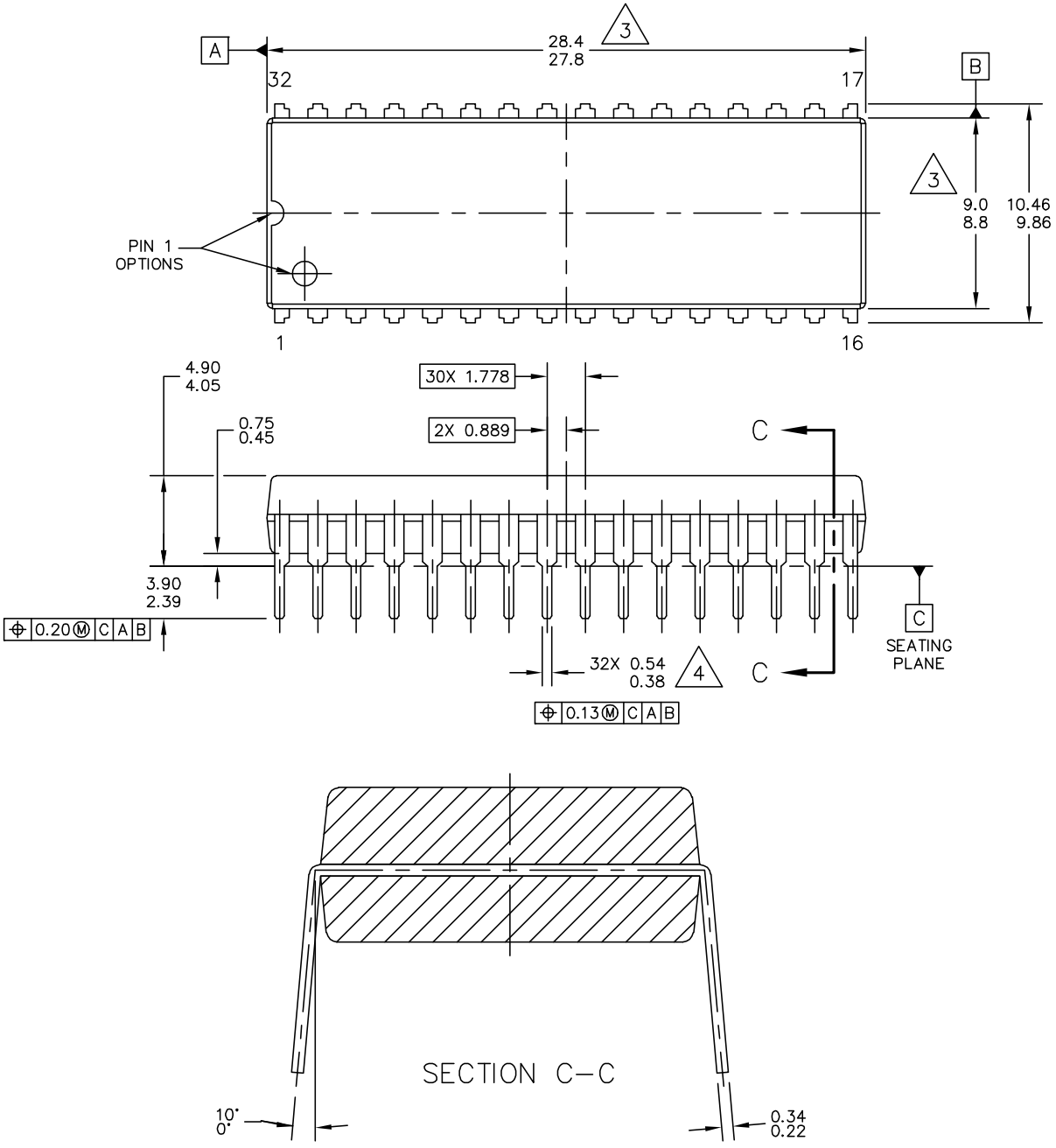
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	CASE NUMBER: 873A-03	
	STANDARD: JEDEC MS-026 BBA	
	PACKAGE CODE: 6300	SHEET: 3 OF 4

Figure 39. 56F8006/56F8002 32-Pin LQFP Mechanical Information

10.4 32-Pin PSDIP



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TITLE: 32 LEAD PDIP	DOCUMENT NO: 98ASA99330D	REV: A
	CASE NUMBER: 1376–02	25 APR 2005
	STANDARD: NON–JEDEC	

Table 43. Interrupt Vector Table Contents[1]

Peripheral	Vector Number	User Encoding	Priority Level	Vector Base Address +	Interrupt Function
Core				P:0x00	Reserved for Reset Overlay[2]
Core				P:0x02	Reserved for COP Reset Overlay
Core	2	N/A	3	P:0x04	Illegal Instruction
Core	3	N/A	3	P:0x06	HW Stack Overflow
Core	4	N/A	3	P:0x08	Misaligned Long Word Access
Core	5	N/A	3	P:0x0A	EOnCE Step Counter
Core	6	N/A	3	P:0x0C	EOnCE Breakpoint Unit
Core	7	N/A	3	P:0x0E	EOnCE Trace Buffer
Core	9	N/A	3	P:0x10	EOnCE Transmit Register Empty
Core	9	N/A	3	P:0x12	EOnCE Receive Register Full
PMC	10	0x0A	0	P:0x14	Low-Voltage Detector
PLL	11	0x0B	0	P:0x16	Phase-Locked Loop Loss of Locks and Loss of Clock
ADCA	12	0x0C	0	P:0x18	ADCA Conversion Complete
ADCB	13	0x0D	0	P:0x1A	ADCB Conversion Complete
PWM	14	0x0E	0	P:0x1C	Reload PWM and/or PWM Faults
CMP0	15	0x0F	0	P:0x1E	Comparator 0 Rising/Falling Flag
CMP1	16	0x10	0	P:0x20	Comparator 1 Rising/Falling Flag
CMP2	17	0x11	0	P:0x22	Comparator 2 Rising/Falling Flag
FM	18	0x12	0	P:0x24	Flash Memory Access Status
SPI	19	0x13	0	P:0x26	SPI Receiver Full
SPI	20	0x14	0	P:0x28	SPI Transmitter Empty
SCI	21	0x15	0	P:0x2A	SCI Transmitter Empty/Idle
SCI	22	0x16	0	P:0x2C	SCI Receiver Full/Overrun/Errors
I^2C	23	0x17	0	P:0x2E	I^2C Interrupt
PIT	24	0x18	0	P:0x30	Interval Timer Interrupt
TMR0	25	0x19	0	P:0x32	Dual Timer, Channel 0 Interrupt
TMR1	26	0x1A	0	P:0x34	Dual Timer, Channel 1 Interrupt
GPIOA	27	0x1B	0	P:0x36	GPIOA Interrupt
GPIOB	28	0x1C	0	P:0x38	GPIOB Interrupt
GPIOC	29	0x1D	0	P:0x3A	GPIOC Interrupt
GPIOD	30	0x1E	0	P:0x3C	GPIOD Interrupt
GPIOE	29	0x1F	0	P:0x3E	GPIOE Interrupt
GPIOF	30	0x20	0	P:0x40	GPIOF Interrupt
RTC	33	0x21	0	P:0x42	Real Time Clock

Table 43. Interrupt Vector Table Contents[1] (continued)

Peripheral	Vector Number	User Encoding	Priority Level	Vector Base Address +	Interrupt Function
Reserved	34- 39	0x22-0x27	0	P:0x44 - P:0x4E	Reserved
core	40	N/A	0	P:0x50	SW Interrupt 0
core	41	N/A	1	P:0x52	SW Interrupt 1
core	42	N/A	2	P:0x54	SW Interrupt 2
core	43	N/A	3	P:0x56	SW Interrupt 3
SWILP	44	N/A	-1	P:0x58	SW Interrupt Low Priority
USER1	45	N/A	1	P:0x5A	User Programmable Priority Level 1 Interrupt
USER2	46	N/A	1	P:0x5C	User Programmable Priority Level 1 Interrupt
USER3	47	N/A	1	P:0x5E	User Programmable Priority Level 1 Interrupt
USER4	48	N/A	2	P:0x60	User Programmable Priority Level 2 Interrupt
USER5	49	N/A	2	P:0x62	User Programmable Priority Level 2 Interrupt
USER6[3]	50	N/A	2	P:0x64	User Programmable Priority Level 2 Interrupt

1 Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.

2 If the VBA is set to the reset value, the first two locations of the vector table overlay the chip reset addresses because the reset address would match the base of this vector table.

3 USER6 vector can be defined as a fast interrupt if the instruction located in this vector location is not a JSR or BSR instruction. Please see section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for detail.

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
1A	0000	TMR1	TMR1_ CSCTRL	DBG_EN		FAULT	ALT_LOAD	0	0	0	0	TCF2EN	TCF1EN	TCF2	TCF1	CL2		CL1	
1B	0000	TMR1	TMR1_ FILT	0	0	0	0	0	FILT_CNT			FILT_PER							
1C–1F	—	TMR1	Reserved	RESERVED															
20	0000	PWM	PWM_ CTRL	LDFQ				HALF	IPOL2	IPOL1	IPOL0	PRSC		PWMRIE	PWMF	ISENS		LDOK	PWMEN
21	0000	PWM	PWM_ FCTRL	0	0	0	0	FPOL3	FPOL2	FPOL1	FPOL0	FIE3	FMODE3	FIE2	FMODE2	FIE1	FMODE1	FIE0	FMODE0
22	0000	PWM	PWM_ FLTACK	FPIN3	FFLAG3	FPIN2	FFLAG2	FPIN1	FFLAG1	FPIN0	FFLAG0		FTACK3		FTACK2		FTACK1		FTACK0
23	0000	PWM	PWM_ OUT	PAD_EN	0	OUTCTL5	OUTCTL4	OUTCTL3	OUTCTL2	OUTCTL1	OUTCTL0	0	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
24	0000	PWM	PWM_ CNTR	0	CR														
25	0000	PWM	PWM_ CMOD	0	PWMCM														
26	0000	PWM	PWM_ VAL0	PMVAL															
27	0000	PWM	PWM_ VAL1	PMVAL															
28	0000	PWM	PWM_ VAL2	PMVAL															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
61	0000	ADC0	ADC0_ ADCSC2	0	0	0	0	0	0	0	0	ADACT	ADTRG	0	0	0	ECC	REFSEL	
62–65	—	ADC0	Reserved	RESERVED															
66	0000	ADC0	ADC0_ ADCCFG	0	0	0	0	0	0	0	0	ADLPC	ADIV		ADLSMP	MODE		ADICLK	
67–69	—	ADC0	Reserved	RESERVED															
6A	001F	ADC0	ADC0_ ADCSC1B	0	0	0	0	0	0	0	0	COCO	AIEN	ADCO	ADCH				
6B	0000	ADC0	ADC0_ ADCRA	0	ADR11	ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	0	0	0
6C	0000	ADC0	ADC0_ ADCRB	0	ADR11	ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	0	0	0
6D–6F	—	ADC0	Reserved	RESERVED															
80	001F	ADC1	ADC1_ ADCSC1A	0	0	0	0	0	0	0	0	COCO	AIEN	ADCO	ADCH				
81	0000	ADC1	ADC1_ ADCSC2	0	0	0	0	0	0	0	0	ADACT	ADTRG	0	0	0	ECC	REFSEL	
82–85	—	ADC1	Reserved	RESERVED															
86	0000	ADC1	ADC1_ ADCCFG	0	0	0	0	0	0	0	0	ADLPC	ADIV		ADLSMP	MODE		ADICLK	
87–89	—	ADC1	Reserved	RESERVED															
8A	001F	ADC1	ADC1_ ADCSC1B	0	0	0	0	0	0	0	0	COCO	AIEN	ADCO	ADCH				

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
8B	0000	ADC1	ADC1_ ADCRA	0	ADR11	ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	0	0	0
8C	0000	ADC1	ADC1_ ADCRB	0	ADR11	ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	0	0	0
8D–8F	—	ADC1	Reserved	RESERVED															
A0	0000	PGA0	PGA0_ CNTL0	0	0	0	0	0	0	0	0	TM	GAINSEL					LP	EN
A1	0002	PGA0	PGA0_ CNTL1	0	0	0	0	0	0	0	0	PPDIS	PARMODE	0	CALMODE		CPD		
A2	000E	PGA0	PGA0_ CNTL2	0	0	0	0	0	0	0	0	0	0	SWTRIG	NUM_CLK_GS			ADIV	
A3	0000	PGA0	PGA0_STS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNNING	STCOMP
A4–BF	—	PGA0	Reserved	RESERVED															
C0	0000	PGA1	PGA1_ CNTL0	0	0	0	0	0	0	0	0	TM	GAINSEL					LP	EN
C1	0002	PGA1	PGA1_ CNTL1	0	0	0	0	0	0	0	0	PPDIS	PARMODE	0	CALMODE		CPD		
C2	000E	PGA1	PGA1_ CNTL2	0	0	0	0	0	0	0	0	0	0	SWTRIG	NUM_CLK_GS			ADIV	

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
A7	0000	GPIOB	GPIOB_ IPR	0	0	0	0	0	0	0	0	IPR							
A8	0000	GPIOB	GPIOB_ IESR	0	0	0	0	0	0	0	0	IESR							
A9	—	GPIOB	Reserved	RESERVED															
AA	0000	GPIOB	GPIOB_ RAWDATA	0	0	0	0	0	0	0	0	RAWDATA							
AB	0000	GPIOB	GPIOB_ DRIVE	0	0	0	0	0	0	0	0	DRIVE							
AC	00FF	GPIOB	GPIOB_IFE	0	0	0	0	0	0	0	0	IFE							
AD	0000	GPIOB	GPIOB_ SLEW	0	0	0	0	0	0	0	0	SLEW							
AE–BF	—	GPIOB	Reserved	RESERVED															
C0	00FF	GPIOC	GPIOC_ PUR	0	0	0	0	0	0	0	0	PUR							
C1	0000	GPIOC	GPIOC_DR	0	0	0	0	0	0	0	0	DR							
C2	0000	GPIOC	GPIOC_ DDR	0	0	0	0	0	0	0	0	DDR							
C3	0080	GPIOC	GPIOC_ PER	0	0	0	0	0	0	0	0	PER							
C4	—	GPIOC	Reserved	RESERVED															
C5	0000	GPIOC	GPIOC_ IENR	0	0	0	0	0	0	0	0	IENR							
C6	0000	GPIOC	GPIOC_ IPOLR	0	0	0	0	0	0	0	0	IPOLR							
C7	0000	GPIOC	GPIOC_ IPR	0	0	0	0	0	0	0	0	IPR							
C8	0000	GPIOC	GPIOC_ IESR	0	0	0	0	0	0	0	0	IESR							

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
A1	0000	CMP1	CMP1_ CR1	0	0	0	0	0	0	0	0	SE	WE	0	PMODE	INV	COS	OPE	EN
A2	0000	CMP1	CMP1_ FPR	0	0	0	0	0	0	0	0	FILT_PER							
A3	0000	CMP1	CMP1_ SCR	0	0	0	0	0	0	0	0	0	0	0	IER	IEF	CFR	CFF	COUT
A4–BF	—	CMP1	Reserved	RESERVED															
C0	0000	CMP2	CMP2_ CR0	0	0	0	0	0	0	0	0	0	FILTER_CNT			PMC		MMC	
C1	0000	CMP2	CMP2_ CR1	0	0	0	0	0	0	0	0	SE	WE	0	PMODE	INV	COS	OPE	EN
C2	0000	CMP2	CMP2_ FPR	0	0	0	0	0	0	0	0	FILT_PER							
C3	0000	CMP2	CMP2_ SCR	0	0	0	0	0	0	0	0	0	0	0	IER	IEF	CFR	CFF	COUT
C4–DF	—	CMP2	Reserved	RESERVED															
E0	0000	PIT	PIT_CTRL	0	0	0	0	0	0	0	0	0	PRESCALER				PRF	PRIE	CNT_EN
E1	0000	PIT	PIT_MOD	MODULO_VALUE															
E2	0000	PIT	PIT_CNTR	COUNTER_VALUE															
E3–FF	—	PIT	Reserved	RESERVED															
00	0000	PDB	PDB_SCR	PRESCALER			0	AOS		0	BOS		CONT	SWTRIG	TRIGSEL			ENA	ENB
01	0000	PDB	PDB_ DELAYA	DELAYA															