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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 16
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pc56f8006vwl

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three internal address buses
- Four internal data buses
- Instruction set supports DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, processor speed–independent, real-time debugging

3.1.2 Operation Range

- 1.8 V to 3.6 V operation (power supplies and I/O)
- From power-on-reset: approximately 1.9 V to 3.6 V
- Ambient temperature operating range:
  - –40 °C to 125 °C

3.1.3 Memory

- Dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Flash security and protection that prevent unauthorized users from gaining access to the internal flash
- On-chip memory
  - 16 KB of program flash for 56F8006 and 12 KB of program flash for 56F8002
  - 2 KB of unified data/program RAM
- EEPROM emulation capability using flash

3.1.4 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: Level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction. Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Allow nested interrupt that higher priority level interrupt request can interrupt lower priority interrupt subroutine
- The masking of interrupt priority level is managed by the 56800E core
- One programmable fast interrupt that can be assigned to any interrupt source
- Notification to system integration module (SIM) to restart clock out of wait and stop states
- Ability to relocate interrupt vector table

3.1.5 Peripheral Highlights

- One multi-function, six-output pulse width modulator (PWM) module
  - Up to 96 MHz PWM operating clock
  - 15 bits of resolution
  - Center-aligned and edge-aligned PWM signal mode
  - Phase shifting PWM pulse generation

In Table 4, peripheral pins in bold identify reset state.

Table 4. 56F8006/56F8002 Pins

Pin Number				Pin Name	Peripherals											
28 SOIC	32 LQFP	32 PSDIP	48 LQFP		GPIO	I^2C	SCI	SPI	ADC	PGA	COMP	Dual Timer	PWM	Power and Ground	JTAG	Misc.
26	1	29	1	GPIOB6/*RXD/SDA/ANA13 and CMP0_P2/CLKIN*	B6	SDA	RXD		ANA13[1]		CMP0_P2					CLKIN
27	2	30	2	GPIOB1/*$\overline{SS}$/SDA/ANA12 andCMP2_P3*	B1	SDA		$\overline{SS}$	ANA12[1]		CMP2_P3					
	3	31	3	GPIOB7/*TXD/SCL/ANA11 and CMP2_M3*	B7	SCL	TXD		ANA11[1]		CMP2_M3					
	4	32	4	GPIOB5/*T1/FAULT3/SCLK*	B5			SCLK				T1	FAULT3			
			5	GPIOE0	E0											
			6	GPIOE1/*ANB9 and CMP0_P1*	E1				ANB9[1]		CMP0_P1					
28	5	1	7	ANB8 and PGA1+ and CMP0_M2/*GPIOC4*	C4				ANB8[1]	PGA1+	CMP0_M2					
			8	GPIOE2/*ANB7 and CMP0_M1*	E2				ANB7[1]		CMP0_M1					
1	6	2	9	ANB6 and PGA1– and CMP0_P4/*GPIOC5*	C5				ANB6[1]	PGA1–	CMP0_P4					
			10	GPIOC7/*ANB5 and CMP1_M2*	C7				ANB5[1]		CMP1_M2					
2	7	3	11	ANB4 and CMP1_P1/*GPIOC6/PWM2*	C6				ANB4[1]		CMP1_P1		PWM2			
3	8	4	12	V_{DDA}										V_{DDA}		
4	9	5	13	V_{SSA}										V_{SSA}		
			14	GPIOE3/*ANA10 and CMP2_M1*	E3				ANA10[1]		CMP2_M1					
5	10	6	15	ANA9 and PGA0– and CMP2_P4/*GPIOC2*	C2				ANA9[1]	PGA0–	CMP2_P4					
			16	GPIOE5/*ANA8 and CMP2_P1*	E5				ANA8[1]		CMP2_P1					
6	11	7	17	ANA7 and PGA0+ and CMP2_M2/*GPIOC1*	C1				ANA7[1]	PGA0+	CMP2_M2					
			18	GPIOE4/ANA6 and CMP2_P2	E4				ANA6[1]		CMP2_P2					
7	12	8	19	ANA5 and CMP1_M1/*GPIOC0/FAULT0*	C0				ANA5[1]		CMP1_M1		FAULT0			
8	13	9	20	V_{SS}										V_{SS}		
			21	V_{DD}										V_{DD}		
9	14	10	22	TCK/*GPIOD2/ANA4 and CMP1_P2/CMP2_OUT*	D2				ANA4[1]		CMP1_P2, CMP2_OUT				TCK	
10	15	11	23	$\overline{RESET}$/*GPIOA7*	A7											$\overline{RESET}$
11	16	12	24	GPIOB3/*MOSI/TIN3/ANA3 and ANB3/PWM5/CMP1_OUT*	B3			MOSI	ANA3[1] and ANB3[1]		CMP1_OUT	TIN3	PWM5			
	17	13	25	GPIOB2/*MISO/TIN2/ANA2 and ANB2/CMP0_OUT*	B2			MISO	ANA2 and ANB2		CMP0_OUT	TIN2				
12	18	14	26	GPIOA6/*FAULT0/ANA1 and ANB1/SCL/TXD/CLKO_1*	A6	SCL	TXD		ANA1 and ANB1				FAULT0			CLKO_1
13	19	15	27	GPIOB4/*T0/CLKO_0/MISO/ SDA/RXD/ANA0 and ANB0*	B4	SDA	RXD	MISO	ANA0 and ANB0			T0				CLKO_0

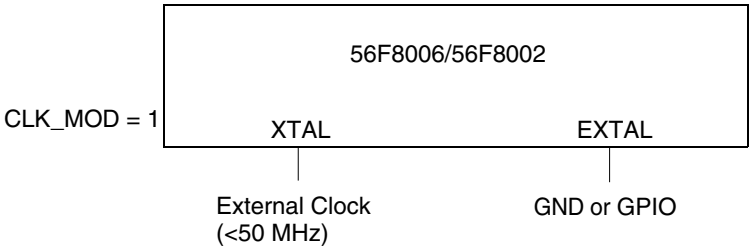


Figure 13. Connecting an External Clock Signal Using XTAL

6.4.4 Alternate External Clock Input

The recommended method of connecting an external clock is illustrated in Figure 14. The external clock source is connected to GPIOB6/RXD/SDA/ANA13 and CMP0_P2/CLKIN while EXT_SEL bit in OSCTL register is set and corresponding bits in GPIOB_PER register GPIO module and GPSB1 register in the system integration module (SIM) are set to the correct values. The external clock input must be generated using a relatively low impedance driver with maximum frequency not greater than 64 MHz.

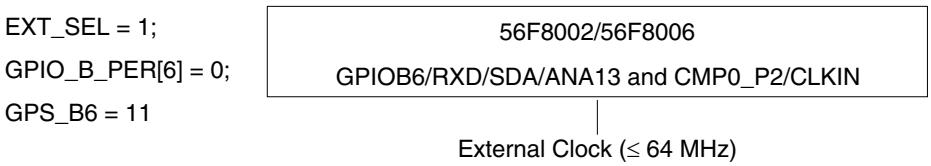


Figure 14. Connecting an External Clock Signal Using GPIO

6.5 Interrupt Controller

The 56F8006/56F8002 interrupt controller (INTC) module arbitrates the various interrupt requests (IRQs). The INTC signals to the 56800E core when an interrupt of sufficient priority exists and what address to jump to to service this interrupt.

The interrupt controller contains registers that allow up to three interrupt sources to be set to priority level 1 and other up to three interrupt sources to be set to priority level 2. By default, all peripheral interrupt sources are set to priority level 0. Next, all of the interrupt requests of a given level are priority encoded to determine the lowest numeric value of the active interrupt requests for that level. Within a given priority level, the lowest vector number is the highest priority and the highest vector number is the lowest.

The highest vector number, a user assignable vector USER6 (vector 50), can be defined as a fast interrupt if the instruction located in this vector location is not a JSR or BSR instruction. Please see section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for detail.

6.6 System Integration Module (SIM)

The SIM module is a system catchall for the glue logic that ties together the system-on-chip. It controls distribution of resets and clocks and provides a number of control features including the pin muxing control; inter-module connection control (for example connecting comparator output to PWM fault input); individual peripheral enable/disable; PWM, timer, and SCI clock rate control; enabling peripheral operation in stop mode; port configuration overwrite protection. For further information, see the *MC56F8006 Peripheral Reference Manual.*

The SIM is responsible for the following functions:

- Chip reset sequencing
- Core and peripheral clock control and distribution
- Stop/wait mode control
- System status control

8.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified Table 12 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 12. Absolute Maximum Ratings

(V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes	Min	Max	Unit
Supply Voltage Range	V_{DD}		–0.3	3.8	V
Analog Supply Voltage Range	V_{DDA}		–0.3	3.6	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		–0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		–0.3	0.3	V
Digital Input Voltage Range	V_{IN}	Pin Groups 1, 2	–0.3	V_{DD}+0.3	V
Oscillator Voltage Range	V_{OSC}	Pin Group 4	TBD	TBD	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	–0.3	3.6	V
Input clamp current, per pin (V_{IN} < 0)[1 2 3]	V_{IC}		—	–25.0	mA
Output clamp current, per pin (V_O < 0)[1 2 3]	V_{OC}		—	–20.0	mA
Output Voltage Range (Normal Push-Pull mode)	V_{OUT}	Pin Group 1	–0.3	V_{DD}	V
Ambient Temperature Industrial	T_A		–40	105	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		–55	150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating VDD range during instantaneous and operating maximum current conditions. If positive injection current (V_{In} > V_{DD}) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} loads shunt current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present or if the clock rate is low (which would reduce overall power consumption).

8.2.1 ESD Protection and Latch-Up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

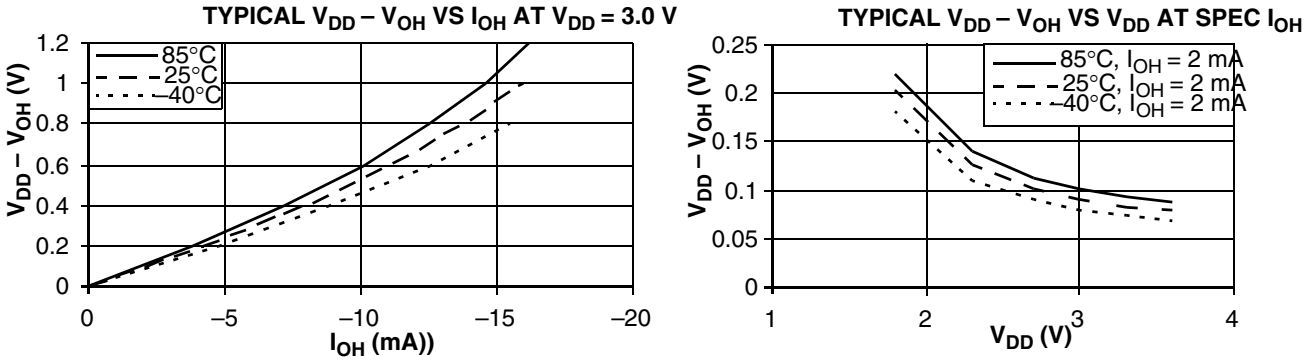


Figure 19. Typical High-Side (Source) Characteristics — Low Drive (GPIO_x_DRIVEn = 0)

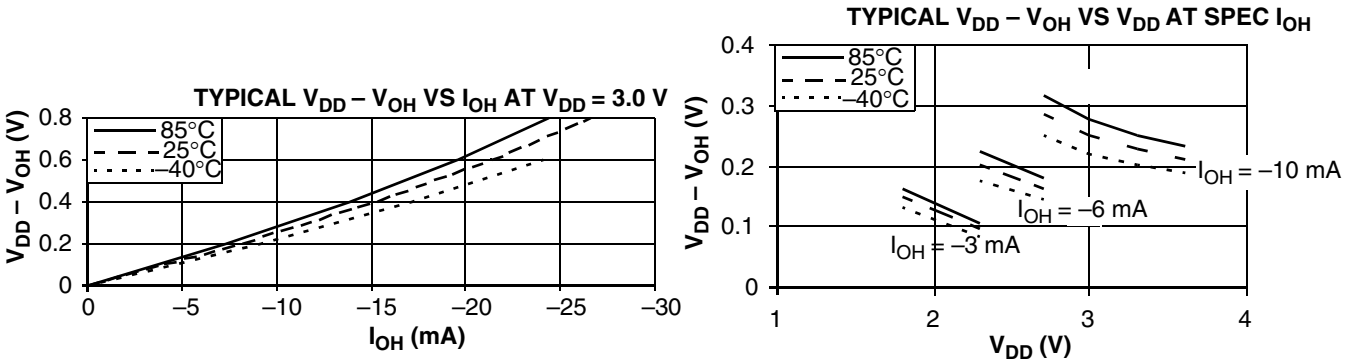


Figure 20. Typical High-Side (Source) Characteristics — High Drive (GPIO_x_DRIVEn = 1)

- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

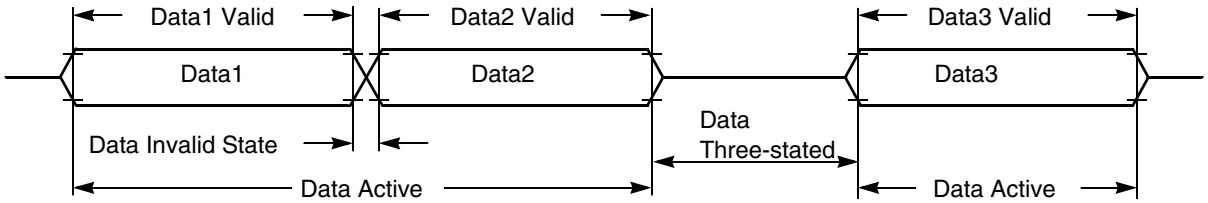


Figure 26. Signal States

8.13.1 Serial Peripheral Interface (SPI) Timing

Table 29. SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 125 62.5	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Enable lead time Master Slave	t_{ELD}	 — 31	 — —	 ns ns	Figure 30
Enable lag time Master Slave	t_{ELG}	 — 125	 — —	 ns ns	Figure 30
Clock (SCK) high time Master Slave	t_{CH}	 50 31	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Clock (SCK) low time Master Slave	t_{CL}	 50 31	 — —	 ns ns	Figure 30
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figure 27, Figure 28, Figure 29, Figure 30
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	Figure 30
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	Figure 30

Figure 31. RXD Pulse Width

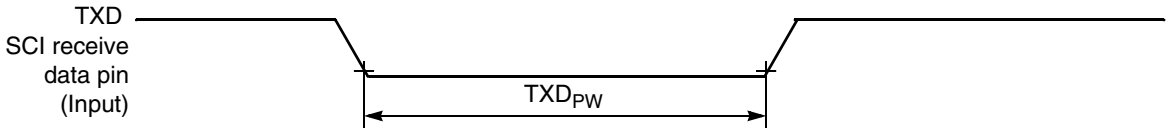


Figure 32. TXD Pulse Width

8.13.3 Inter-Integrated Circuit Interface (I^2C) Timing

Table 31. I^2C Timing

Characteristic	Symbol	Standard Mode		Unit
		Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7	—	µs
Data hold time for I^2C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	ns
Fall time of SDA and SCL signals	t_f	—	300	ns
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	ns

1 The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

2 The maximum $t_{HD;\ DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

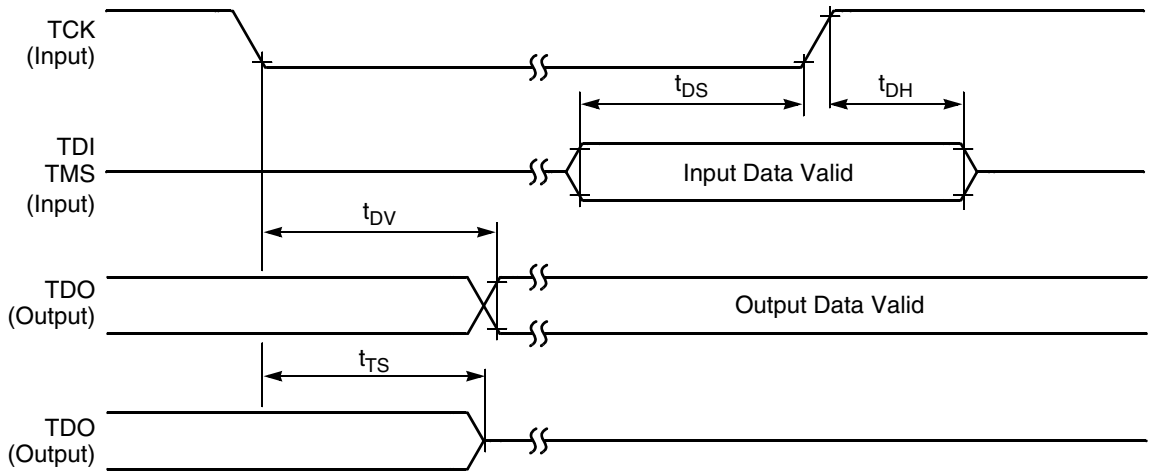


Figure 35. Test Access Port Timing Diagram

8.13.5 Dual Timer Timing

Table 33. Timer Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	Figure 36
Timer input high/low period	P_{INHL}	1T + 3	—	ns	Figure 36
Timer output period	P_{OUT}	125	—	ns	Figure 36
Timer output high/low period	P_{OUTHL}	50	—	ns	Figure 36

1 In the formulas listed, T = the clock cycle. For 32 MHz operation, T = 31.25ns.

2. Parameters listed are guaranteed by design.

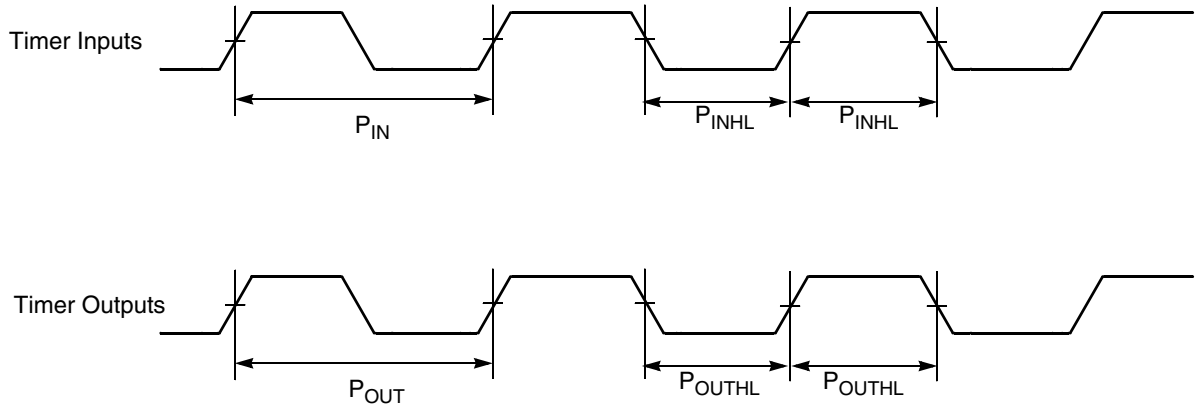


Figure 36. Timer Timing

9 Design Considerations

9.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_A = Ambient temperature for the package (^oC)
$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^oC/W$)
P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 4}$$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = Package junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

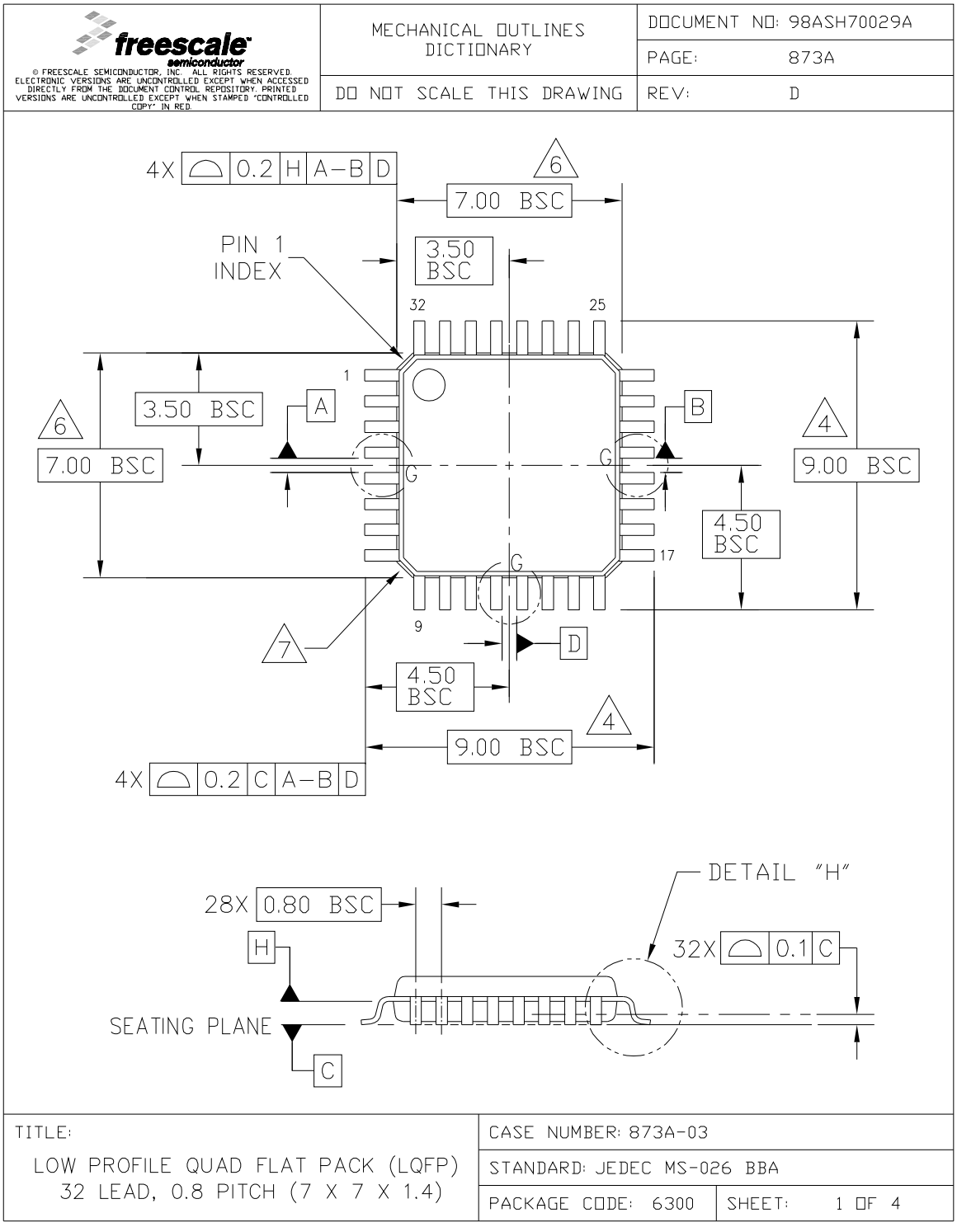
$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 5}$$

where:

T_T = Thermocouple temperature on top of package (^oC)
Ψ_{JT} = Thermal characterization parameter ($^oC/W$)
P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the

10.2 32-pin LQFP



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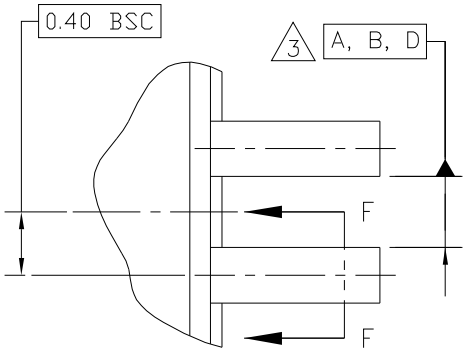
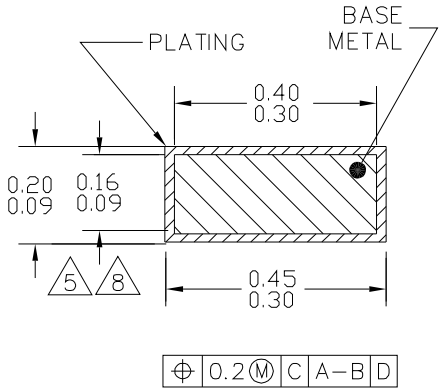
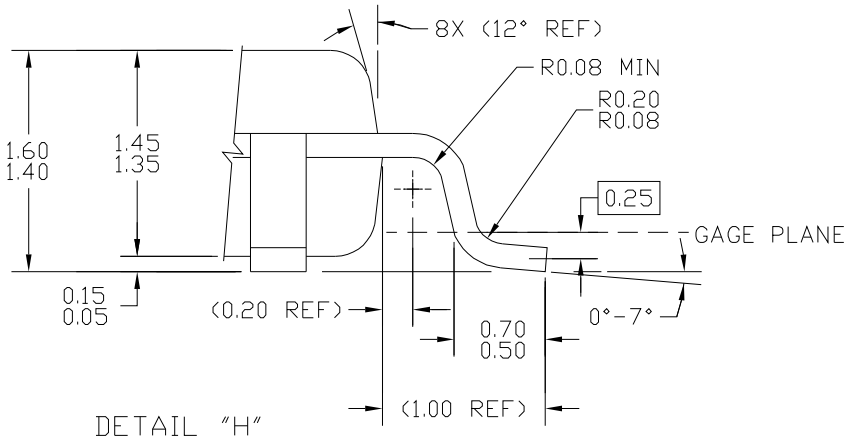


DETAIL G



SECTION F–F
ROTATED 90°CW
32 PLACES



DETAIL "H"

TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	CASE NUMBER: 873A-03
	STANDARD: JEDEC MS-026 BBA
	PACKAGE CODE: 6300 SHEET: 2 OF 4

Table 43. Interrupt Vector Table Contents[1]

Peripheral	Vector Number	User Encoding	Priority Level	Vector Base Address +	Interrupt Function
Core				P:0x00	Reserved for Reset Overlay[2]
Core				P:0x02	Reserved for COP Reset Overlay
Core	2	N/A	3	P:0x04	Illegal Instruction
Core	3	N/A	3	P:0x06	HW Stack Overflow
Core	4	N/A	3	P:0x08	Misaligned Long Word Access
Core	5	N/A	3	P:0x0A	EOnCE Step Counter
Core	6	N/A	3	P:0x0C	EOnCE Breakpoint Unit
Core	7	N/A	3	P:0x0E	EOnCE Trace Buffer
Core	9	N/A	3	P:0x10	EOnCE Transmit Register Empty
Core	9	N/A	3	P:0x12	EOnCE Receive Register Full
PMC	10	0x0A	0	P:0x14	Low-Voltage Detector
PLL	11	0x0B	0	P:0x16	Phase-Locked Loop Loss of Locks and Loss of Clock
ADCA	12	0x0C	0	P:0x18	ADCA Conversion Complete
ADCB	13	0x0D	0	P:0x1A	ADCB Conversion Complete
PWM	14	0x0E	0	P:0x1C	Reload PWM and/or PWM Faults
CMP0	15	0x0F	0	P:0x1E	Comparator 0 Rising/Falling Flag
CMP1	16	0x10	0	P:0x20	Comparator 1 Rising/Falling Flag
CMP2	17	0x11	0	P:0x22	Comparator 2 Rising/Falling Flag
FM	18	0x12	0	P:0x24	Flash Memory Access Status
SPI	19	0x13	0	P:0x26	SPI Receiver Full
SPI	20	0x14	0	P:0x28	SPI Transmitter Empty
SCI	21	0x15	0	P:0x2A	SCI Transmitter Empty/Idle
SCI	22	0x16	0	P:0x2C	SCI Receiver Full/Overrun/Errors
I^2C	23	0x17	0	P:0x2E	I^2C Interrupt
PIT	24	0x18	0	P:0x30	Interval Timer Interrupt
TMR0	25	0x19	0	P:0x32	Dual Timer, Channel 0 Interrupt
TMR1	26	0x1A	0	P:0x34	Dual Timer, Channel 1 Interrupt
GPIOA	27	0x1B	0	P:0x36	GPIOA Interrupt
GPIOB	28	0x1C	0	P:0x38	GPIOB Interrupt
GPIOC	29	0x1D	0	P:0x3A	GPIOC Interrupt
GPIOD	30	0x1E	0	P:0x3C	GPIOD Interrupt
GPIOE	29	0x1F	0	P:0x3E	GPIOE Interrupt
GPIOF	30	0x20	0	P:0x40	GPIOF Interrupt
RTC	33	0x21	0	P:0x42	Real Time Clock

Appendix B
Peripheral Register Memory Map and Reset Value

NOTE

In Table 44, ADC0 stands for ADCA, ADC1 stands for ADCB, and GPIOn is the same as GPIO_n (for example, GPIOA_PUR is the same as GPIO_A_PUR).

Table 44. Detailed Peripheral Memory Map

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
00	0000	TMR0	TMR0_ COMP1	COMPARISON_1															
01	0000	TMR0	TMR0_ COMP2	COMPARISON_2															
02	0000	TMR0	TMR0_ CAPT	CAPTURE															
03	0000	TMR0	TMR0_ LOAD	LOAD															
04	0000	TMR0	TMR0_ HOLD	HOLD															
05	0000	TMR0	TMR0_ CNTR	COUNTER															
06	0000	TMR0	TMR0_ CTRL	CM			PCS				SCS		ONCE	LENGTH	DIR	Co_INIT	OM		
07	0000	TMR0	TMR0_ SCTRL	TCF	TCFIE	TOF	TOFIE	IEF	IEFIE	IPS	INPUT	CAPTURE_ MODE		MSTR	EEOF	VAL	FORCE	OPS	OEN
08	0000	TMR0	TMR0_ CMPLD1	COMPARATOR_LOAD_1															
09	0000	TMR0	TMR0_ CMPLD2	COMPARATOR_LOAD_2															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
1A	0000	TMR1	TMR1_ CSCTRL	DBG_EN		FAULT	ALT_LOAD	0	0	0	0	TCF2EN	TCF1EN	TCF2	TCF1	CL2		CL1	
1B	0000	TMR1	TMR1_ FILT	0	0	0	0	0	FILT_CNT			FILT_PER							
1C–1F	—	TMR1	Reserved	RESERVED															
20	0000	PWM	PWM_ CTRL	LDFQ				HALF	IPOL2	IPOL1	IPOL0	PRSC		PWMRIE	PWMF	ISENS		LDOK	PWMEN
21	0000	PWM	PWM_ FCTRL	0	0	0	0	FPOL3	FPOL2	FPOL1	FPOL0	FIE3	FMODE3	FIE2	FMODE2	FIE1	FMODE1	FIE0	FMODE0
22	0000	PWM	PWM_ FLTACK	FPIN3	FFLAG3	FPIN2	FFLAG2	FPIN1	FFLAG1	FPIN0	FFLAG0		FTACK3		FTACK2		FTACK1		FTACK0
23	0000	PWM	PWM_ OUT	PAD_EN	0	OUTCTL5	OUTCTL4	OUTCTL3	OUTCTL2	OUTCTL1	OUTCTL0	0	0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
24	0000	PWM	PWM_ CNTR	0	CR														
25	0000	PWM	PWM_ CMOD	0	PWMCM														
26	0000	PWM	PWM_ VAL0	PMVAL															
27	0000	PWM	PWM_ VAL1	PMVAL															
28	0000	PWM	PWM_ VAL2	PMVAL															

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
35	0000	PWM	PWM_ SYNC	SYNC_OUT_EN	SYNC_WINDOW														
36	0000	PWM	PWM_ FFILT0	GSTR0	0	0	0	0	FILT0_CNT			FILT0_PER							
37	0000	PWM	PWM_ FFILT1	GSTR1	0	0	0	0	FILT1_CNT			FILT1_PER							
38	0000	PWM	PWM_ FFILT2	GSTR2	0	0	0	0	FILT2_CNT			FILT2_PER							
39	0000	PWM	PWM_ FFILT3	GSTR3	0	0	0	0	FILT3_CNT			FILT3_PER							
3B–3F	—	PWM	Reserved	RESERVED															
40	0000	INTC	INTC_ ICSR	INT	IPIC		VAB							INT_DIS	ERRF	ETRE	TRBUF	BKPT	STPCNT
41	0000	INTC	INTC_ VBA	0	0	VECTOR_BASE_ADDRESS													
42	0000	INTC	INTC_ IAR0	0	0	USER2						0	0	USER1					
43	0000	INTC	INTC_ IAR1	0	0	USER4						0	0	USER3					
44	0000	INTC	INTC_ IAR2	0	0	USER6						0	0	USER5					
45–5F	—	INTC	Reserved	RESERVED															
60	001F	ADC0	ADC0_ ADCSC1A	0	0	0	0	0	0	0	0	COCO	AIEN	ADCO	ADCH				

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
61	0000	ADC0	ADC0_ ADCSC2	0	0	0	0	0	0	0	0	ADACT	ADTRG	0	0	0	ECC	REFSEL	
62–65	—	ADC0	Reserved	RESERVED															
66	0000	ADC0	ADC0_ ADCCFG	0	0	0	0	0	0	0	0	ADLPC	ADIV		ADLSMP	MODE		ADICLK	
67–69	—	ADC0	Reserved	RESERVED															
6A	001F	ADC0	ADC0_ ADCSC1B	0	0	0	0	0	0	0	0	COCO	AIEN	ADCO	ADCH				
6B	0000	ADC0	ADC0_ ADCRA	0	ADR11	ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	0	0	0
6C	0000	ADC0	ADC0_ ADCRB	0	ADR11	ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	0	0	0
6D–6F	—	ADC0	Reserved	RESERVED															
80	001F	ADC1	ADC1_ ADCSC1A	0	0	0	0	0	0	0	0	COCO	AIEN	ADCO	ADCH				
81	0000	ADC1	ADC1_ ADCSC2	0	0	0	0	0	0	0	0	ADACT	ADTRG	0	0	0	ECC	REFSEL	
82–85	—	ADC1	Reserved	RESERVED															
86	0000	ADC1	ADC1_ ADCCFG	0	0	0	0	0	0	0	0	ADLPC	ADIV		ADLSMP	MODE		ADICLK	
87–89	—	ADC1	Reserved	RESERVED															
8A	001F	ADC1	ADC1_ ADCSC1B	0	0	0	0	0	0	0	0	COCO	AIEN	ADCO	ADCH				

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
8B	0000	ADC1	ADC1_ ADCRA	0	ADR11	ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	0	0	0
8C	0000	ADC1	ADC1_ ADCRB	0	ADR11	ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	0	0	0
8D–8F	—	ADC1	Reserved	RESERVED															
A0	0000	PGA0	PGA0_ CNTL0	0	0	0	0	0	0	0	0	TM	GAINSEL					LP	EN
A1	0002	PGA0	PGA0_ CNTL1	0	0	0	0	0	0	0	0	PPDIS	PARMODE	0	CALMODE		CPD		
A2	000E	PGA0	PGA0_ CNTL2	0	0	0	0	0	0	0	0	0	0	SWTRIG	NUM_CLK_GS			ADIV	
A3	0000	PGA0	PGA0_STS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNNING	STCOMP
A4–BF	—	PGA0	Reserved	RESERVED															
C0	0000	PGA1	PGA1_ CNTL0	0	0	0	0	0	0	0	0	TM	GAINSEL					LP	EN
C1	0002	PGA1	PGA1_ CNTL1	0	0	0	0	0	0	0	0	PPDIS	PARMODE	0	CALMODE		CPD		
C2	000E	PGA1	PGA1_ CNTL2	0	0	0	0	0	0	0	0	0	0	SWTRIG	NUM_CLK_GS			ADIV	

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
C9	—	GPIOC	Reserved	RESERVED															
CA	0000	GPIOC	GPIOC_ RAWDATA	0	0	0	0	0	0	0	0	RAWDATA							
CB	0000	GPIOC	GPIOC_ DRIVE	0	0	0	0	0	0	0	0	DRIVE							
CC	00FF	GPIOC	GPIOC_ IFE	0	0	0	0	0	0	0	0	IFE							
CD	0000	GPIOC	GPIOC_ SLEW	0	0	0	0	0	0	0	0	SLEW							
CE–DF	—	GPIOC	Reserved	RESERVED															
E0	00FF	GPIOD	GPIOD_ PUR	0	0	0	0	0	0	0	0	0	0	0	0	PUR			
E1	0000	GPIOD	GPIOD_DR	0	0	0	0	0	0	0	0	0	0	0	0	DR			
E2	0000	GPIOD	GPIOD_ DDR	0	0	0	0	0	0	0	0	0	0	0	0	DDR			
E3	0080	GPIOD	GPIOD_ PER	0	0	0	0	0	0	0	0	0	0	0	0	PER			
E4	—	GPIOD	Reserved	RESERVED															
E5	0000	GPIOD	GPIOD_ IENR	0	0	0	0	0	0	0	0	0	0	0	0	IENR			
E6	0000	GPIOD	GPIOD_ IPOLR	0	0	0	0	0	0	0	0	0	0	0	0	IPOLR			
E7	0000	GPIOD	GPIOD_ IPR	0	0	0	0	0	0	0	0	0	0	0	0	IPR			
E8	0000	GPIOD	GPIOD_ IESR	0	0	0	0	0	0	0	0	0	0	0	0	IESR			
E9	—	GPIOD	Reserved	RESERVED															
EA	0000	GPIOD	GPIOD_ RAWDATA	0	0	0	0	0	0	0	0	0	0	0	0	RAWDATA			

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
02	0000	PDB	PDB_ DELAYB	DELAYB															
03	FFFF	PDB	PDB_MOD	MOD															
04	FFFF	PDB	PDB_ COUNT	COUNT															
05–1F	—	PDB	Reserved	RESERVED															
20	0000	RTC	RTC_SC	0	0	0	0	0	0	0	0	RTIF	RTCLKS		RTIE	RTCPS			
21	0000	RTC	RTC_CNT	0	0	0	0	0	0	0	0	RTCCNT							
22	0000	RTC	RTC_MOD	0	0	0	0	0	0	0	0	RTCMOD							
23–FF	—	RTC	Reserved	RESERVED															
00	0000	HFM	FM_ CLKDIV	0	0	0	0	0	0	0	0	DIVLD	PRDIV8	DIV					
01	0000	HFM	FM_CNFG	0	0	0	0	0	LOCK	0	AEIE	CBEIE	CCIE	KEYACC	0	0	0	LBTS	BTS
03	-000[3]	HFM	FM_SECHI	KEYEN	SECSTAT	0	0	0	0	0	0	0	0	0	0	0	0	0	0
04	0000	HFM	FM_ SECLO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SEC	
06–0F	—	HFM	Reserved	RESERVED															
10	FFFF[6]	HFM	FM_PROT	PROTECT															
11	—	HFM	Reserved	RESERVED															
13	00C0	HFM	FM_USTAT	0	0	0	0	0	0	0	0	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
14	0000	HFM	FM_CMD	0	0	0	0	0	0	0	0	0	CMD						

Table 44. Detailed Peripheral Memory Map (continued)

Offset Addr. (Hex)	Reset Value (Hex)	Periph.	Register	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
17	—	HFM	Reserved	RESERVED															
18	0000	HFM	FM_DATA	FMDATA															
19	—	HFM	Reserved	RESERVED															
1A	FFFF[4]	HFM	FM_OPT0	IFR_OPT0															
1B	FFFF[5]	HFM	FM_OPT1	IFR_OPT1															
1D	FFFF[6]	HFM	FM_ TSTSIG	TST_AREA_SIG															
1E–3F	—	HFM	Reserved	RESERVED															

1 The binary reset value of this register is 0000 0000 0UUU UUUU, where U represents an undefined value. Spaces have been added to the value for clarity.

2 The binary reset value of this register is 0000 0000 111NC NC NC NC NC. Spaces have been added to the value for clarity.

3 The binary reset value of this register is FS00 0000 0000 0000, where F indicates that the reset state is loaded from the flash array during reset, and where S indicates that the reset state is determined by the security state of the module. Spaces have been added to the value for clarity.

4 The reset state is loaded from the flash array during reset.

5 The reset state is loaded from the flash array during reset.

6 The reset state is loaded from the flash array during reset.