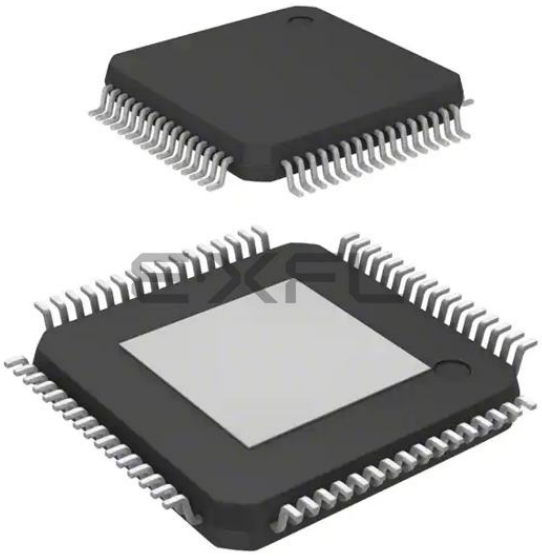
Infineon Technologies - XC2734X40F80LAAKXUMA1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-64-6
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2734x40f80laakxuma1

XC2734X Data Sheet
Revision History: V1.5 2013-02

Previous Versions:
V1.4, 2011-07
V1.3, 2010-04
V1.2, 2009-07
V1.1, 2009-07
V1.0, 2009-03 Preliminary

Page	Subjects (major changes since last revision)
25	Added AB step marking.
75	Errata SWD_X.P002 implemented: V_{SWD} tolerance boundaries for 5.5 V are changed.
77	Clarified “Coding of bit fields LEVxV” descriptions. Matched with Operating Conditions: marked some coding values “out of valid operation range”.
78	Errata FLASH_X.P001 implemented: Test Condition for Flash parameter N_{ER} corrected

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Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
7	P6.0	O0 / I	DA/A	**Bit 0 of Port 6, General Purpose Input/Output**
	EMUX0	O1	DA/A	**External Analog MUX Control Output 0 (ADC0)**
	$\overline{\text{BRKOUT}}$	O3	DA/A	**OCDS Break Signal Output**
	ADCx_REQGTyG	I	DA/A	**External Request Gate Input for ADC0/1**
	U1C1_DX0E	I	DA/A	**USIC1 Channel 1 Shift Data Input**
8	P6.1	O0 / I	DA/A	**Bit 1 of Port 6, General Purpose Input/Output**
	EMUX1	O1	DA/A	**External Analog MUX Control Output 1 (ADC0)**
	T3OUT	O2	DA/A	**GPT12E Timer T3 Toggle Latch Output**
	U1C1_DOUT	O3	DA/A	**USIC1 Channel 1 Shift Data Output**
	ADCx_REQTRyE	I	DA/A	**External Request Trigger Input for ADC0/1**
	ESR1_6	I	DA/A	**ESR1 Trigger Input 6**
10	P15.0	I	In/A	**Bit 0 of Port 15, General Purpose Input**
	ADC1_CH0	I	In/A	**Analog Input Channel 0 for ADC1**
11	P15.4	I	In/A	**Bit 4 of Port 15, General Purpose Input**
	ADC1_CH4	I	In/A	**Analog Input Channel 4 for ADC1**
	T6INA	I	In/A	**GPT12E Timer T6 Count/Gate Input**
12	V_{AREF}	-	PS/A	**Reference Voltage for A/D Converters ADC0/1**
13	V_{AGND}	-	PS/A	**Reference Ground for A/D Converters ADC0/1**
14	P5.0	I	In/A	**Bit 0 of Port 5, General Purpose Input**
	ADC0_CH0	I	In/A	**Analog Input Channel 0 for ADC0**
15	P5.2	I	In/A	**Bit 2 of Port 5, General Purpose Input**
	ADC0_CH2	I	In/A	**Analog Input Channel 2 for ADC0**
	TDI_A	I	In/A	**JTAG Test Data Input**
19	P5.4	I	In/A	**Bit 4 of Port 5, General Purpose Input**
	ADC0_CH4	I	In/A	**Analog Input Channel 4 for ADC0**
	T3EUDA	I	In/A	**GPT12E Timer T3 External Up/Down Control Input**
	TMS_A	I	In/A	**JTAG Test Mode Selection Input**

3 Functional Description

The architecture of the XC2734X combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources. This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XC2734X.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XC2734X.

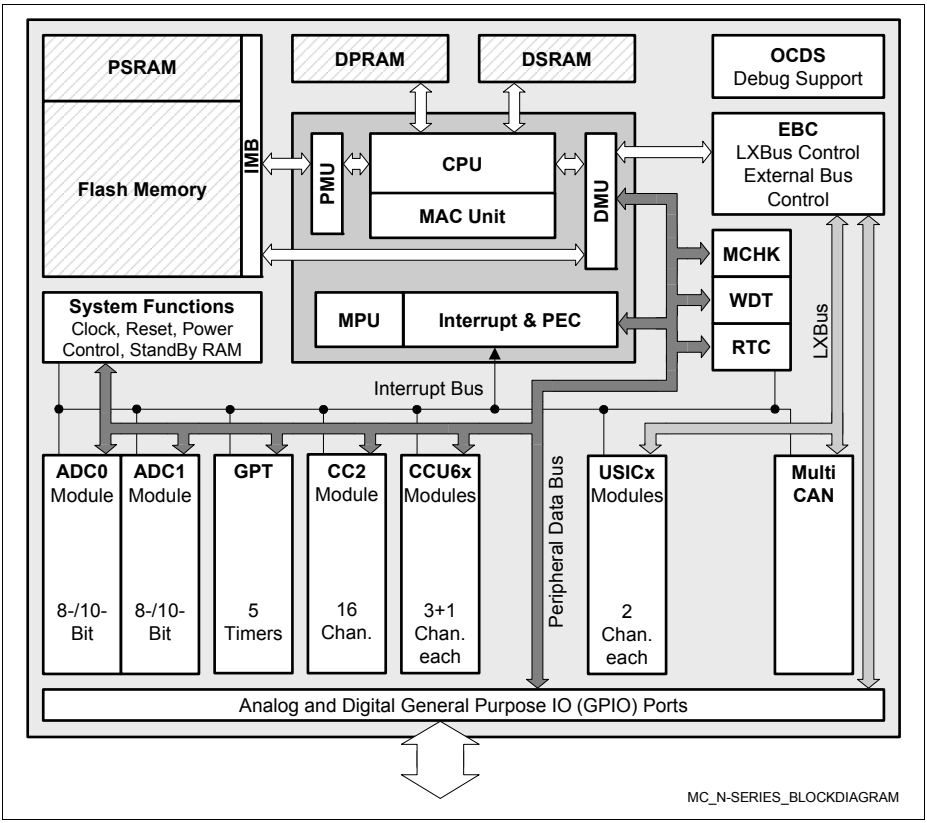

Figure 4 Block Diagram

Table 7 XC2734X Memory Map (cont'd)[1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
Reserved for DSRAM	$00'8000_H$	$00'9FFF_H$	8 Kbytes	
External memory area	$00'0000_H$	$00'7FFF_H$	32 Kbytes	

1) Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.

2) The areas marked with "<" are slightly smaller than indicated, see column "Notes".

3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

4) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

Up to 16 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

Note: The actual size of the PSRAM depends on the quoted device type.

The timing in the AC Characteristics refers to TCSs. Timing must be calculated using the minimum TCS possible under the given circumstances.
The actual minimum value for TCS depends on the jitter of the PLL. Because the PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or oscillator), the accumulated jitter is limited. This means that the relative deviation for periods of more than one TCS is lower than for a single TCS (see formulas and **Figure 20**).

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler K2 to generate the system clock signal f_{SYS}. The number of VCO cycles is K2 u**T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

The maximum accumulated jitter (long-term jitter) D_{Tmax} is defined by:

D_{Tmax} [ns] = r(220 / (K2 uf_{SYS}) + 4.3)

This maximum value is applicable, if either the number of clock cycles T > (f_{SYS} / 1.2) or the prescaler value K2 > 17.

In all other cases for a timeframe of **T** uTCS the accumulated jitter D_T is determined by:

D_T [ns] = D_{Tmax} u[(1 - 0.058 uK2) u(T - 1) / (0.83 uf_{SYS} - 1) + 0.058 uK2]

f_{SYS} in [MHz] in all formulas.

Example, for a period of 3 TCSs @ 33 MHz and K2 = 4:

D_{max} = r(220 / (4 u33) + 4.3) = 5.97 ns (Not applicable directly in this case!)

D_3 = 5.97 u[(1 - 0.058 u4) u(3 - 1) / (0.83 u33 - 1) + 0.058 u4]
= 5.97 u[0.768 u2 / 26.39 + 0.232]
= 1.7 ns

Example, for a period of 3 TCSs @ 33 MHz and K2 = 2:

D_{max} = r(220 / (2 u33) + 4.3) = 7.63 ns (Not applicable directly in this case!)

D_3 = 7.63 u[(1 - 0.058 u2) u(3 - 1) / (0.83 u33 - 1) + 0.058 u2]
= 7.63 u[0.884 u2 / 26.39 + 0.116]
= 1.4 ns

4.7.4 Pad Properties

The output pad drivers of the XC2734X can operate in several user-selectable modes. Strong driver mode allows controlling external components requiring higher currents such as power bridges or LEDs. Reducing the driving power of an output pad reduces electromagnetic emissions (EME). In strong driver mode, selecting a slower edge reduces EME.

The dynamic behavior, i.e. the rise time and fall time, depends on the applied external capacitance that must be charged and discharged. Timing values are given for a capacitance of 20 pF, unless otherwise noted.

In general, the performance of a pad driver depends on the available supply voltage V_{DDP}. Therefore the following tables list the pad parameters for the upper voltage range and the lower voltage range, respectively.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 27 is valid under the following conditions: V_{DDP} d5.5 V; V_{DDP}typ. 5 V; V_{DDP} t 4.5 V

Table 27 Standard Pad Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value)[1)]	I_{Omax} CC			4.0	mA	Driver_Strength = Medium
				10	mA	Driver_Strength = Strong
				0.5	mA	Driver_Strength = Weak
Nominal output driver current (absolute value)	I_{Onom} CC			1.0	mA	Driver_Strength = Medium
				2.5	mA	Driver_Strength = Strong
				0.1	mA	Driver_Strength = Weak

Table 27 Standard Pad Parameters for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC			23 + 0.6 x C_L	ns	C_L t 20 pF; C_L d100 pF; Driver_Strength = Medium
				11.6 + 0.22 x C_L	ns	C_L t 20 pF; C_L d100 pF; Driver_Strength = Strong ; Driver_Edge= Medium
				4.2 + 0.14 x C_L	ns	C_L t 20 pF; C_L d100 pF; Driver_Strength = Strong ; Driver_Edge= Sharp
				20.6 + 0.22 x C_L	ns	C_L t 20 pF; C_L d100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
				212 + 1.9 x C_L	ns	C_L t 20 pF; C_L d100 pF; Driver_Strength = Weak

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΘI_{OL} and ΘI_{OH}) must remain below 50 mA.