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Details

Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	CANbus, SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 2x16b, 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f061-gqr

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Table 1.1. Product Selection Guide

	MIPS (Peak)	Flash Memory	RAM	External Memory Interface	SMBus/I2C and SPI	CAN	UARTS	Timers (16-bit)	Programmable Counter Array	Digital Port I/O's	16-bit 1 Msps ADC Typical INL (LSBs)	10-bit 200 ksps ADC Inputs	Voltage Reference	Temperature Sensor	DAC Resolution (bits)	DAC Outputs	Analog Comparators	Package
C8051F060	25	64 k	4352	✓	✓	✓	2	5	✓	59	±0.75	8	✓	✓	12	2	3	100 TQFP
C8051F061	25	64 k	4352	-	✓	✓	2	5	✓	24	±0.75	8	✓	✓	12	2	3	64 TQFP
C8051F062	25	64 k	4352	✓	✓	✓	2	5	✓	59	±1.5	8	✓	✓	12	2	3	100 TQFP
C8051F063	25	64 k	4352	-	✓	✓	2	5	✓	24	±1.5	8	✓	✓	12	2	3	64 TQFP
C8051F064	25	64 k	4352	✓	✓	-	2	5	✓	59	±0.75	-	✓	-	-	-	3	100 TQFP
C8051F065	25	64 k	4352	-	✓	-	2	5	✓	24	±0.75	-	✓	-	-	-	3	64 TQFP
C8051F066	25	32 k	4352	✓	✓	-	2	5	✓	59	±0.75	-	✓	-	-	-	3	100 TQFP
C8051F067	25	32 k	4352	-	✓	-	2	5	✓	24	±0.75	-	✓	-	-	-	3	64 TQFP

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1.9. 10-Bit Analog to Digital Converter

The C8051F060/1/2/3 devices have an on-board 10-bit SAR ADC (ADC2) with a 9-channel input multiplexer and programmable gain amplifier. This ADC features a 200 kps maximum throughput and true 10-bit performance with an INL of ± 1 LSB. Eight input pins are available for measurement and can be programmed as single-ended or differential inputs. Additionally, the on-chip temperature sensor can be used as an input to the ADC. The ADC is under full control of the CIP-51 microcontroller via the Special Function Registers. The ADC2 voltage reference is selected between the analog power supply (AV+) and the external VREF2 pin. User software may put ADC2 into shutdown mode to save power.

A flexible conversion scheduling system allows ADC2 conversions to be initiated by software commands, timer overflows, or an external input signal. Conversion completions are indicated by a status bit and an interrupt (if enabled), and the resulting 10-bit data word is latched into two SFR locations upon completion.

ADC2 also contains Window Compare registers, which can be configured to interrupt the controller when ADC2 data is within or outside of a specified range. ADC2 can monitor a key voltage continuously in background mode, and not interrupt the controller unless the converted data is within the specified window.

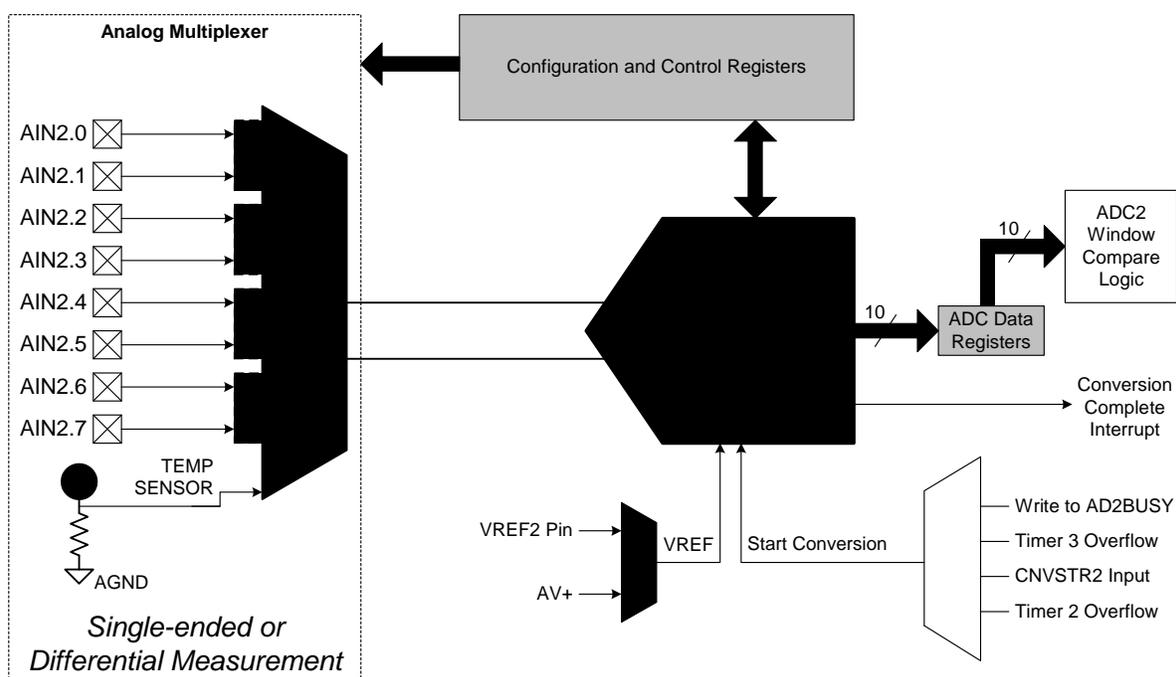


Figure 1.13. 10-Bit ADC Diagram

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7.1. Analog Multiplexer

The analog multiplexer (AMUX2) selects the inputs to the ADC, allowing any of the pins on Port 1 to be measured in single-ended mode, or as a differential pair. Additionally, the on-chip temperature sensor may be selected as a single-ended input. The ADC2 input channels are configured and selected in the AMX2CF and AMX2SL registers as described in Figure 7.5 and Figure 7.6, respectively. In Single-ended Mode, the selected pin is measured with respect to AGND. In Differential Mode, the selected differential pair is measured with respect to one another. The polarity of the differential measurement depends on the setting of the AMX2AD3-0 bits in the AMX2SL register. For example, if pins AIN2.0 and AIN2.1 are configured for differential measurement ($AIN01IC = 1$), and $AMX2AD3-0 = 0000b$, the ADC will measure the voltage ($AIN2.0 - AIN2.1$). If $AMX2AD3-0$ is changed to $0001b$, the ADC will measure the same voltage, with opposite polarity ($AIN2.1 - AIN2.0$).

The conversion code format differs between Single-ended and Differential modes. The registers ADC2H and ADC2L contain the high and low bytes of the output conversion code from the ADC at the completion of each conversion. Data can be right-justified or left-justified, depending on the setting of the AD2LJST bit (ADC2CN.0). When in Single-ended Mode, conversion codes are represented as 10-bit unsigned integers. Inputs are measured from '0' to $VREF * 1023/1024$. Example codes are shown below for both right-justified and left-justified data. Unused bits in the ADC2H and ADC2L registers are set to '0'.

Input Voltage	Right-Justified ADC2H:ADC2L (AD2LJST = 0)	Left-Justified ADC2H:ADC2L (AD2LJST = 1)
$VREF * 1023/1024$	0x03FF	0xFFC0
$VREF * 512/1024$	0x0200	0x8000
$VREF * 256/1024$	0x0100	0x4000
0	0x0000	0x0000

When in Differential Mode, conversion codes are represented as 10-bit signed 2's complement numbers. Inputs are measured from $-VREF$ to $VREF * 511/512$. Example codes are shown below for both right-justified and left-justified data. For right-justified data, the unused MSBs of ADC2H are a sign-extension of the data word. For left-justified data, the unused LSBs in the ADC2L register are set to '0'.

Input Voltage	Right-Justified ADC2H:ADC2L (AD2LJST = 0)	Left-Justified ADC2H:ADC2L (AD2LJST = 1)
$VREF * 511/512$	0x01FF	0x7FC0
$VREF * 256/512$	0x0100	0x4000
0	0x0000	0x0000
$-VREF * 256/512$	0xFF00	0xC000
$-VREF$	0xFE00	0x8000

Important Note About ADC2 Input Configuration: Port 1 pins selected as ADC2 inputs should be configured as analog inputs. To configure a Port 1 pin for analog input, set to '1' the corresponding bit in register P1MDIN. Port 1 pins used as ADC2 inputs will be skipped by the crossbar for peripheral assignments. See Section "18. Port Input/Output" on page 203 for more Port I/O configuration details.

The Temperature Sensor transfer function is shown in Figure 7.2 on Page 89. The output voltage (V_{TEMP}) is a single-ended input to ADC2 when the Temperature Sensor is selected by bits AMX2AD3-0 in register AMX2SL. Typical values for the Slope and Offset parameters can be found in Table 7.1.

Table 8.1. DAC Electrical Characteristics

VDD = 3.0 V, AV+ = 3.0 V, VREF = 2.40 V (REFBE = 0), No Output Load unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Static Performance					
Resolution			12		bits
Integral Nonlinearity			±1.5		LSB
Differential Nonlinearity				±1	LSB
Output Noise	No Output Filter 100 kHz Output Filter 10 kHz Output Filter		250 128 41		μVrms
Offset Error	Data Word = 0x014		±3	±30	mV
Offset Tempco			6		ppm/°C
Full-Scale Error			±20	±60	mV
Full-Scale Error Tempco			10		ppm/°C
VDD Power Supply Rejection Ratio			-60		dB
Output Impedance in Shutdown Mode	DACnEN = 0		100		kΩ
Output Sink Current			300		μA
Output Short-Circuit Current	Data Word = 0xFFFF		15		mA
Dynamic Performance					
Voltage Output Slew Rate	Load = 40pF		0.44		V/μs
Output Settling Time to 1/2 LSB	Load = 40pF, Output swing from code 0xFFFF to 0x014		10		μs
Output Voltage Swing		0		VREF-1LSB	V
Startup Time			10		μs
Analog Outputs					
Load Regulation	I _L = 0.01mA to 0.3mA at code 0xFFFF		60		ppm
Power Consumption (each DAC)					
Power Supply Current (AV+ supplied to DAC)	Data Word = 0x7FF		300	500	μA

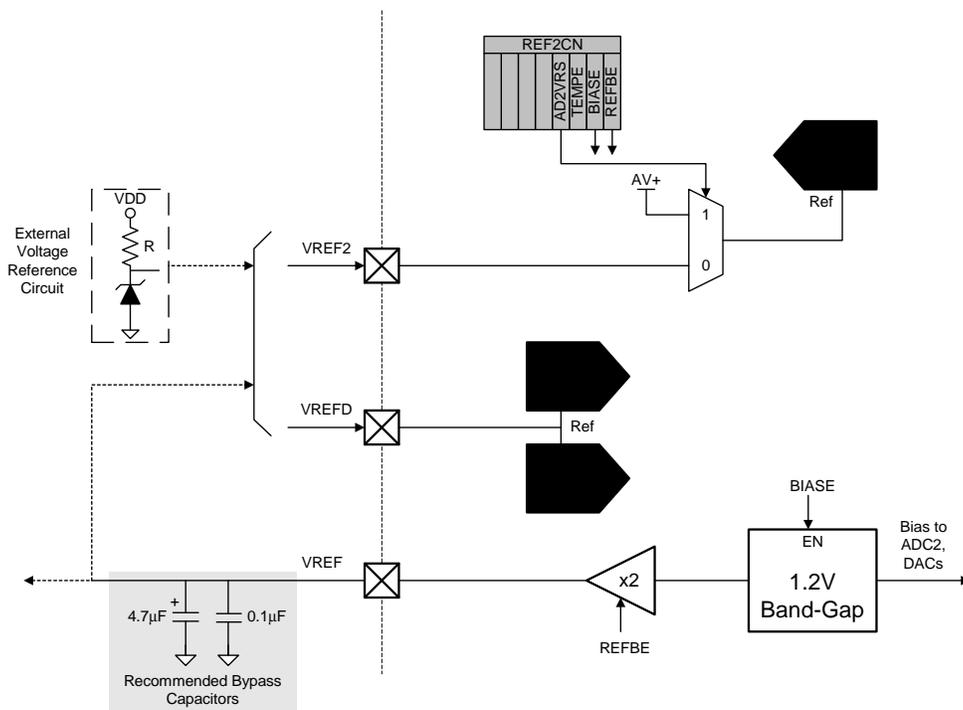
9. Voltage Reference 2 (C8051F060/2)

The voltage reference circuitry offers full flexibility in operating the ADC2 and DAC modules. Two voltage reference input pins allow ADC2 and the two DACs to reference an external voltage reference or the on-chip voltage reference output. ADC2 may also reference the analog power supply voltage, via the VREF multiplexer shown in Figure 9.1.

The internal voltage reference circuit consists of a 1.2 V, temperature stable bandgap voltage reference generator and a gain-of-two output buffer amplifier. The internal reference may be routed via the VREF pin to external system components or to the voltage reference input pins shown in Figure 9.1. The maximum load seen by the VREF pin must be less than 200 μ A to AGND. Bypass capacitors of 0.1 μ F and 4.7 μ F are recommended from the VREF pin to AGND, as shown in Figure 9.1.

The Reference Control Register 2, REF2CN (defined in Figure 9.2) enables/disables the internal reference generator and selects the reference input for ADC2. The BIASE bit in REF2CN enables the on-board reference generator while the REFBE bit enables the gain-of-two buffer amplifier which drives the VREF pin. When disabled, the supply current drawn by the bandgap and buffer amplifier falls to less than 1 μ A (typical) and the output of the buffer amplifier enters a high impedance state. If the internal bandgap is used as the reference voltage generator, BIASE and REFBE must both be set to logic 1. If the internal reference is not used, REFBE may be set to logic 0. Note that the BIASE bit must be set to logic 1 if ADC2 or either DAC is used, regardless of the voltage reference used. If neither ADC2 nor the DACs are being used, both of these bits can be set to logic 0 to conserve power. Bit AD2VRS selects between VREF2 and AV+ for the ADC2 voltage reference source. The electrical specifications for the Voltage Reference are given in Table 9.1.

Figure 9.1. Voltage Reference Functional Block Diagram



Comparator interrupts can be generated on either rising-edge and falling-edge output transitions. (For Interrupt enable and priority control, see Section “13.3. Interrupt Handler” on page 151). The rising and/or falling -edge interrupts are enabled using the comparator’s Rising/Falling Edge Interrupt Enable Bits (CPnRIE and CPnFIE) in their respective Comparator Mode Selection Register (CPTnMD), shown in Figure 12.4. These bits allow the user to control which edge (or both) will cause a comparator interrupt. However, the comparator interrupt must also be enabled in the Extended Interrupt Enable Register (EIE1). The CPnFIF flag is set to logic 1 upon a Comparator falling-edge interrupt, and the CPnRIF flag is set to logic 1 upon the Comparator rising-edge interrupt. Once set, these bits remain set until cleared by software. The output state of a Comparator can be obtained at any time by reading the CPnOUT bit. A Comparator is enabled by setting its respective CPnEN bit to logic 1, and is disabled by clearing this bit to logic 0. Upon enabling a comparator, the output of the comparator is not immediately valid. Before using a comparator as an interrupt or reset source, software should wait for a minimum of the specified “Power-up time” as specified in Table 12.1, “Comparator Electrical Characteristics,” on page 122.

12.1. Comparator Inputs

The Port pins selected as comparator inputs should be configured as analog inputs in the Port 2 Input Configuration Register (for details on Port configuration, see Section “18.1.3. Configuring Port Pins as Digital Inputs” on page 207). The inputs for Comparator are on Port 2 as follows:

Comparator Input	Port PIN
CP0 +	P2.6
CP0 -	P2.7
CP1 +	P2.2
CP1 -	P2.3
CP2 +	P2.4
CP2 -	P2.5

13.2.2. Data Memory

The CIP-51 implements 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFRs) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing above 0x7F will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 13.2 illustrates the data memory organization of the CIP-51.

13.2.3. General Purpose Registers

The lower 32 bytes of data memory, locations 0x00 through 0x1F, may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word, RS0 (PSW.3) and RS1 (PSW.4), select the active register bank (see description of the PSW in Figure 13.16). This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

13.2.4. Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit 7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (a bit source or destination operand as opposed to a byte source or destination).

The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction:

```
MOV    C, 22.3h
```

moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

13.2.5. Stack

A programmer's stack can be located anywhere in the 256 byte data memory. The stack area is designated using the Stack Pointer (SP, address 0x81) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07; therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

The MCUs also have built-in hardware for a stack record which is accessed by the debug logic. The stack record is a 32-bit shift register, where each PUSH or increment SP pushes one record bit onto the register,

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Figure 13.17. ACC: Accumulator

R/W	Reset Value							
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable
								SFR Address: 0xE0
								SFR Page: All Pages

Bits7-0: ACC: Accumulator.
This register is the accumulator for arithmetic operations.

Figure 13.18. B: B Register

R/W	Reset Value							
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable
								SFR Address: 0xF0
								SFR Page: All Pages

Bits7-0: B: B Register.
This register serves as a second accumulator for certain arithmetic operations.

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Figure 16.4. FLSCL: Flash Memory Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
FOSE	FRAE	Reserved	Reserved	Reserved	Reserved	Reserved	FLWE	10000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
								SFR Address: 0xB7
								SFR Page: 0
Bit 7:	FOSE: Flash One-Shot Timer Enable This is the timer that turns off the sense amps after a Flash read. 0: Flash One-Shot Timer disabled. 1: Flash One-Shot Timer enabled (recommended setting.)							
Bit 6:	FRAE: Flash Read Always Enable 0: Flash reads occur as necessary (recommended setting.). 1: Flash reads occur every system clock cycle.							
Bits 5-1:	RESERVED. Read = 00000b. Must Write 00000b.							
Bit 0:	FLWE: Flash Write/Erase Enable This bit must be set to allow Flash writes/erases from user software. 0: Flash writes/erases disabled. 1: Flash writes/erases enabled.							

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17.6. Timing

The timing parameters of the External Memory Interface can be configured to enable connection to devices having different setup and hold time requirements. The Address Setup time, Address Hold time, /RD and /WR strobe widths, and in multiplexed mode, the width of the ALE pulse are all programmable in units of SYSCLK periods through EMI0TC, shown in Figure 17.6, and EMI0CF[1:0].

The timing for an off-chip MOVX instruction can be calculated by adding 4 SYSCLK cycles to the timing parameters defined by the EMI0TC register. Assuming non-multiplexed operation, the minimum execution time for an off-chip XRAM operation is 5 SYSCLK cycles (1 SYSCLK for /RD or /WR pulse + 4 SYSCLKs). For multiplexed operations, the Address Latch Enable signal will require a minimum of 2 additional SYSCLK cycles. Therefore, the minimum execution time for an off-chip XRAM operation in multiplexed mode is 7 SYSCLK cycles (2 for /ALE + 1 for /RD or /WR + 4). The programmable setup and hold times default to the maximum delay settings after a reset.

Figure 17.6. EMI0TC: External Memory Timing Control

R/W	Reset Value							
EAS1	EAS0	ERW3	EWR2	EWR1	EWR0	EAH1	EAH0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA1
SFR Page: 0

Bits7-6: EAS1-0: EMIF Address Setup Time Bits.
 00: Address setup time = 0 SYSCLK cycles.
 01: Address setup time = 1 SYSCLK cycle.
 10: Address setup time = 2 SYSCLK cycles.
 11: Address setup time = 3 SYSCLK cycles.

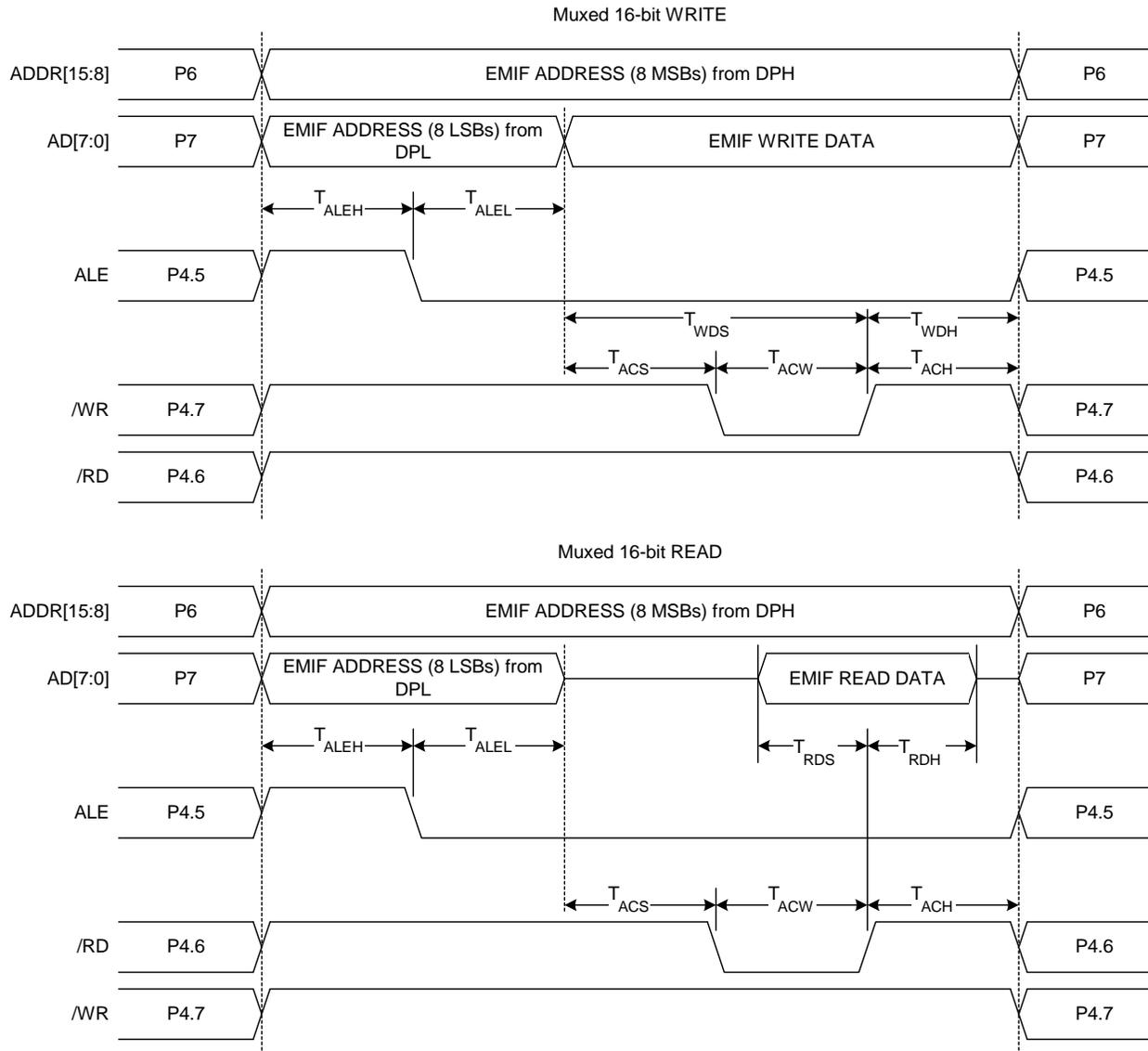
Bits5-2: EWR3-0: EMIF /WR and /RD Pulse-Width Control Bits.
 0000: /WR and /RD pulse width = 1 SYSCLK cycle.
 0001: /WR and /RD pulse width = 2 SYSCLK cycles.
 0010: /WR and /RD pulse width = 3 SYSCLK cycles.
 0011: /WR and /RD pulse width = 4 SYSCLK cycles.
 0100: /WR and /RD pulse width = 5 SYSCLK cycles.
 0101: /WR and /RD pulse width = 6 SYSCLK cycles.
 0110: /WR and /RD pulse width = 7 SYSCLK cycles.
 0111: /WR and /RD pulse width = 8 SYSCLK cycles.
 1000: /WR and /RD pulse width = 9 SYSCLK cycles.
 1001: /WR and /RD pulse width = 10 SYSCLK cycles.
 1010: /WR and /RD pulse width = 11 SYSCLK cycles.
 1011: /WR and /RD pulse width = 12 SYSCLK cycles.
 1100: /WR and /RD pulse width = 13 SYSCLK cycles.
 1101: /WR and /RD pulse width = 14 SYSCLK cycles.
 1110: /WR and /RD pulse width = 15 SYSCLK cycles.
 1111: /WR and /RD pulse width = 16 SYSCLK cycles.

Bits1-0: EAH1-0: EMIF Address Hold Time Bits.
 00: Address hold time = 0 SYSCLK cycles.
 01: Address hold time = 1 SYSCLK cycle.
 10: Address hold time = 2 SYSCLK cycles.
 11: Address hold time = 3 SYSCLK cycles.

17.6.2. Multiplexed Mode

17.6.2.1. 16-bit MOVX: EMI0CF[4:2] = '001', '010', or '011'.

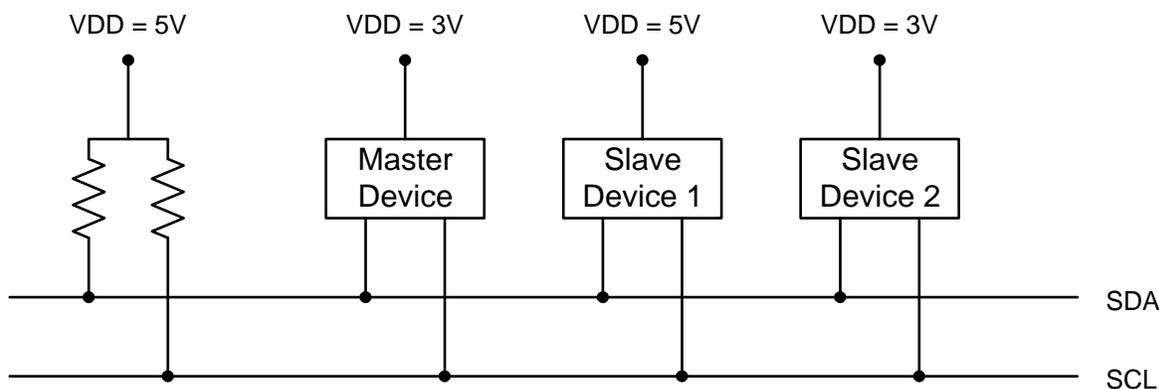
Figure 17.10. Multiplexed 16-bit MOVX Timing



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Figure 20.2 shows a typical SMBus configuration. The SMBus0 interface will work at any voltage between 3.0 V and 5.0 V and different devices on the bus may operate at different voltage levels. The bi-directional SCL (serial clock) and SDA (serial data) lines must be connected to a positive power supply voltage through a pull-up resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines, so that both are pulled high when the bus is free. The maximum number of devices on the bus is limited only by the requirement that the rise and fall times on the bus will not exceed 300 ns and 1000 ns, respectively.

Figure 20.2. Typical SMBus Configuration



20.1. Supporting Documents

It is assumed the reader is familiar with or has access to the following supporting documents:

1. The I2C-bus and how to use it (including specifications), Philips Semiconductor.
2. The I2C-Bus Specification -- Version 2.0, Philips Semiconductor.
3. System Management Bus Specification -- Version 1.1, SBS Implementers Forum.

20.2. SMBus Protocol

Two types of data transfers are possible: data transfers from a master transmitter to an addressed slave receiver (WRITE), and data transfers from an addressed slave transmitter to a master receiver (READ). The master device initiates both types of data transfers and provides the serial clock pulses on SCL. Note: multiple master devices on the same bus are supported. If two or more masters attempt to initiate a data transfer simultaneously, an arbitration scheme is employed with a single master always winning the arbitration. Note that it is not necessary to specify one device as the master in a system; any device who transmits a START and a slave address becomes the master for that transfer.

A typical SMBus transaction consists of a START condition followed by an address byte (Bits7-1: 7-bit slave address; Bit0: R/W direction bit), one or more bytes of data, and a STOP condition. Each byte that is received (by a master or slave) must be acknowledged (ACK) with a low SDA during a high SCL (see Figure 20.3). If the receiving device does not ACK, the transmitting device will read a "not acknowledged" (NACK), which is a high SDA during a high SCL.

20.4. SMBus Special Function Registers

The SMBus0 serial interface is accessed and controlled through five SFRs: SMB0CN Control Register, SMB0CR Clock Rate Register, SMB0ADR Address Register, SMB0DAT Data Register and SMB0STA Status Register. The five special function registers related to the operation of the SMBus0 interface are described in the following sections.

20.4.1. Control Register

The SMBus0 Control register SMB0CN is used to configure and control the SMBus0 interface. All of the bits in the register can be read or written by software. Two of the control bits are also affected by the SMBus0 hardware. The Serial Interrupt flag (SI, SMB0CN.3) is set to logic 1 by the hardware when a valid serial interrupt condition occurs. It can only be cleared by software. The Stop flag (STO, SMB0CN.4) is set to logic 1 by software. It is cleared to logic 0 by hardware when a STOP condition is detected on the bus.

Setting the ENSMB flag to logic 1 enables the SMBus0 interface. Clearing the ENSMB flag to logic 0 disables the SMBus0 interface and removes it from the bus. Momentarily clearing the ENSMB flag and then resetting it to logic 1 will reset SMBus0 communication. However, ENSMB should not be used to temporarily remove a device from the bus since the bus state information will be lost. Instead, the Assert Acknowledge (AA) flag should be used to temporarily remove the device from the bus (see description of AA flag below).

Setting the Start flag (STA, SMB0CN.5) to logic 1 will put SMBus0 in a master mode. If the bus is free, SMBus0 will generate a START condition. If the bus is not free, SMBus0 waits for a STOP condition to free the bus and then generates a START condition after a 5 μ s delay per the SMB0CR value (In accordance with the SMBus protocol, the SMBus0 interface also considers the bus free if the bus is idle for 50 μ s and no STOP condition was recognized). If STA is set to logic 1 while SMBus0 is in master mode and one or more bytes have been transferred, a repeated START condition will be generated.

When the Stop flag (STO, SMB0CN.4) is set to logic 1 while the SMBus0 interface is in master mode, the interface generates a STOP condition. In a slave mode, the STO flag may be used to recover from an error condition. In this case, a STOP condition is not generated on the bus, but the SMBus hardware behaves as if a STOP condition has been received and enters the "not addressed" slave receiver mode. Note that this simulated STOP will not cause the bus to appear free to SMBus0. The bus will remain occupied until a STOP appears on the bus or a Bus Free Timeout occurs. Hardware automatically clears the STO flag to logic 0 when a STOP condition is detected on the bus.

The Serial Interrupt flag (SI, SMB0CN.3) is set to logic 1 by hardware when the SMBus0 interface enters one of 27 possible states. If interrupts are enabled for the SMBus0 interface, an interrupt request is generated when the SI flag is set. The SI flag must be cleared by software.

Important Note: If SI is set to logic 1 while the SCL line is low, the clock-low period of the serial clock will be stretched and the serial transfer is suspended until SI is cleared to logic 0. A high level on SCL is not affected by the setting of the SI flag.

The Assert Acknowledge flag (AA, SMB0CN.2) is used to set the level of the SDA line during the acknowledge clock cycle on the SCL line. Setting the AA flag to logic 1 will cause an ACK (low level on SDA) to be sent during the acknowledge cycle if the device has been addressed. Setting the AA flag to logic 0 will cause a NACK (high level on SDA) to be sent during acknowledge cycle. After the transmission of a byte in slave mode, the slave can be temporarily removed from the bus by clearing the AA flag. The slave's own address and general call address will be ignored. To resume operation on the bus, the AA flag must be reset to logic 1 to allow the slave's address to be recognized.

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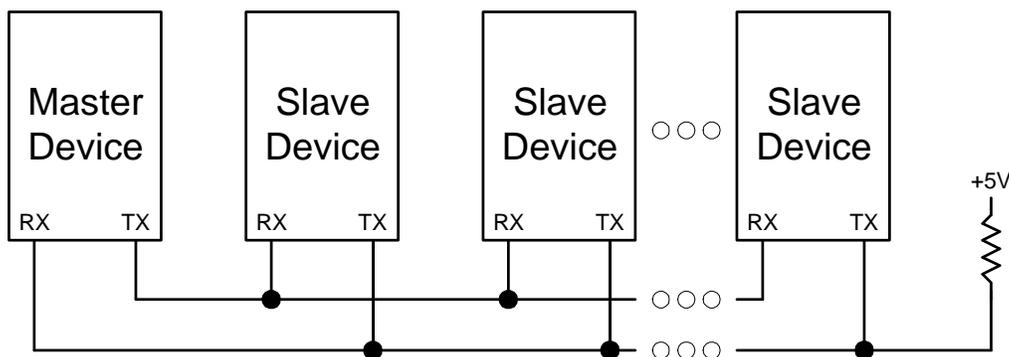
Setting the SMBus0 Free Timer Enable bit (FTE, SMB0CN.1) to logic 1 enables the timer in SMB0CR. When SCL goes high, the timer in SMB0CR counts up. A timer overflow indicates a free bus timeout: if SMBus0 is waiting to generate a START, it will do so after this timeout. The bus free period should be less than 50 μ s (see Figure 20.9, SMBus0 Clock Rate Register).

When the TOE bit in SMB0CN is set to logic 1, Timer 4 is used to detect SCL low timeouts. If Timer 4 is enabled (see Section “24.2. Timer 2, Timer 3, and Timer 4” on page 295), Timer 4 is forced to reload when SCL is high, and forced to count when SCL is low. With Timer 4 enabled and configured to overflow after

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address as valid. If a master were to then send an address of “11111111”, all three slave devices would recognize the address as a valid broadcast address.

Figure 22.7. UART Multi-Processor Mode Interconnect Diagram



22.3. Frame and Transmission Error Detection

All Modes:

The Transmit Collision bit (TXCOL0 bit in register SCON0) reads ‘1’ if user software writes data to the SBUF0 register while a transmit is in progress. Note that the TXCOL0 bit is also used as the SM20 bit when written by user software. This bit does not generate an interrupt.

Modes 1, 2, and 3:

The Receive Overrun bit (RXOV0 in register SCON0) reads ‘1’ if a new data byte is latched into the receive buffer before software has read the previous byte. Note that the RXOV0 bit is also used as the SM10 bit when written by user software. The Frame Error bit (FE0 in register SSTA0) reads ‘1’ if an invalid (low) STOP bit is detected. Note that the FE0 bit is also used as the SM00 bit when written by user software. The RXOV0 and FE0 bits do not generate interrupts.

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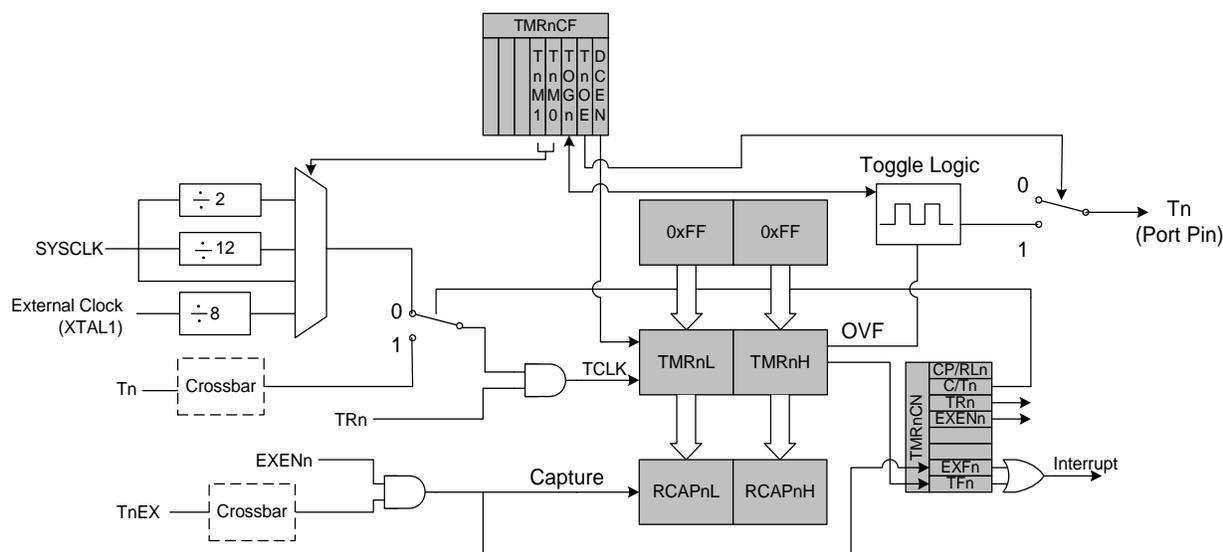
24.2.2. Capture Mode

In Capture Mode, Timer 2, 3, and 4 will operate as a 16-bit counter/timer with capture facility. When the Timer External Enable bit (found in the TMRnCN register) is set to '1', a high-to-low transition on the TnEX input pin causes the 16-bit value in the associated timer (TnH, TnL) to be loaded into the capture registers (RCAPnH, RCAPnL). If a capture is triggered in the counter/timer, the Timer External Flag (TMRnCN.6) will be set to '1' and an interrupt will occur if the interrupt is enabled. See Section "13.3. Interrupt Handler" on page 151 for further information concerning the configuration of interrupt sources.

As the 16-bit timer register increments and overflows TMRnH:TMRnL, the TFn Timer Overflow/Underflow Flag (TMRnCN.7) is set to '1' and an interrupt will occur if the interrupt is enabled. The timer can be configured to count down by setting the Decrement Enable Bit (TMRnCF.0) to '1'. This will cause the timer to decrement with every timer clock/count event and underflow when the timer transitions from 0x0000 to 0xFFFF. Just as in overflows, the Overflow/Underflow Flag (TFn) will be set to '1', and an interrupt will occur if enabled.

Counter/Timer with Capture mode is selected by setting the Capture/Reload Select bit CP/RLn (TMRnCN.0) and the Timer 2, 3, and 4 Run Control bit TRn (TnCON.2) to logic 1. The Timer 2, 3, and 4 respective External Enable EXENn (TnCON.3) must also be set to logic 1 to enable a captures. If EXENn is cleared, transitions on TnEX will be ignored.

Figure 24.11. T2, 3, and 4 Capture Mode Block Diagram



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Figure 24.18. TMRnH: Timer 2, 3, and 4 High Byte

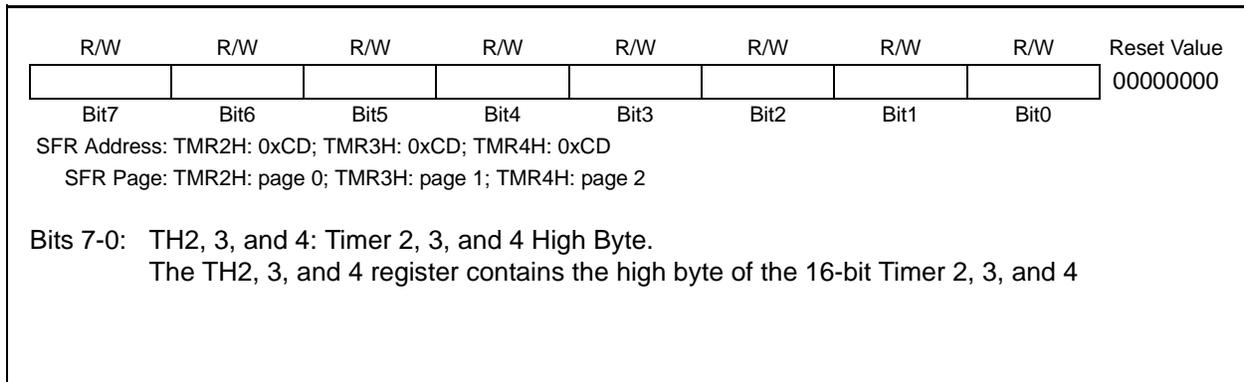


Table 26.2. Boundary Data Register Bit Definitions (C8051F061/3/5/7) (Continued)

EXTEST provides access to both capture and update actions, while Sample only performs a capture.

Bit	Action	Target
87, 89, 91, 93, 95, 97, 99, 101	Capture	P6.n input from pin (follows P0.n numbering scheme)†
	Update	P6.n output to pin (follows P0.n numbering scheme)†
102, 104, 106, 108, 110, 112, 114, 116	Capture	P7.n output enable from MCU (follows P0.n numbering scheme)†
	Update	P7.n output enable to pin (follows P0.n numbering scheme)†
103, 105, 107, 109, 111, 113, 115, 117	Capture	P7.n input from pin (follows P0.n numbering scheme)†
	Update	P7.n output to pin (follows P0.n numbering scheme)†

† Not connected to pins in this device package.

26.1.1. EXTEST Instruction

The EXTEST instruction is accessed via the IR. The Boundary DR provides control and observability of all the device pins as well as the Weak Pullup feature. All inputs to on-chip logic are set to logic 1.

26.1.2. SAMPLE Instruction

The SAMPLE instruction is accessed via the IR. The Boundary DR provides observability and presetting of the scan-path latches.

26.1.3. BYPASS Instruction

The BYPASS instruction is accessed via the IR. It provides access to the standard JTAG Bypass data register.

26.1.4. IDCODE Instruction

The IDCODE instruction is accessed via the IR. It provides access to the 32-bit Device ID register.

Figure 26.2. DEVICEID: JTAG Device ID Register

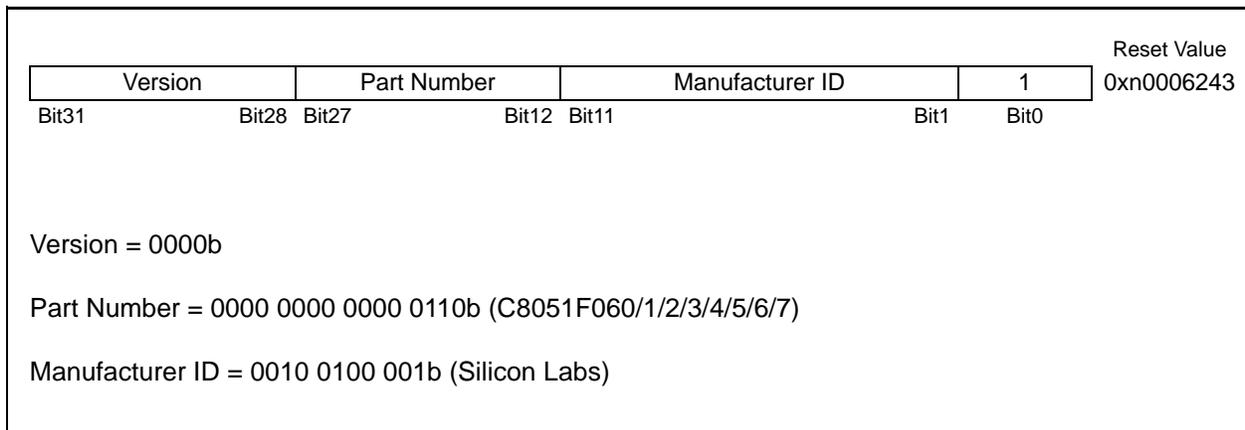


Figure 26.3. FLASHCON: JTAG Flash Control Register

SFLE	WRMD2	WRMD1	WRMD0	RDMD3	RDMD2	RDMD1	RDMD0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000

This register determines how the Flash interface logic will respond to reads and writes to the FLASHDAT Register.

Bit7: SFLE: Scratchpad Flash Memory Access Enable
 When this bit is set, Flash reads and writes through the JTAG port are directed to the 128-byte Scratchpad Flash sector. When SFLE is set to logic 1, Flash accesses out of the address range 0x00-0x7F should not be attempted. Reads/Writes out of this range will yield undefined results.
 0: Flash access from JTAG directed to the Program/Data Flash sector.
 1: Flash access from JTAG directed to the Scratchpad sector.

Bits6-4: WRMD2-0: Write Mode Select Bits.
 The Write Mode Select Bits control how the interface logic responds to writes to the FLASHDAT Register per the following values:
 000: A FLASHDAT write replaces the data in the FLASHDAT register, but is otherwise ignored.
 001: A FLASHDAT write initiates a write of FLASHDAT into the memory address by the FLASHADR register. FLASHADR is incremented by one when complete.
 010: A FLASHDAT write initiates an erasure (sets all bytes to 0xFF) of the Flash page containing the address in FLASHADR. The data written must be 0xA5 for the erase to occur. FLASHADR is not affected. If FLASHADR = 0x7BFE - 0x7BFF, the entire user space will be erased (i.e. entire Flash memory except for Reserved area 0x7C00 - 0x7FFF).
 (All other values for WRMD2-0 are reserved.)

Bits3-0: RDMD3-0: Read Mode Select Bits.
 The Read Mode Select Bits control how the interface logic responds to reads to the FLASHDAT Register per the following values:
 0000: A FLASHDAT read provides the data in the FLASHDAT register, but is otherwise ignored.
 0001: A FLASHDAT read initiates a read of the byte addressed by the FLASHADR register if no operation is currently active. This mode is used for block reads.
 0010: A FLASHDAT read initiates a read of the byte addressed by FLASHADR only if no operation is active and any data from a previous read has already been read from FLASHDAT. This mode allows single bytes to be read (or the last byte of a block) without initiating an extra read.
 (All other values for RDMD3-0 are reserved.)