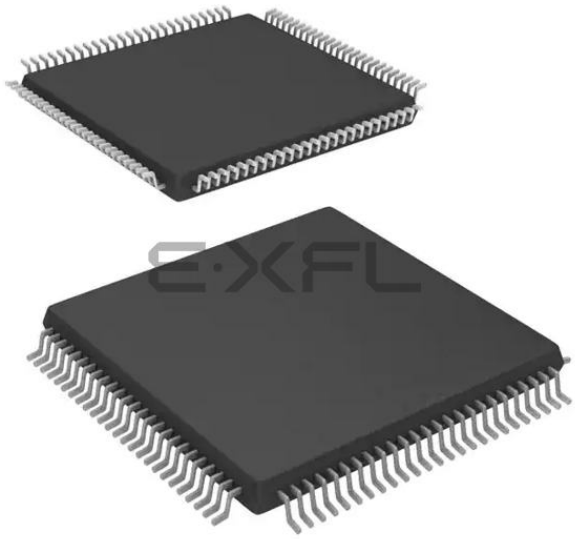

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 2x16b, 8x10b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f062r

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings*

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		-55		125	°C
Storage Temperature		-65		150	°C
Voltage on any pin (except VDD, AV+, AVDD, and Port 0) with respect to DGND		-0.3		VDD + 0.3	V
Voltage on any Port 0 Pin with respect to DGND.		-0.3		5.8	V
Voltage on VDD, AV+, or AVDD with respect to DGND		-0.3		4.2	V
Maximum Total current through VDD, AV+, AVDD, DGND, and AGND				800	mA
Maximum output current sunk by any Port pin				100	mA
Maximum output current sunk by any other I/O pin				50	mA
Maximum output current sourced by any Port pin				100	mA
Maximum output current sourced by any other I/O pin				50	mA

* Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

4. Pinout and Package Definitions

Table 4.1. Pin Definitions

Name	Pin Numbers				Type	Description
	F060	F061	F064	F065		
	F062	F063	F066	F067		
VDD	37, 64, 90	26, 40, 55	37, 64, 90	26, 40, 55		Digital Supply Voltage. Must be tied to +2.7 to +3.6 V.
DGND	38, 63, 89	27, 39, 54	38, 63, 89	27, 39, 54		Digital Ground. Must be tied to Ground.
AV+	11, 16, 24	7, 10, 18	11, 16, 24	7, 10, 18		Analog Supply Voltage. Must be tied to +2.7 to +3.6 V.
AVDD	13	23	13	23		Analog Supply Voltage. Must be tied to +2.7 to +3.6 V.
AGND	10, 14, 17, 23	6, 11, 19, 22	10, 14, 17, 23	6, 11, 19, 22		Analog Ground. Must be tied to Ground.
TMS	96	52	96	52	D In	JTAG Test Mode Select with internal pull-up.
TCK	97	53	97	53	D In	JTAG Test Clock with internal pull-up.
TDI	98	56	98	56	D In	JTAG Test Data Input with internal pull-up. TDI is latched on the rising edge of TCK.
TDO	99	57	99	57	D Out	JTAG Test Data Output with internal pull-up. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.
/RST	100	58	100	58	D I/O	Device Reset. Open-drain output of internal VDD monitor. Is driven low when VDD is <2.7 V and MONEN is high. An external source can initiate a system reset by driving this pin low.
XTAL1	26	20	26	20	A In	Crystal Input. This pin is the return for the internal oscillator circuit for a crystal or ceramic resonator. For a precision internal clock, connect a crystal or ceramic resonator from XTAL1 to XTAL2. If over-driven by an external CMOS clock, this becomes the system clock.
XTAL2	27	21	27	21	A Out	Crystal Output. This pin is the excitation driver for a crystal or ceramic resonator.
MONEN	28	63	28	63	D In	VDD Monitor Enable. When tied high, this pin enables the internal VDD monitor, which forces a system reset when VDD is < 2.7 V. When tied low, the internal VDD monitor is disabled. Recommended configuration is to connect directly to VDD.
VREF	4	61	4	61	A Out	Bandgap Voltage Reference Output
VREF0	21	15	21	15	A I/O	Bandgap Voltage Reference Output for ADC0. ADC0 Voltage Reference Input.

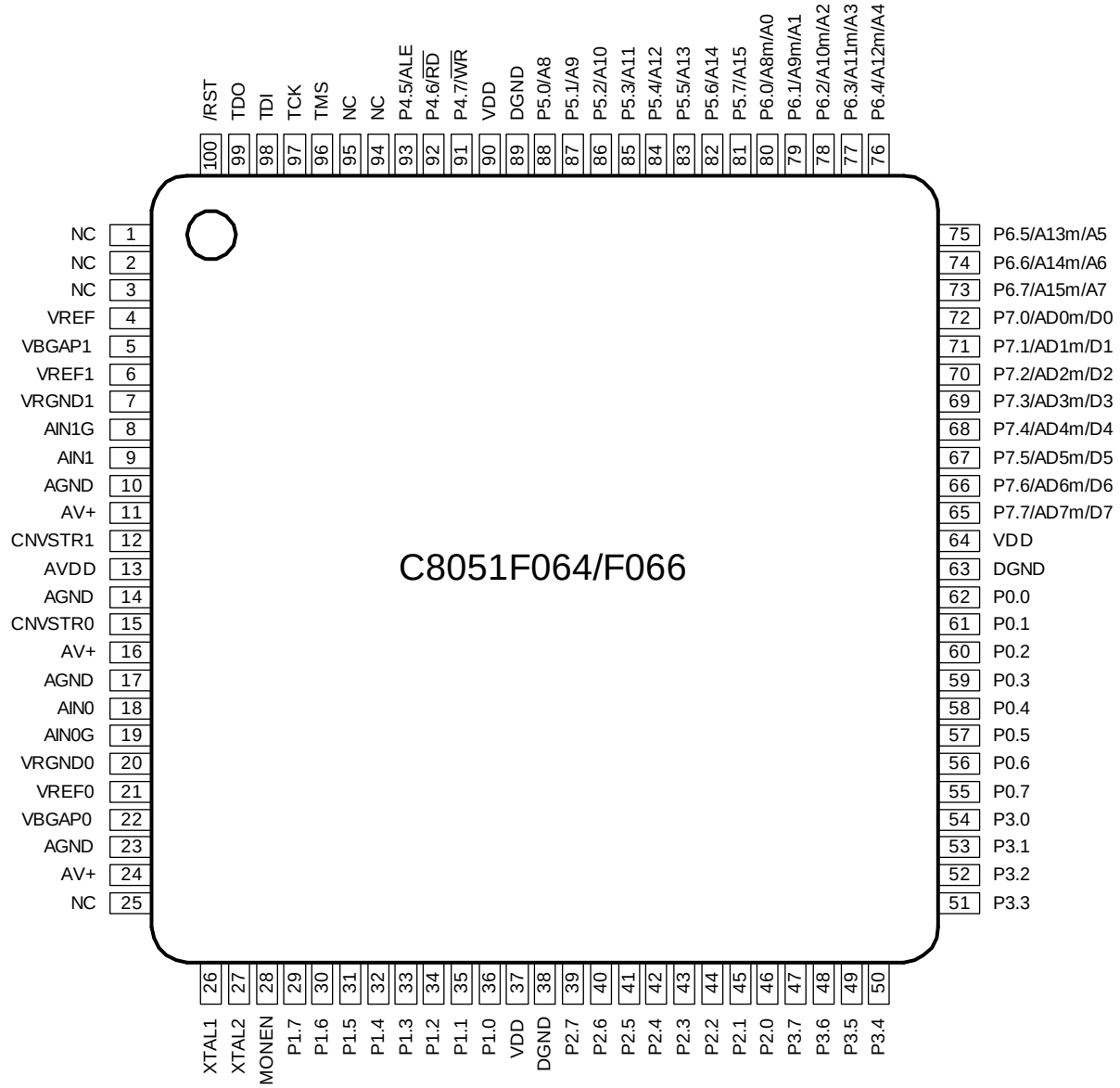


Figure 4.2. C8051F064 / C8051F066 Pinout Diagram (TQFP-100)

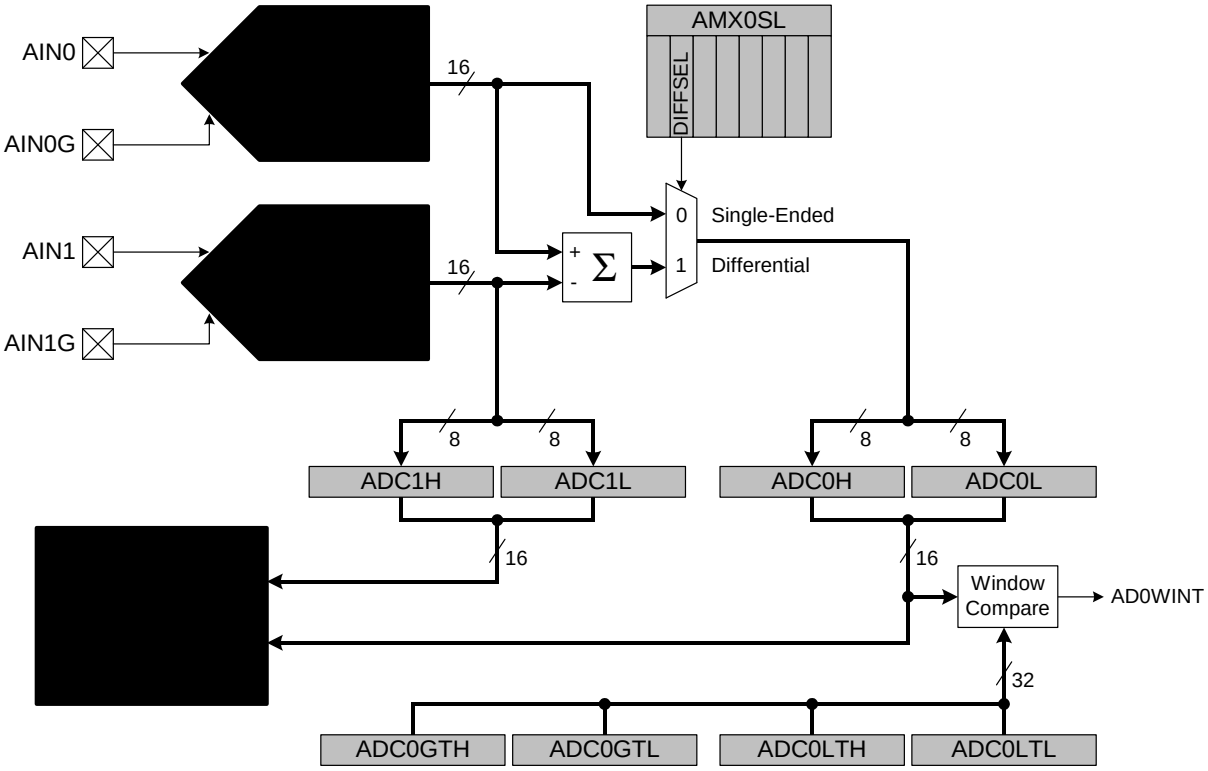


Figure 5.2. 16-bit ADC0 and ADC1 Data Path Diagram

5.1. Single-Ended or Differential Operation

ADC0 and ADC1 can be programmed to operate independently as single-ended ADCs, or together to accept a differential input. In single-ended mode, the ADCs can be configured to sample simultaneously, or to use different conversion speeds. In differential mode, ADC1 is a slave to ADC0, and its configuration is based on ADC0 settings, except during offset or gain calibrations. The DIFFSEL bit in the Channel Select Register AMX0SL (Figure 5.6) selects between single-ended and differential mode.

5.1.1. Pseudo-Differential Inputs

The inputs to the ADCs are pseudo-differential. The actual voltage measured by each ADC is equal to the voltage between the AINn pin and the AINnG pin. AINnG must be a DC signal between -0.2 and 0.6 V. In most systems, AINnG will be connected to AGND. If not tied to AGND, the AINnG signal can be used to negate a limited amount of fixed offset, but it is recommended that the internal offset calibration features of the device be used for this purpose. When operating in differential mode, AIN0G and AIN1G should be tied together. AINn must remain above AINnG in both modes for accurate conversion results.

6.2. DMA0 Instruction Format

DMA instructions can request single-ended data from both ADC0 and ADC1, as well as the differential combination of the two ADC inputs. The instruction format is identical to the DMA0IDT register, shown in Figure 6.7. Depending on which bits are set to ‘1’ in the instruction word, either 2 or 4 bytes of data will be written to XRAM for each DMA instruction cycle (excluding End-Of-Operation instructions). Table 6.1 details all of the valid DMA instructions. Instructions not listed in the table are not valid DMA instructions, and should not be used. Note that the ADCs can be independently controlled by the microcontroller when their outputs are not requested by the DMA.

Table 6.1. DMA0 Instruction Set

Instruction Word	Description	First Data Written to XRAM (2 bytes)	Second Data Written to XRAM (2 bytes)
00000000b	End-Of-Operation	none	none
10000000b	End-Of-Operation with Continuous Conversion	none	none
x0010000b	Retrieve ADC0 Data	ADC0H:ADC0L	none
x0100000b	Retrieve ADC1 Data	ADC1H:ADC1L	none
x0110000b	Retrieve ADC0 and ADC1 Data	ADC0H:ADC0L	ADC1H:ADC1L
x10x0000b	Retrieve Differential Data	ADC0H:ADC0L (differential result from both ADCs)	none
x11x0000b	Retrieve Differential and ADC1 Data	ADC0H:ADC0L (differential result from both ADCs)	ADC1H:ADC1L

6.3. XRAM Addressing and Setup

The DMA Interface can be configured to access either on-chip or off-chip XRAM. Any writes to on-chip XRAM by the DMA Control Logic occur when the processor core is not accessing the on-chip XRAM. This ensures that the DMA will not interfere with processor instruction timing.

Off-chip XRAM access (only available on the C8051F060/2/4/6) is controlled by the DMA0HLT bit in DMA0CF (DMA Configuration Register, Figure 6.5). The DMA will have full access to off-chip XRAM when this bit is ‘0’, and the processor core will have full access to off-chip XRAM when this bit is ‘1’. The DMA0HLT bit should be controlled in software when both the processor core and the DMA Interface require access to off-chip XRAM data space. Before setting DMA0HLT to ‘1’, the software should check the DMA0XBY bit to ensure that the DMA is not currently accessing off-chip XRAM. The processor core cannot access off-chip XRAM while DMA0HLT is ‘0’. The processor will continue as though it was able to perform the desired memory access, but the data will not be written to or read from off-chip XRAM. When the processor core is finished accessing off-chip XRAM, DMA0HLT should be set back to ‘0’in software to return control to the DMA Interface. The DMA Control Logic will wait until DMA0HLT is ‘0’ before writing data to off-chip XRAM. If new data becomes available to the DMA Interface before the previous data has been written, an overflow condition will occur, and the new data word may be lost.

The Data Address Pointer Registers (DMA0DSH and DMA0DSL) contain the 16-bit XRAM address location where the DMA interface will write data. When the DMA is initially enabled, the DMA Data Address

6.5. Instruction Execution in Mode 1

When the DMA interface begins an operation cycle, the DMA Instruction Status Register (DMA0ISW, Figure 6.9) is loaded with the address contained within the DMA Instruction Boundary Register (DMA0BND, Figure 6.8). The instruction is fetched from the Instruction Buffer, and the DMA Control Logic waits for data from the appropriate ADC(s). At the end of an instruction, the Repeat Counter (Registers DMA0CSH and DMA0CSL) is decremented, and the instruction will be repeated until the Repeat Counter reaches 0x0000. The Repeat Counter is then reset to the Repeat Counter Limit value (Registers DMA0CTH and DMA0CTL), and the DMA will increment DMA0ISW to the next instruction address. When the current DMA instruction is an End of Operation instruction, the Instruction Status Register is reset to the Instruction Boundary Register. If the Continuous Conversion bit (bit 7, CCNV) in the End of Operation instruction word is set to '1', the DMA will continue to execute instructions. When CCNV is set to '0', the DMA will stop executing instructions at this point. An example of Mode 1 operation is shown in Figure 6.3.

Figure 6.3. DMA Mode 1 Operation

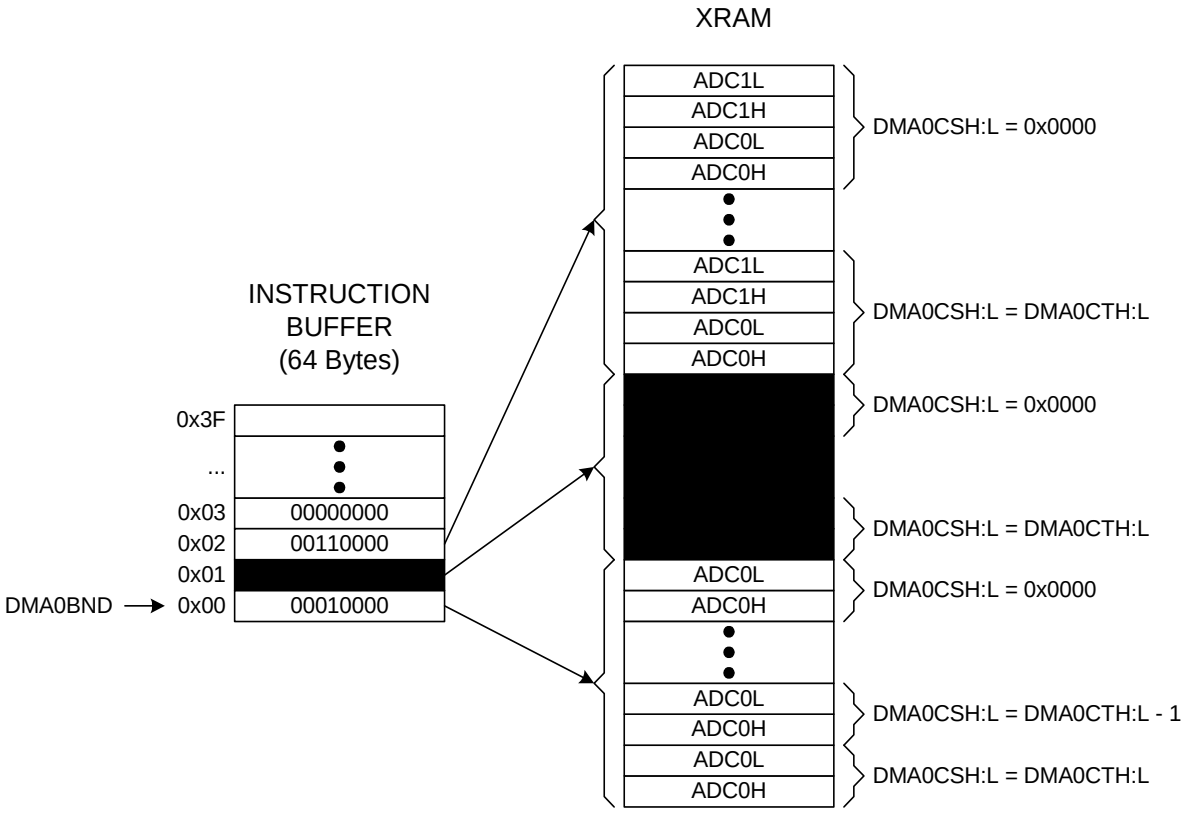


Figure 6.4. DMA0CN: DMA0 Control Register

SFR Page: 3
SFR Address: 0xD8 (bit addressable)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
DMA0EN	DMA0INT	DMA0MD	DMA0DE1	DMA0DE0	DMA0DOE	DMA0DO1	DMA0DO0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit 7: DMA0EN: DMA0 Enable.
Write:
0: Stop DMA0 Operations.
1: Begin DMA0 Operations.
Read:
0: DMA0 is Idle.
1: DMA0 Operation is in Progress.

Bit 6: DMA0INT: DMA0 Operations Complete Flag.
0: DMA0 has not completed all operations.
1: DMA0 operations are complete. This bit must be cleared by software.

Bit 5: DMA0MD: DMA0 Mode Select.
0: DMA0 will operate in Mode 0.
1: DMA0 will operate in Mode 1.

Bit 4: DMA0DE1: ADC1 Data Overflow Error Flag.
0: ADC1 Data Overflow has not occured.
1: ADC1 Data Overflow has occured, and data from ADC1 has been lost. This bit must be cleared by software.

Bit 3: DMA0DE0: ADC0 Data Overflow Error Flag.
0: ADC0 Data Overflow has not occured.
1: ADC0 Data Overflow has occured, and data from ADC0 has been lost. This bit must be cleared by software.

Bit 2: DMA0DOE: Data Overflow Warning Interrupt Enable.
0: Disable Data Overflow Warning interrupts.
1: Enable Data Overflow Warning interrups.

Bit 1: DMA0DO1: ADC1 Data Overflow Warning Flag.
0: No ADC1 Data Buffer Warnings have been issued.
1: ADC1 Data Buffer is full, and the DMA has not written previous data to XRAM. This bit must be cleared by software.

Bit 0: DMA0DO0: ADC0 Data Overflow Warning Flag.
0: No ADC0 Data Buffer Warnings have been issued.
1: ADC0 Data Buffer is full, and the DMA has not written previous data to XRAM. This bit must be cleared by software.

Figure 8.7. DAC1CN: DAC1 Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
DAC1EN	-	-	DAC1MD1	DAC1MD0	DAC1DF2	DAC1DF1	DAC1DF0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD4
SFR Page: 1

Bit7: DAC1EN: DAC1 Enable Bit.
0: DAC1 Disabled. DAC1 Output pin is disabled; DAC1 is in low-power shutdown mode.
1: DAC1 Enabled. DAC1 Output pin is active; DAC1 is operational.

Bits6-5: UNUSED. Read = 00b; Write = don't care.

Bits4-3: DAC1MD1-0: DAC1 Mode Bits:
00: DAC output updates occur on a write to DAC1H.
01: DAC output updates occur on Timer 3 overflow.
10: DAC output updates occur on Timer 4 overflow.
11: DAC output updates occur on Timer 2 overflow.

Bits2-0: DAC1DF2: DAC1 Data Format Bits:

000: The most significant nibble of the DAC1 Data Word is in DAC1H[3:0], while the least significant byte is in DAC1L.

DAC1H								DAC1L							
				MSB											LSB

001: The most significant 5-bits of the DAC1 Data Word is in DAC1H[4:0], while the least significant 7-bits are in DAC1L[7:1].

DAC1H								DAC1L							
			MSB											LSB	

010: The most significant 6-bits of the DAC1 Data Word is in DAC1H[5:0], while the least significant 6-bits are in DAC1L[7:2].

DAC1H								DAC1L							
		MSB											LSB		

011: The most significant 7-bits of the DAC1 Data Word is in DAC1H[6:0], while the least significant 5-bits are in DAC1L[7:3].

DAC1H								DAC1L							
	MSB											LSB			

1xx: The most significant 8-bits of the DAC1 Data Word is in DAC1H[7:0], while the least significant 4-bits are in DAC1L[7:4].

DAC1H								DAC1L							
MSB											LSB				

10. Voltage Reference 2 (C8051F061/3)

The internal voltage reference circuit consists of a 1.2 V, temperature stable bandgap voltage reference generator and a gain-of-two output buffer amplifier. The internal reference may be routed via the VREF pin to external system components or to the VREF2 input pin shown in Figure 10.1. The maximum load seen by the VREF pin must be less than 200 µA to AGND. Bypass capacitors of 0.1 µF and 4.7 µF are recommended from the VREF pin to AGND, as shown in Figure 10.1.

The VREF2 pin provides a voltage reference input for ADC2 and the DACs. ADC2 may also reference the analog power supply voltage, via the VREF multiplexers shown in Figure 10.1.

The Reference Control Register 2, REF2CN (defined in Figure 10.2) enables/disables the internal reference generator and selects the reference input for ADC2. The BIASE bit in REF2CN enables the on-board reference generator while the REFBE bit enables the gain-of-two buffer amplifier which drives the VREF pin. When disabled, the supply current drawn by the bandgap and buffer amplifier falls to less than 1 µA (typical) and the output of the buffer amplifier enters a high impedance state. If the internal bandgap is used as the reference voltage generator, BIASE and REFBE must both be set to logic 1. If the internal reference is not used, REFBE may be set to logic 0. Note that the BIASE bit must be set to logic 1 if ADC2 or either DAC is used, regardless of the voltage reference used. If neither ADC2 nor the DACs are being used, both of these bits can be set to logic 0 to conserve power. Bit AD2VRS selects between VREF2 and AV+ for the ADC2 voltage reference source. The electrical specifications for the Voltage Reference are given in Table 10.1.

Figure 10.1. Voltage Reference Functional Block Diagram

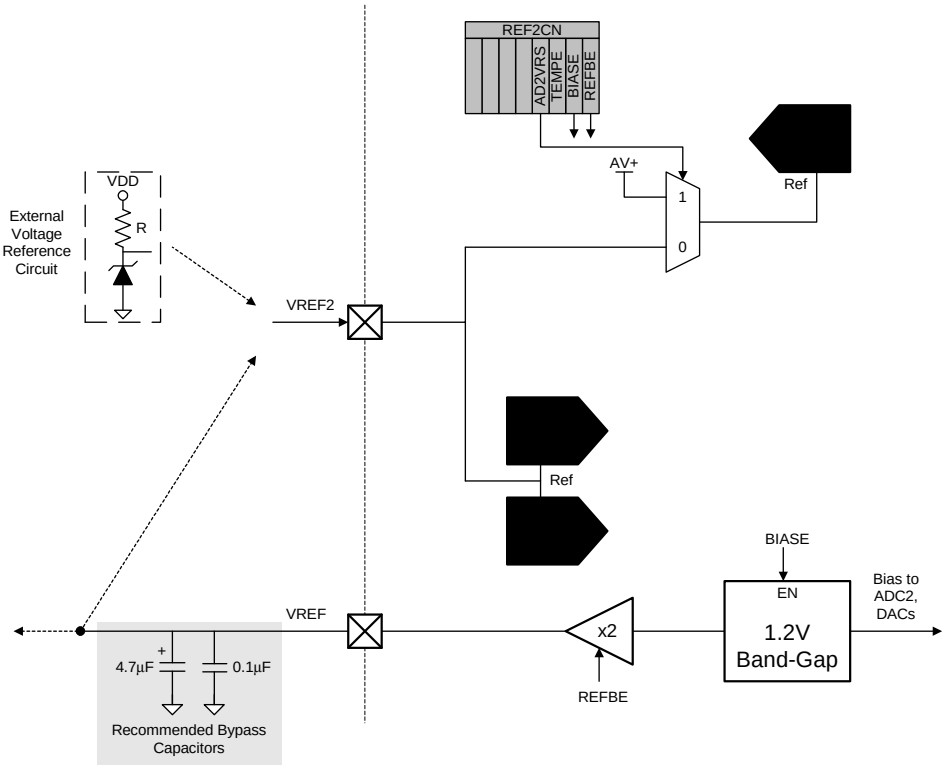


Figure 11.2. REF2CN: Reference Control Register 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	0	0	BIASE	REFBE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD1
SFR Page: 2

Bits7-4: UNUSED. Read = 0000b; Write = don't care.
Bits2-3: RESERVED. Must Write to 00b.
Bit1: BIASE: ADC/DAC Bias Generator Enable Bit. (Must be '1' if using ADC2 or DACs).
0: Internal Bias Generator Off.
1: Internal Bias Generator On.
Bit0: REFBE: Internal Reference Buffer Enable Bit.
0: Internal Reference Buffer Off.
1: Internal Reference Buffer On. Internal voltage reference is driven on the VREF pin.

Table 11.1. Voltage Reference Electrical Characteristics

VDD = 3.0 V, AV+ = 3.0 V, -40 to +85 °C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Internal Reference (REFBE = 1)					
Output Voltage	25 °C ambient	2.36	2.43	2.48	V
VREF Power Supply Current			50		µA
VREF Short-Circuit Current				30	mA
VREF Temperature Coefficient			15		ppm/°C
Load Regulation	Load = 0 to 200 µA to AGND		0.5		ppm/µA
VREF Turn-on Time 1	4.7 µF tantalum, 0.1 µF ceramic bypass		2		ms
VREF Turn-on Time 2	0.1 µF ceramic bypass		20		µs
VREF Turn-on Time 3	no bypass cap		10		µs

Table 13.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
ANL C, /bit	AND complement of direct bit to Carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to Carry	2	2
MOV C, bit	Move direct bit to Carry	2	2
MOV bit, C	Move Carry to direct bit	2	2
JC rel	Jump if Carry is set	2	2/3
JNC rel	Jump if Carry is not set	2	2/3
JB bit, rel	Jump if direct bit is set	3	3/4
JNB bit, rel	Jump if direct bit is not set	3	3/4
JBC bit, rel	Jump if direct bit is set and clear bit	3	3/4
Program Branching			
ACALL addr11	Absolute subroutine call	2	3
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	5
RETI	Return from interrupt	1	5
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
JZ rel	Jump if A equals zero	2	2/3
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	3/4
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/4
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/3
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/4
NOP	No operation	1	1

While in the ADC2 ISR, a PCA interrupt occurs. Recall the PCA interrupt is configured as a *high* priority interrupt, while the ADC2 interrupt is configured as a *low* priority interrupt. Thus, the CIP-51 will now vector to the high priority PCA ISR. Upon doing so, the CIP-51 will automatically place the SFR page needed to access the PCA's special function registers into the SFRPAGE register, SFR Page 0x00. The value that was in the SFRPAGE register before the PCA interrupt (SFR Page 2 for ADC2) is pushed down the stack into SFRNEXT. Likewise, the value that was in the SFRNEXT register before the PCA interrupt (in this case SFR Page 0x0F for Port 5) is pushed down to the SFRLAST register, the "bottom" of the stack. Note that a value stored in SFRLAST (via a previous software write to the SFRLAST register) will be overwritten. See Figure 13.6 below.

Figure 13.6. SFR Page Stack Upon PCA Interrupt Occurring During an ADC2 ISR

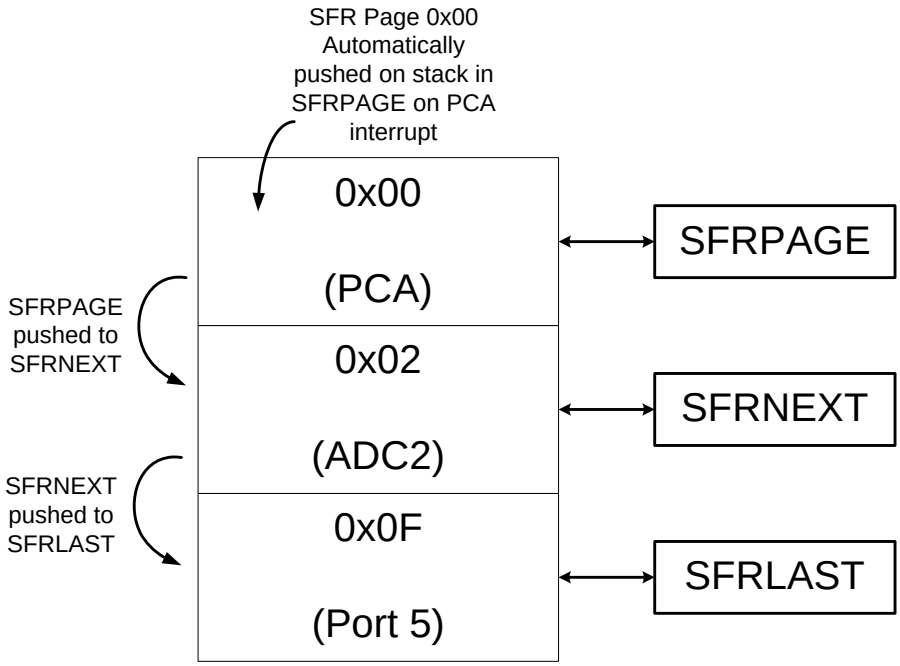


Table 13.2. Special Function Register (SFR) Memory Map

ADDRESS	SFR PAGE	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
F8	0 1 2 3 F	SPI0CN CAN0CN DMA0CF P7	PCA0L DMA0CTL	PCA0H DMA0CTH	PCA0CPL0 DMA0CSL	PCA0CPH0 DMA0CSH	PCA0CPL1 DMA0BND	PCA0CPH1 DMA0ISW	WDTCN **(ALL PAGES)**
F0	0 1 2 3 F	B **(ALL PAGES)**						EIP1 **(ALL PAGES)**	EIP2 **(ALL PAGES)**
E8	0 1 2 3 F	ADC0CN ADC1CN ADC2CN P6	PCA0CPL2	PCA0CPH2	PCA0CPL3	PCA0CPH3	PCA0CPL4	PCA0CPH4	RSTSRC
E0	0 1 2 3 F	ACC **(ALL PAGES)**	PCA0CPL5 XBR0	PCA0CPH5 XBR1	XBR2	XBR3		EIE1 **(ALL PAGES)**	EIE2 **(ALL PAGES)**
D8	0 1 2 3 F	PCA0CN CAN0DATL DMA0CN P5	PCA0MD CAN0DATH DMA0DAL	PCA0CPM0 CAN0ADR DMA0DAH	PCA0CPM1 CAN0TST DMA0DSL	PCA0CPM2 DMA0DSH	PCA0CPM3 DMA0IPT	PCA0CPM4 DMA0IDT	PCA0CPM5
D0	0 1 2 3 F	PSW **(ALL PAGES)**	REF0CN REF1CN REF2CN	DAC0L DAC1L	DAC0H DAC1H	DAC0CN DAC1CN			
C8	0 1 2 3 F	TMR2CN TMR3CN TMR4CN P4	TMR2CF TMR3CF TMR4CF	RCAP2L RCAP3L RCAP4L	RCAP2H RCAP3H RCAP4H	TMR2L TMR3L TMR4L	TMR2H TMR3H TMR4H		SMB0CR
C0	0 1 2 3 F	SMB0CN CAN0STA	SMB0STA	SMB0DAT	SMB0ADR	ADC0GTL ADC2GTL	ADC0GTH ADC2GTH	ADC0LTL ADC2LTL	ADC0LTH ADC2LTH
B8	0 1 2 3 F	IP **(ALL PAGES)**	SADEN0	AMX2CF ADC0CPT	AMX0SL AMX2SL ADC0CCF	ADC0CF ADC1CF ADC2CF		ADC0L ADC1L ADC2L	ADC0H ADC1H ADC2H
		0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

Table 13.4. Interrupt Summary

Interrupt Source	Interrupt Vector	Priority Order	Pending Flag	Bit addressable	Cleared by HW	Enable Flag	Priority Control
Reset	0x0000	Top	None	N/A	N/A	Always Enabled	Always Highest
External Interrupt 0 (/INT0)	0x0003	0	IE0 (TCON.1)	Y	Y	EX0 (IE.0)	PX0 (IP.0)
Timer 0 Overflow	0x000B	1	TF0 (TCON.5)	Y	Y	ET0 (IE.1)	PT0 (IP.1)
External Interrupt 1 (/INT1)	0x0013	2	IE1 (TCON.3)	Y	Y	EX1 (IE.2)	PX1 (IP.2)
Timer 1 Overflow	0x001B	3	TF1 (TCON.7)	Y	Y	ET1 (IE.3)	PT1 (IP.3)
UART0	0x0023	4	RI0 (SCON0.0) TI0 (SCON0.1)	Y		ES0 (IE.4)	PS0 (IP.4)
Timer 2	0x002B	5	TF2 (TMR2CN.7)	Y		ET2 (IE.5)	PT2 (IP.5)
Serial Peripheral Interface	0x0033	6	SPIF (SPI0CN.7) WCOL (SPI0CN.6) MODF (SPI0CN.5) RXOVRN (SPI0CN.4)	Y		ESPI0 (EIE1.0)	PSPI0 (EIP1.0)
SMBus Interface	0x003B	7	SI (SMB0CN.3)	Y		ESMB0 (EIE1.1)	PSMB0 (EIP1.1)
ADC0 Window Comparator	0x0043	8	AD0WINT (ADC0CN.1)	Y		EWADC0 (EIE1.2)	PWADC0 (EIP1.2)
Programmable Counter Array	0x004B	9	CF (PCA0CN.7) CCFn (PCA0CN.n)	Y		EPCA0 (EIE1.3)	PPCA0 (EIP1.3)
Comparator 0	0x0053	10	CP0FIF/CP0RIF (CPT0CN.4/.5)	Y		CP0IE (EIE1.4)	PCP0 (EIP1.4)
Comparator 1	0x005B	11	CP1FIF/CP1RIF (CPT1CN.4/.5)	Y		CP1IE (EIE1.5)	PCP1 (EIP1.5)
Comparator 2	0x0063	12	CP2FIF/CP2RIF (CPT2CN.4/.5)	Y		CP2IE (EIE1.6)	PCP2 (EIP1.6)
ADC0 End of Conversion	0x006B	13	ADC0INT (ADC0CN.5)	Y		EADC0 (EIE1.7)	PADC0 (EIP1.7)
Timer 3	0x0073	14	TF3 (TMR3CN.7)	Y		ET3 (EIE2.0)	PT3 (EIP2.0)
ADC1 End of Conversion	0x007B	15	ADC1INT (ADC1CN.5)	Y		EADC1 (EIE2.1)	PADC1 (EIP2.1)
Timer 4	0x0083	16	TF4 (TMR4CN.7)	Y		ET4 (EIE2.2)	PT4 (EIP2.2)
ADC2 Window Comparator	0x008B	17	AD2WINT (ADC2CN.1)	Y		EWADC2 (EIE2.3)	PWADC2 (EIP2.3)
ADC2 End of Conversion	0x0093	18	AD2INT (ADC2CN.5)	Y		EADC2 (EIE2.4)	PADC2 (EIP2.4)
CAN Interrupt	0x009B	19	CAN0CN.7	Y	Y	ECAN0 (EIE2.5)	PCAN0 (EIP2.5)
UART1	0x00A3	20	RI1 (SCON1.0) TI1 (SCON1.1)	Y		ES1 (EIP2.6)	PS1 (EIP2.6)
DMA0 Interrupt	0x00AB	21	DMA0INT (DMA0CN.6)	Y		EDMA0 (EIE2.7)	PDMA0 (EIP2.7)

Table 14.1. Reset Electrical Characteristics

-40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
/RST Output Low Voltage	I_{OL} = 8.5 mA, VDD = 2.7 V to 3.6 V			0.6	V
/RST Input High Voltage		0.7 x VDD			V
/RST Input Low Voltage				0.3 x VDD	
/RST Input Leakage Current	/RST = 0.0 V		50		µA
VDD for /RST Output Valid		1.0			V
AV+ for /RST Output Valid		1.0			V
VDD POR Threshold (V_{RST})		2.40	2.55	2.70	V
Minimum /RST Low Time to Generate a System Reset		10			ns
Reset Time Delay	/RST rising edge after VDD crosses V_{RST} threshold	80	100	120	ms
Missing Clock Detector Time-out	Time from last system clock to reset initiation	100	220	500	µs

17. External Data Memory Interface and On-Chip XRAM

The C8051F060/1/2/3/4/5/6/7 MCUs include 4 k bytes of on-chip RAM mapped into the external data memory space (XRAM). In addition, the C8051F060/2/4/6 include an External Data Memory Interface which can be used to access off-chip memories and memory-mapped devices connected to the GPIO ports. The external memory space may be accessed using the external move instruction (MOVX) and the data pointer (DPTR), or using the MOVX indirect addressing mode using R0 or R1. If the MOVX instruction is used with an 8-bit address operand (such as @R1), then the high byte of the 16-bit address is provided by the External Memory Interface Control Register (EMI0CN, shown in Figure 17.1). Note: the MOVX instruction can also be used for writing to the Flash memory. See Section “16. Flash Memory” on page 177 for details. The MOVX instruction accesses XRAM by default.

17.1. Accessing XRAM

The XRAM memory space (both internal and external) is accessed using the MOVX instruction. The MOVX instruction has two forms, both of which use an indirect addressing method. The first method uses the Data Pointer, DPTR, a 16-bit register which contains the effective address of the XRAM location to be read or written. The second method uses R0 or R1 in combination with the EMI0CN register to generate the effective XRAM address. Examples of both of these methods are given below.

17.1.1. 16-Bit MOVX Example

The 16-bit form of the MOVX instruction accesses the memory location pointed to by the contents of the DPTR register. The following series of instructions reads the value of the byte at address 0x1234 into the accumulator A:

```
MOV    DPTR, #1234h        ; load DPTR with 16-bit address to read (0x1234)
MOVX   A, @DPTR            ; load contents of 0x1234 into accumulator A
```

The above example uses the 16-bit immediate MOV instruction to set the contents of DPTR. Alternately, the DPTR can be accessed through the SFR registers DPH, which contains the upper 8-bits of DPTR, and DPL, which contains the lower 8-bits of DPTR.

17.1.2. 8-Bit MOVX Example

The 8-bit form of the MOVX instruction uses the contents of the EMI0CN SFR to determine the upper 8-bits of the effective address to be accessed and the contents of R0 or R1 to determine the lower 8-bits of the effective address to be accessed. The following series of instructions read the contents of the byte at address 0x1234 into the accumulator A.

```
MOV    EMI0CN, #12h        ; load high byte of address into EMI0CN
MOV    R0, #34h            ; load low byte of address into R0 (or R1)
MOVX   a, @R0              ; load contents of 0x1234 into accumulator A
```

24.1.2. Mode 1: 16-bit Counter/Timer

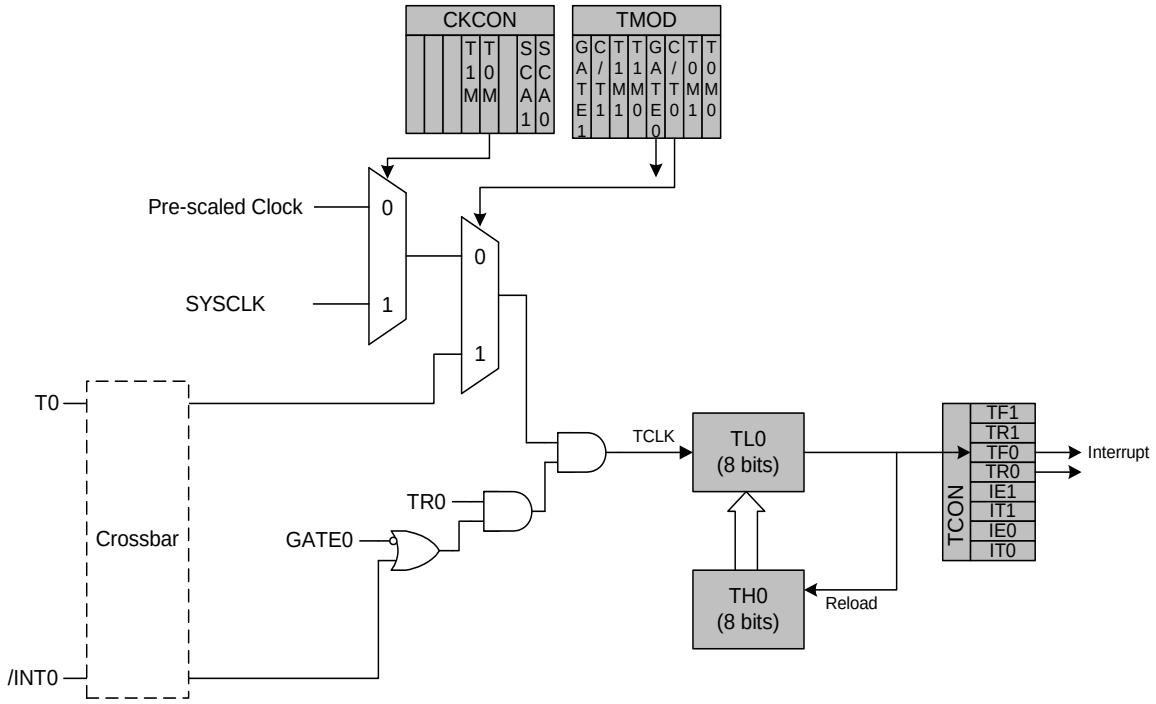
Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.

24.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload

Mode 2 configures Timer 0 or Timer 1 to operate as 8-bit counter/timers with automatic reload of the start value. TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from 0xFF to 0x00, the timer overflow flag TF0 (TCON.5) is set and the counter in TL0 is reloaded from TH0. If Timer 0 interrupts are enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. When in Mode 2, Timer 1 operates identically to Timer 0.

Both counter/timers are enabled and configured in Mode 2 in the same manner as Mode 0. Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or when the input signal /INT0 is low.

Figure 24.2. T0 Mode 2 Block Diagram



25.1. PCA Counter/Timer

The 16-bit PCA counter/timer consists of two 8-bit SFRs: PCA0L and PCA0H. PCA0H is the high byte (MSB) of the 16-bit counter/timer and PCA0L is the low byte (LSB). Reading PCA0L automatically latches the value of PCA0H into a “snapshot” register; the following PCA0H read accesses this “snapshot” register. Reading the PCA0L Register first guarantees an accurate reading of the entire 16-bit PCA0 counter. Reading PCA0H or PCA0L does not disturb the counter operation. The CPS2-CPS0 bits in the PCA0MD register select the timebase for the counter/timer as shown in Table 25.1.

When the counter/timer overflows from 0xFFFF to 0x0000, the Counter Overflow Flag (CF) in PCA0MD is set to logic 1 and an interrupt request is generated if CF interrupts are enabled. Setting the ECF bit in PCA0MD to logic 1 enables the CF flag to generate an interrupt request. The CF bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software (Note: PCA0 interrupts must be globally enabled before CF interrupts are recognized. PCA0 interrupts are globally enabled by setting the EA bit (IE.7) and the EPCA0 bit in EIE1 to logic 1). Clearing the CIDL bit in the PCA0MD register allows the PCA to continue normal operation while the CPU is in Idle mode.

Table 25.1. PCA Timebase Input Options

CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)
1	0	0	System clock
1	0	1	External oscillator source divided by 8 (synchronized with system clock)

Figure 25.2. PCA Counter/Timer Block Diagram

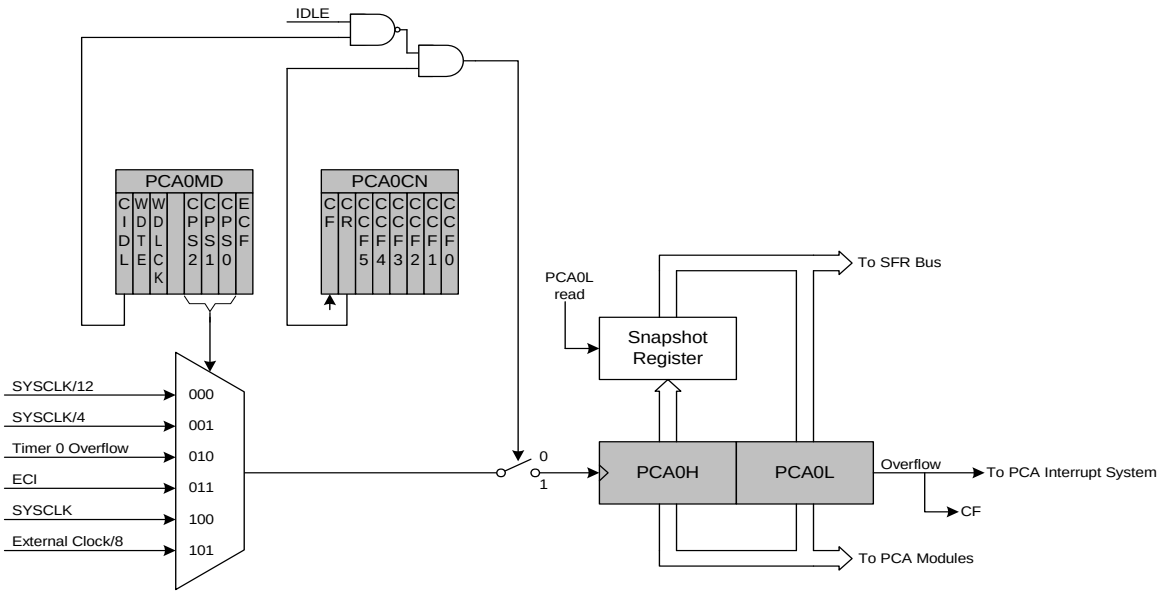


Figure 25.15. PCA0CPLn: PCA0 Capture Module Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPL0: 0xFB, PCA0CPL1: 0xFD, PCA0CPL2: 0xE9, PCA0CPL3: 0xEB, PCA0CPL4: 0xED, PCA0CPL5: 0xE1

SFR Page: PCA0CPL0: page 0, PCA0CPL1: page 0, PCA0CPL2: page 0, PCA0CPL3: page 0, PCA0CPL4: page 0, PCA0CPL5: page 0

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Bits7-0: PCA0CPLn: PCA0 Capture Module Low Byte.
The PCA0CPLn register holds the low byte (LSB) of the 16-bit capture module n.

Figure 25.16. PCA0CPHn: PCA0 Capture Module High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: PCA0CPH0: 0xFC, PCA0CPH1: 0xFD, PCA0CPH2: 0xEA, PCA0CPH3: 0xEC, PCA0CPH4: 0xEE, PCA0CPH5: 0xE2

SFR Page: PCA0CPH0: page 0, PCA0CPH1: page 0, PCA0CPH2: page 0, PCA0CPH3: page 0, PCA0CPH4: page 0, PCA0CPH5: page 0

Bits7-0: PCA0CPHn: PCA0 Capture Module High Byte.
The PCA0CPHn register holds the high byte (MSB) of the 16-bit capture module n.