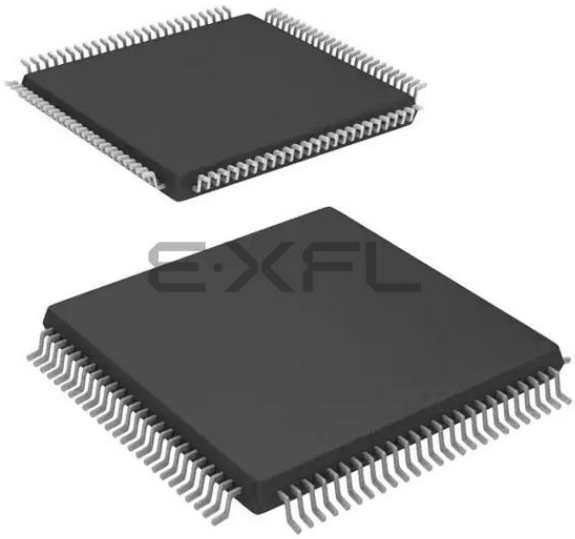

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f064

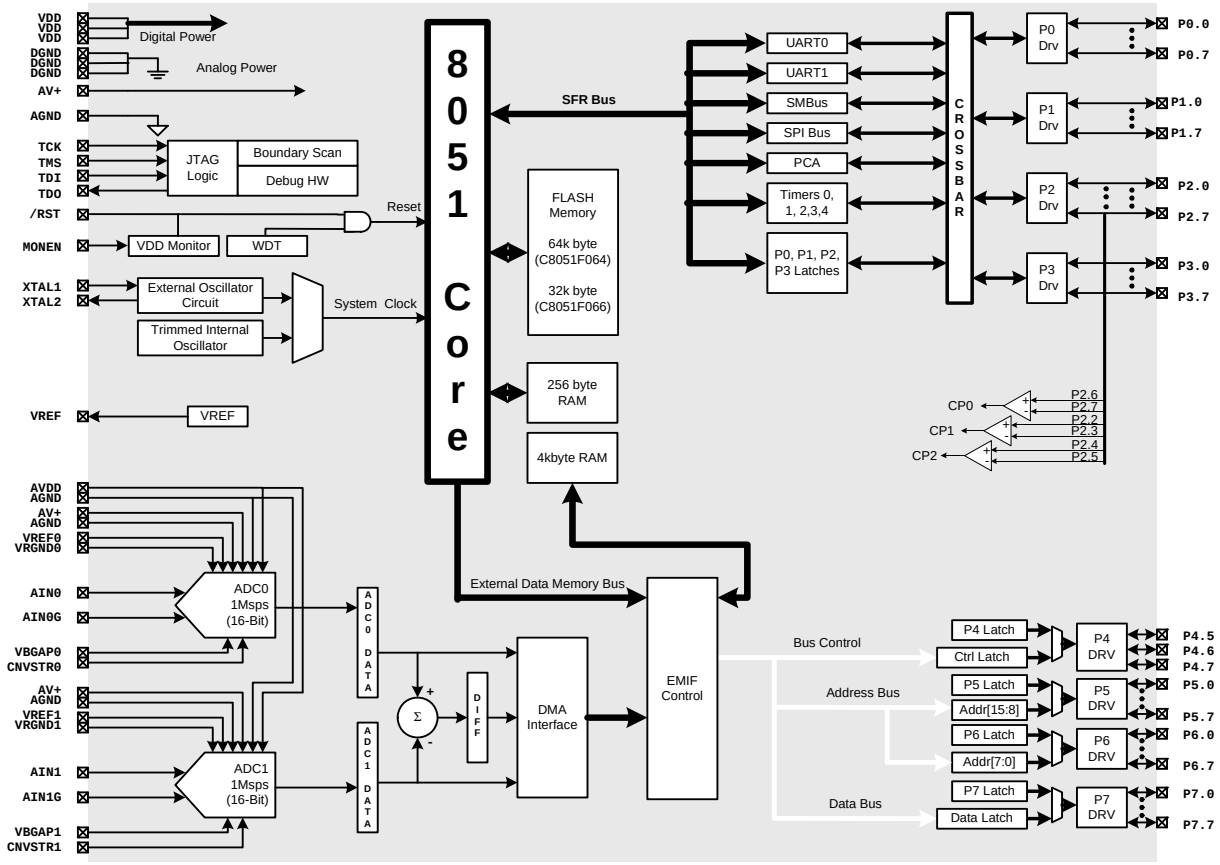


Figure 1.3. C8051F064 / C8051F066 Block Diagram

5. 16-Bit ADCs (ADC0 and ADC1)

The ADC subsystem for the C8051F060/1/2/3/4/5/6/7 consists of two 1 Msps, 16-bit successive-approximation-register ADCs with integrated track-and-hold, a Programmable Window Detector, and a DMA interface (see block diagrams in Figure 5.1 and Figure 5.2). The ADCs can be configured as two separate, single-ended ADCs, or as a differential pair. The Data Conversion Modes, Window Detector, and DMA interface are all configurable under software control via the Special Function Registers shown in Figure 5.1 and Figure 5.2. The voltage references used by ADC0 and ADC1 are selected as described in Section 5.2. The ADCs and their respective track-and-hold circuitry can be independently enabled or disabled with the Special Function Registers. Either ADC can be enabled by setting the ADnEN bit in the ADC's Control register (ADCnCN) to logic 1. The ADCs are in low power shutdown when these bits are logic 0.

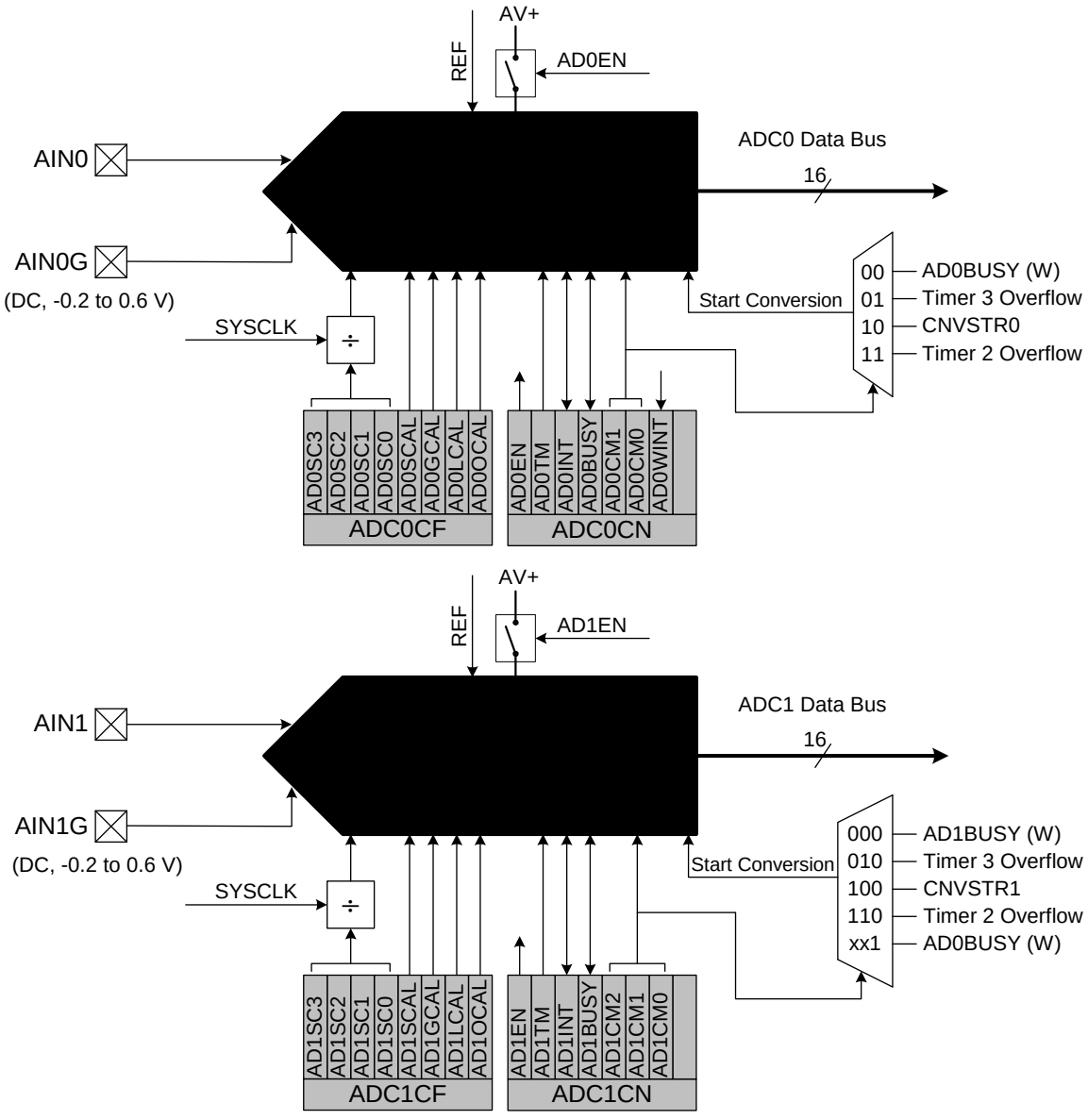
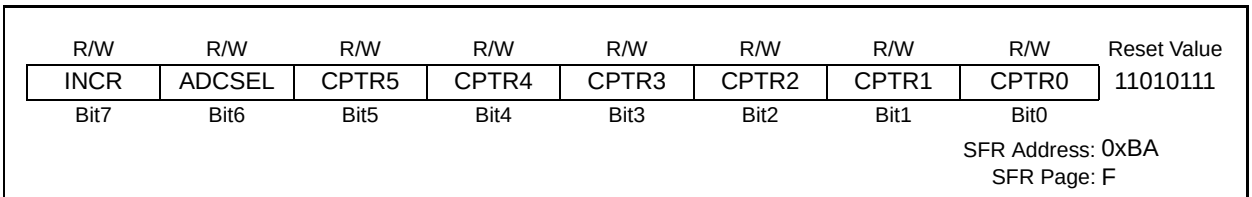


Figure 5.1. 16-Bit ADC0 and ADC1 Control Path Diagram

Figure 5.22. ADC0CPT: ADC Calibration Pointer Register



R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
INCR	ADCSEL	CPTR5	CPTR4	CPTR3	CPTR2	CPTR1	CPTR0	11010111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

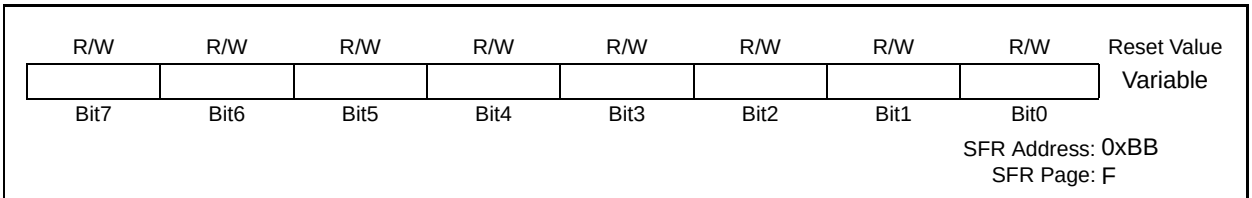
SFR Address: 0xBA
SFR Page: F

Bit 7: INCR: Pointer Address Automatic Increment.
0: Disable Auto-Increment.
1: Enable Auto-Increment. CPTR5-0 will automatically be incremented after each read or write to ADC0CCF.

Bit 6: ADCSEL: ADC Calibration Coefficient Select.
0: Reads and Writes of ADC0CCF will access ADC0 Calibration Coefficients.
1: Reads and Writes of ADC0CCF will access ADC1 Calibration Coefficients.

Bits 5-0: CPTR5-0: Calibration Coefficent Pointer.
Select which Calibration Coefficient location will be accessed when ADC0CCF is read or written.

Figure 5.23. ADC0CCF: ADC Calibration Coefficient Register



R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBB
SFR Page: F

Bits 7-0: Calibration Coefficients at the location specified in ADC0CPT. See Table 5.19.

Figure 6.4. DMA0CN: DMA0 Control Register

SFR Page: 3
SFR Address: 0xD8 (bit addressable)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
DMA0EN	DMA0INT	DMA0MD	DMA0DE1	DMA0DE0	DMA0DOE	DMA0DO1	DMA0DO0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit 7: DMA0EN: DMA0 Enable.
Write:
0: Stop DMA0 Operations.
1: Begin DMA0 Operations.
Read:
0: DMA0 is Idle.
1: DMA0 Operation is in Progress.

Bit 6: DMA0INT: DMA0 Operations Complete Flag.
0: DMA0 has not completed all operations.
1: DMA0 operations are complete. This bit must be cleared by software.

Bit 5: DMA0MD: DMA0 Mode Select.
0: DMA0 will operate in Mode 0.
1: DMA0 will operate in Mode 1.

Bit 4: DMA0DE1: ADC1 Data Overflow Error Flag.
0: ADC1 Data Overflow has not occured.
1: ADC1 Data Overflow has occured, and data from ADC1 has been lost. This bit must be cleared by software.

Bit 3: DMA0DE0: ADC0 Data Overflow Error Flag.
0: ADC0 Data Overflow has not occured.
1: ADC0 Data Overflow has occured, and data from ADC0 has been lost. This bit must be cleared by software.

Bit 2: DMA0DOE: Data Overflow Warning Interrupt Enable.
0: Disable Data Overflow Warning interrupts.
1: Enable Data Overflow Warning interrups.

Bit 1: DMA0DO1: ADC1 Data Overflow Warning Flag.
0: No ADC1 Data Buffer Warnings have been issued.
1: ADC1 Data Buffer is full, and the DMA has not written previous data to XRAM. This bit must be cleared by software.

Bit 0: DMA0DO0: ADC0 Data Overflow Warning Flag.
0: No ADC0 Data Buffer Warnings have been issued.
1: ADC0 Data Buffer is full, and the DMA has not written previous data to XRAM. This bit must be cleared by software.

Figure 6.8. DMA0BND: DMA0 Instruction Boundary Register

SFR Page: 3
SFR Address: 0xFD

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-							00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7-6: Unused.
Bits 5-0: DMA0 instruction address to begin with when executing DMA instructions.

Figure 6.9. DMA0ISW: DMA0 Instruction Status Register

SFR Page: 3
SFR Address: 0xFE

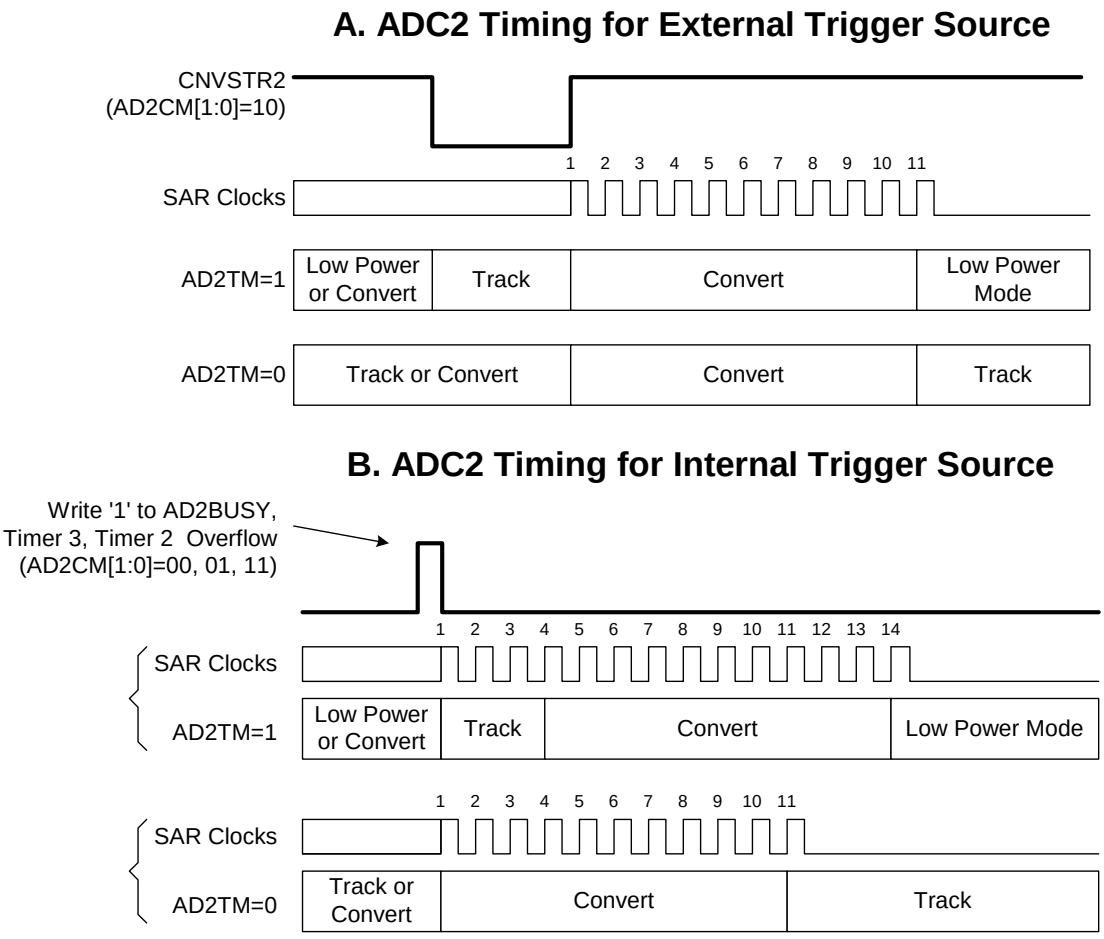
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-							00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7-6: Unused.
Bits 5-0: Contains the address of the current DMA0 Instruction to be executed.

7.2.2. Tracking Modes

The AD2TM bit in register ADC2CN controls the ADC2 track-and-hold mode. In its default state, the ADC2 input is continuously tracked, except when a conversion is in progress. When the AD2TM bit is logic 1, ADC2 operates in low-power track-and-hold mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR2 signal is used to initiate conversions in low-power tracking mode, ADC2 tracks only when CNVSTR2 is low; conversion begins on the rising edge of CNVSTR2 (see Figure 7.3). Tracking can also be disabled (shutdown) when the device is in low power standby or sleep modes. Low-power track-and-hold mode is also useful when AMUX settings are frequently changed, due to the settling time requirements described in Section "7.2.3. Settling Time Requirements" on page 91.

Figure 7.3. 10-Bit ADC Track and Conversion Example Timing



7.2.3. Settling Time Requirements

A minimum tracking time is required before an accurate conversion can be performed. This tracking time is determined by the AMUX2 resistance, the ADC2 sampling capacitance, any external source resistance, and the accuracy required for the conversion. Note that in low-power tracking mode, three SAR clocks are used for tracking at the start of every conversion. For most applications, these three SAR clocks will meet the minimum tracking time requirements.

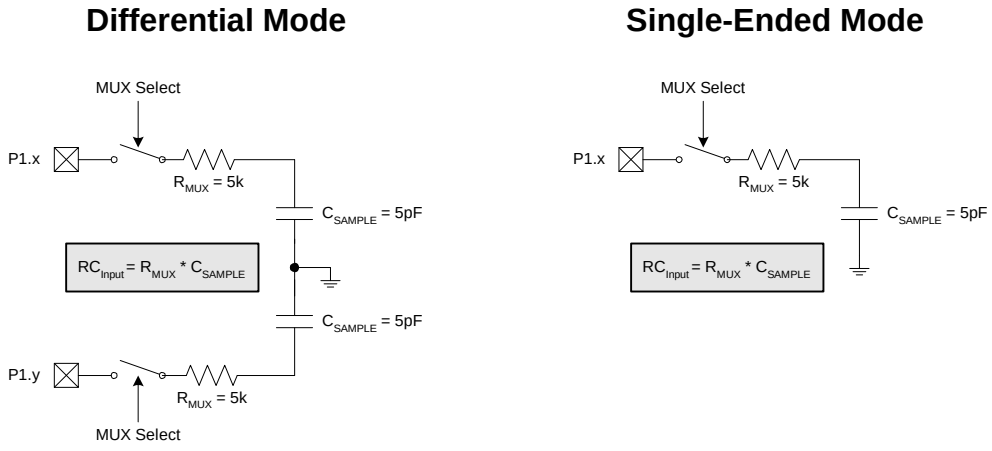
Figure 7.4 shows the equivalent ADC2 input circuits for both Differential and Single-ended modes. Notice that the equivalent time constant for both input circuits is the same. The required ADC2 settling time for a given settling accuracy (SA) may be approximated by Equation 7.1. When measuring the Temperature Sensor output, R_{TOTAL} reduces to R_{MUX}. See Table 7.1 for ADC2 minimum settling time requirements.

Equation 7.1. ADC2 Settling Time Requirements

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required settling time in seconds
R_{TOTAL} is the sum of the AMUX2 resistance and any external source resistance.
n is the ADC resolution in bits (10).

Figure 7.4. ADC2 Equivalent Input Circuits



7.3.2. Window Detector In Differential Mode

Figure 7.17 shows two example window comparisons for right-justified, differential data, with ADC2LTH:ADC2LTL = 0x0040 (+64d) and ADC2GTH:ADC2GTH = 0xFFFF (-1d). In differential mode, the measurable voltage between the input pins is between -VREF and VREF*(511/512). Output codes are represented as 10-bit 2's complement signed integers. In the left example, an AD2WINT interrupt will be generated if the ADC2 conversion word (ADC2H:ADC2L) is within the range defined by ADC2GTH:ADC2GTL and ADC2LTH:ADC2LTL (if 0xFFFF (-1d) < ADC2H:ADC2L < 0x0040 (64d)). In the right example, an AD2WINT interrupt will be generated if the ADC2 conversion word is outside of the range defined by the ADC2GT and ADC2LT registers (if ADC2H:ADC2L < 0xFFFF (-1d) or ADC2H:ADC2L > 0x0040 (+64d)). Figure 7.18 shows an example using left-justified data with the same comparison values.

Figure 7.17. ADC Window Compare Example: Right-Justified Differential Data

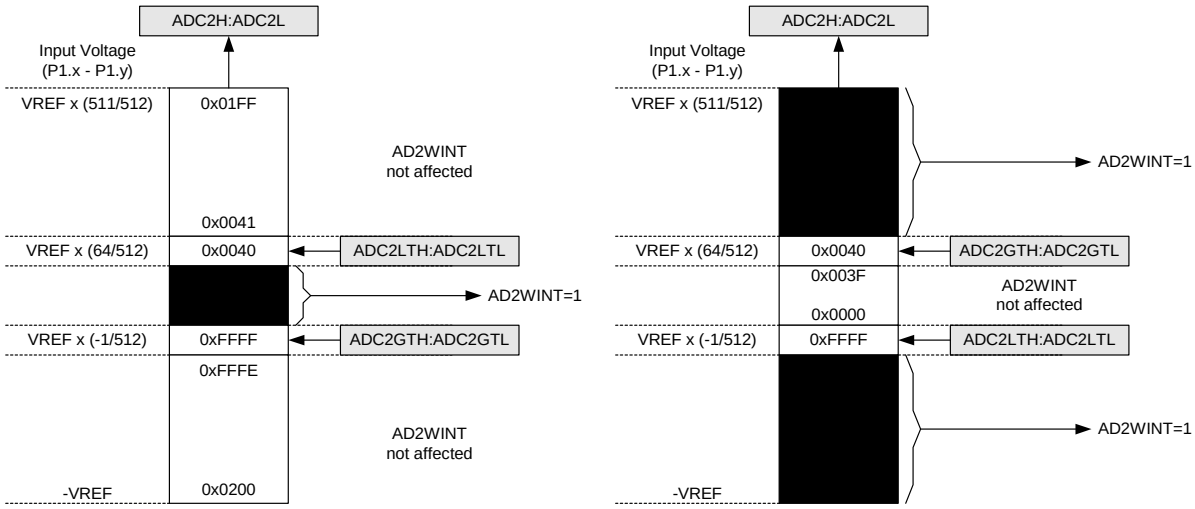
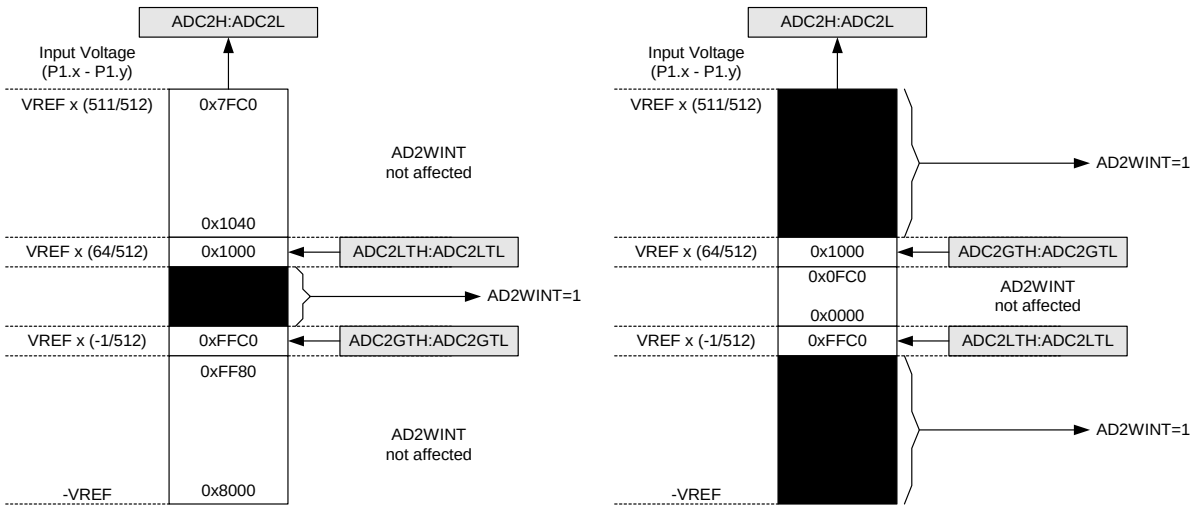


Figure 7.18. ADC Window Compare Example: Left-Justified Differential Data



and each CALL pushes two record bits onto the register. (A POP or decrement SP pops one record bit, and a RET pops two record bits, also.) The stack record circuitry can also detect an overflow or underflow on the 32-bit shift register, and can notify the debug software even with the MCU running at speed.

13.2.6. Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the Special Function Registers (SFRs). The SFRs provide control and data exchange with the CIP-51's resources and peripherals. The CIP-51 duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the MCU. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set. Table 13.2 lists the SFRs implemented in the CIP-51 System Controller.

The SFRs are accessed whenever the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g. P0, TCON, P1, SCON, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided. Refer to the corresponding pages of the datasheet, as indicated in Table 13.3, for a detailed description of each register.

13.2.6.1.SFR Paging

The CIP-51 features SFR paging, allowing the device to map many SFRs into the 0x80 to 0xFF memory address space. The SFR memory space has 256 pages. In this way, each memory location from 0x80 to 0xFF can access up to 256 SFRs. The C8051F06x family of devices utilizes five SFR pages: 0, 1, 2, 3, and F. SFR pages are selected using the Special Function Register Page Selection register, SFRPAGE (see Figure 13.10). The procedure for reading and writing an SFR is as follows:

1. Select the appropriate SFR page number using the SFRPAGE register.
2. Use direct accessing mode to read or write the special function register (MOV instruction).

13.2.6.2.Interrupts and SFR Paging

When an interrupt occurs, the SFR Page Register will automatically switch to the SFR page containing the flag bit that caused the interrupt. The automatic SFR Page switch function conveniently removes the burden of switching SFR pages from the interrupt service routine. Upon execution of the RETI instruction, the SFR page is automatically restored to the SFR Page in use prior to the interrupt. This is accomplished via a three-byte SFR Page Stack. The top byte of the stack is SFRPAGE, the current SFR Page. The second byte of the SFR Page Stack is SFRNEXT. The third, or bottom byte of the SFR Page Stack is SFRLAST. On interrupt, the current SFRPAGE value is pushed to the SFRNEXT byte, and the value of SFRNEXT is pushed to SFRLAST. Hardware then loads SFRPAGE with the SFR Page containing the flag bit associated with the interrupt. On a return from interrupt, the SFR Page Stack is popped resulting in the value of SFRNEXT returning to the SFRPAGE register, thereby restoring the SFR page context without software intervention. The value in SFRLAST (0x00 if there is no SFR Page value in the bottom of the stack) of the stack is placed in SFRNEXT register. If desired, the values stored in SFRNEXT and SFRLAST may be modified during an interrupt, enabling the CPU to return to a different SFR Page upon execution of the RETI instruction (on interrupt exit). Modifying registers in the SFR Page Stack does not cause a push or pop of the stack. Only interrupt calls and returns will cause push/pop operations on the SFR Page Stack.

Figure 13.16. PSW: Program Status Word

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CY	AC	F0	RS1	RS0	OV	F1	PARITY	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xD0
SFR Page: All Pages

Bit7: CY: Carry Flag.
This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to 0 by all other arithmetic operations.

Bit6: AC: Auxiliary Carry Flag.
This bit is set when the last arithmetic operation resulted in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to 0 by all other arithmetic operations.

Bit5: F0: User Flag 0.
This is a bit-addressable, general purpose flag for use under software control.

Bits4-3: RS1-RS0: Register Bank Select.
These bits select which register bank is used during register accesses.

RS1	RS0	Register Bank	Address
0	0	0	0x00 - 0x07
0	1	1	0x08 - 0x0F
1	0	2	0x10 - 0x17
1	1	3	0x18 - 0x1F

Bit2: OV: Overflow Flag.
This bit is set to 1 under the following circumstances:
- An ADD, ADDC, or SUBB instruction causes a sign-change overflow.
- A MUL instruction results in an overflow (result is greater than 255).
- A DIV instruction causes a divide-by-zero condition.

The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.

Bit1: F1: User Flag 1.
This is a bit-addressable, general purpose flag for use under software control.

Bit0: PARITY: Parity Flag.
This bit is set to 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

Figure 13.17. ACC: Accumulator

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xE0
SFR Page: All Pages

Bits7-0: ACC: Accumulator.
This register is the accumulator for arithmetic operations.

Figure 13.18. B: B Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xF0
SFR Page: All Pages

Bits7-0: B: B Register.
This register serves as a second accumulator for certain arithmetic operations.

15.4. External Crystal Example

If a crystal or ceramic resonator is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 15.1, Option 1. The External Oscillator Frequency Control value (XFCN) should be chosen from the Crystal column of the table in Figure 15.5 (OSCXCN register). For example, an 11.0592 MHz crystal requires an XFCN setting of 111b.

When the crystal oscillator is enabled, the oscillator amplitude detection circuit requires a settle time to achieve proper bias. Introducing a blanking interval of at least 1 ms between enabling the oscillator and checking the XTLVLD bit will prevent a premature switch to the external oscillator as the system clock. Switching to the external oscillator before the crystal oscillator has stabilized can result in unpredictable behavior. The recommended procedure is:

Step 1. Enable the external oscillator.
Step 2. Wait at least1 ms.
Step 3. Poll for XTLVLD => '1'.
Step 4. Switch the system clock to the external oscillator.

Important Note on External Crystals: Crystal oscillator circuits are quite sensitive to PCB layout and external noise. The crystal should be placed as close as possible to the XTAL pins on the device. The traces should be as short as possible and shielded with ground plane from any other traces which could introduce noise or interference. Crystal loading capacitors should be referenced to AGND.

15.5. External RC Example

If an RC network is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 15.1, Option 2. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, first select the RC network value to produce the desired frequency of oscillation. If the frequency desired is 100 kHz, let R = 246 kΩ and C = 50 pF:

$f = 1.23(10^3) / RC = 1.23 (10^3) / [246 * 50] = 0.1 \text{ MHz} = 100 \text{ kHz}$
Referring to the table in Figure 15.5, the required XFCN setting is 010.

15.6. External Capacitor Example

If a capacitor is used as an external oscillator for the MCU, the circuit should be configured as shown in Figure 15.1, Option 3. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, select the capacitor to be used and find the frequency of oscillation from the equations below. Assume VDD = 3.0 V and C = 50 pF:

$f = KF / (C * VDD) = KF / (50 * 3)$
$f = KF / 150$

If a frequency of roughly 50 kHz is desired, select the K Factor from the table in Figure 15.5 as KF = 7.7:

f = 7.7 / 150 = 0.051 MHz, or 51 kHz

Therefore, the XFCN value to use in this example is 010.

18.1. Ports 0 through 3 and the Priority Crossbar Decoder

The Priority Crossbar Decoder, or “Crossbar”, allocates and assigns Port pins on Port 0 through Port 3 to the digital peripherals (UARTs, SMBus, PCA, Timers, etc.) on the device using a priority order. The Port pins are allocated in order starting with P0.0 and continue through P3.7 (on the C8051F060/2/4/6) or P2.7 (on the C8051F061/3/5/7) if necessary. The digital peripherals are assigned Port pins in a priority order which is listed in Figure 18.3, with UART0 having the highest priority and CNVSTR2 having the lowest priority.

18.1.1. Crossbar Pin Assignment and Allocation

The Crossbar assigns Port pins to a peripheral if the corresponding enable bits of the peripheral are set to a logic 1 in the Crossbar configuration registers XBR0, XBR1, XBR2, and XBR3, shown in Figure 18.5, Figure 18.6, Figure 18.7, and Figure 18.8. For example, if the UART0EN bit (XBR0.2) is set to a logic 1, the TX0 and RX0 pins will be mapped to P0.0 and P0.1 respectively. Because UART0 has the highest priority, its pins will always be mapped to P0.0 and P0.1 when UART0EN is set to a logic 1. If a digital periph-

Figure 18.3. Priority Crossbar Decode Table

(P1MDIN = 0xFF; P2MDIN = 0xFF)

	P0								P1								P2								P3								Crossbar Register Bits
PIN I/O	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
TX0	●																																UART0EN: XBR0.2
RX0		●																															
SCK	●		●																														SPI0EN: XBR0.1
MISO		●		●																													
MOSI			●		●																												
NSS				●		●			NSS is not assigned to a port pin when the SPI is placed in 3-wire mode																							
SDA	●		●	●	●	●	●																										SMB0EN: XBR0.0
SCL		●		●	●	●	●	●																									
TX1	●		●	●	●	●	●	●	●																								UART1EN: XBR2.2
RX1		●		●	●	●	●	●	●	●																							
CEX0	●		●	●	●	●	●	●	●	●	●																						PCA0ME: XBR0.[5:3]
CEX1		●		●	●	●	●	●	●	●	●	●																					
CEX2			●		●	●	●	●	●	●	●	●	●																					
CEX3				●		●	●	●	●	●	●	●	●	●																				
CEX4					●		●	●	●	●	●	●	●	●	●																			
CEX5						●		●	●	●	●	●	●	●	●	●																		
ECI	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●																ECI0E: XBR0.6
CP0	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●															CP0E: XBR0.7
CP1	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●														CP1E: XBR1.0
CP2	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●													CP2E: XBR3.3
T0	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●												T0E: XBR1.1
/INT0	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●											INT0E: XBR1.2
T1	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●										T1E: XBR1.3
/INT1	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●									INT1E: XBR1.4
T2	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●								T2E: XBR1.5
T2EX	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●							T2EXE: XBR1.6
T3	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●						T3E: XBR3.0
T3EX	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●					T3EXE: XBR3.1
T4	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●				T4E: XBR2.3
T4EX	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●			T4EXE: XBR2.4
/SYSCLK	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●		SYSCKE: XBR1.7
CNVSTR2	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	CNVSTE2: XBR3.2
									AIN2.0	AIN2.1	AIN2.2	AIN2.3	AIN2.4	AIN2.5	AIN2.6	AIN2.7				CP1+	CP1-	CP2+	CP2-	CP0+	CP0-									

Figure 18.7. XBR2: Port I/O Crossbar Register 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
WEAKPUD	XBARE	-	T4EXE	T4E	UART1E	-	-	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE3
SFR Page: F

Bit7: WEAKPUD: Weak Pull-Up Disable Bit.
0: Weak pull-ups globally enabled.
1: Weak pull-ups globally disabled.
Bit6: XBARE: Crossbar Enable Bit.
0: Crossbar disabled. All pins on Ports 0, 1, 2, and 3, are forced to Input mode.
1: Crossbar enabled.
Bit5: UNUSED. Read = 0, Write = don't care.
Bit4: T4EXE: T4EX Input Enable Bit.
0: T4EX unavailable at Port pin.
1: T4EX routed to Port pin.
Bit3: T4E: T4 Input Enable Bit.
0: T4 unavailable at Port pin.
1: T4 routed to Port pin.
Bit2: UART1E: UART1 I/O Enable Bit.
0: UART1 I/O unavailable at Port pins.
1: UART1 TX and RX routed to 2 Port pins.
Bits1-0: Reserved

Figure 18.9. P0: Port0 Data Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x80
SFR Page: All Pages

Bits7-0: P0.[7:0]: Port0 Output Latch Bits.
(Write - Output appears on I/O pins per XBR0, XBR1, XBR2, and XBR3 Registers)
0: Logic Low Output.
1: Logic High Output (open if corresponding P0MDOUT.n bit = 0).
(Read - Regardless of XBR0, XBR1, XBR2, and XBR3 Register settings).
0: P0.n pin is logic low.
1: P0.n pin is logic high.

Figure 18.10. P0MDOUT: Port0 Output Mode Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA4
SFR Page: F

Bits7-0: P0MDOUT.[7:0]: Port0 Output Mode Bits.
0: Port Pin output mode is configured as Open-Drain.
1: Port Pin output mode is configured as Push-Pull.

Note: SDA, SCL, and RX0 (when UART0 is in Mode 0) and RX1 (when UART1 is in Mode 0) are always configured as Open-Drain when they appear on Port pins.