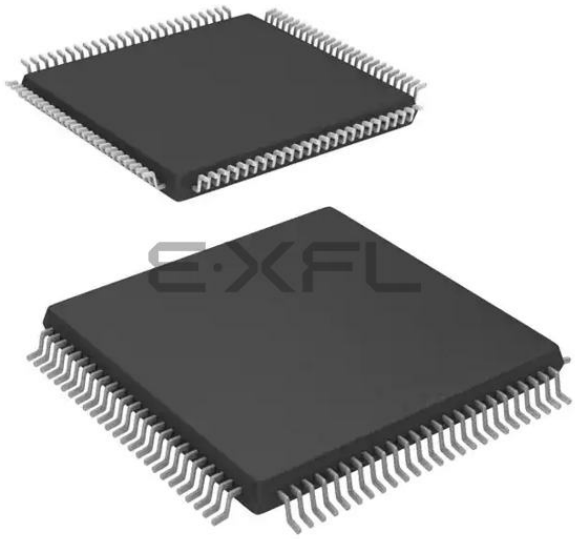

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	59
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f064r

Table 4.1. Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	F060	F061	F064	F065		
	F062	F063	F066	F067		
VRGND0	20	14	20	14	A In	ADC0 Voltage Reference Ground. This pin should be grounded if using the ADC.
VBGAP0	22	16	22	16	A Out	ADC0 Bandgap Bypass Pin.
VREF1	6	2	6	2	A I/O	Bandgap Voltage Reference Output for ADC1. ADC1 Voltage Reference Input.
VRGND1	7	3	7	3	A In	ADC1 Voltage Reference Ground. This pin should be grounded if using the ADC.
VBGAP1	5	1	5	1	A Out	ADC1 Bandgap Bypass Pin.
VREF2	2				A In	ADC2 Voltage Reference Input.
		62			A In	ADC2, DAC0, and DAC1 Voltage Reference Input.
VREFD	3				A In	DAC0 and DAC1 Voltage Reference Input.
AIN0	18	12	18	12	A In	ADC0 Signal Input (See ADC0 Specification for complete description).
AIN0G	19	13	19	13	A In	ADC0 DC Bias Input (See ADC0 Specification for complete description).
AIN1	9	5	9	5	A In	ADC1 Signal Input (See ADC1 Specification for complete description).
AIN1G	8	4	8	4	A In	ADC1 DC Bias Input (See ADC1 Specification for complete description).
CNVSTR0	15	9	15	9	D In	External Conversion Start Source for ADC0
CNVSTR1	12	8	12	8	D In	External Conversion Start Source for ADC1
CANTX	94	59			D Out	Controller Area Network Transmit Output.
CANRX	95	60			D In	Controller Area Network Receive Input.
DAC0	25	17			A Out	Digital to Analog Converter 0 Voltage Output. (See DAC Specification for complete description).
DAC1	1	64			A Out	Digital to Analog Converter 1 Voltage Output. (See DAC Specification for complete description).
P0.0	62	51	62	51	D I/O	Port 0.0. See Port Input/Output section for complete description.
P0.1	61	50	61	50	D I/O	Port 0.1. See Port Input/Output section for complete description.
P0.2	60	49	60	49	D I/O	Port 0.2. See Port Input/Output section for complete description.
P0.3	59	48	59	48	D I/O	Port 0.3. See Port Input/Output section for complete description.
P0.4	58	47	58	47	D I/O	Port 0.4. See Port Input/Output section for complete description.

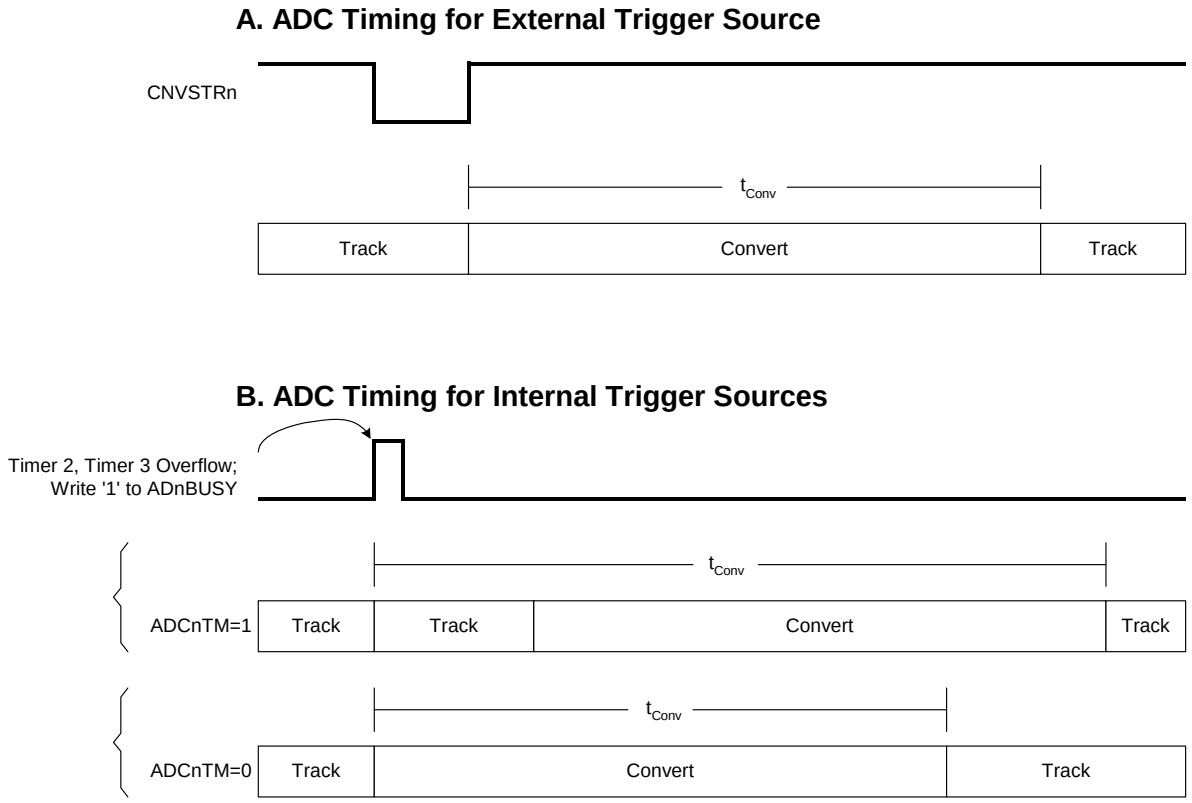


Figure 5.4. ADC Track and Conversion Example Timing

Table 5.1. Conversion Timing (t_{Conv})

ADnSC3-0	ADCnTM = 0	ADCnTM = 1	ADnSC3-0	ADCnTM = 0	ADCnTM = 1
0000	21*t_{SYSCLK}	38*t_{SYSCLK}	1000	171*t_{SYSCLK}	315*t_{SYSCLK}
0001	40*t_{SYSCLK}	72*t_{SYSCLK}	1001	189*t_{SYSCLK}	349*t_{SYSCLK}
0010	58*t_{SYSCLK}	106*t_{SYSCLK}	1010	208*t_{SYSCLK}	384*t_{SYSCLK}
0011	78*t_{SYSCLK}	142*t_{SYSCLK}	1011	226*t_{SYSCLK}	418*t_{SYSCLK}
0100	97*t_{SYSCLK}	177*t_{SYSCLK}	1100	245*t_{SYSCLK}	453*t_{SYSCLK}
0101	115*t_{SYSCLK}	211*t_{SYSCLK}	1101	263*t_{SYSCLK}	487*t_{SYSCLK}
0110	134*t_{SYSCLK}	246*t_{SYSCLK}	1110	282*t_{SYSCLK}	522*t_{SYSCLK}
0111	152*t_{SYSCLK}	280*t_{SYSCLK}	1111	300*t_{SYSCLK}	556*t_{SYSCLK}

Figure 5.15. ADC0 Data Word Example

16-bit ADC0 Data Word appears in the ADC0 Data Word Registers as follows:

Example: ADC0 Data Word Conversion Map, AIN0 Input in Single-Ended Mode (AMX0SL = 0x00)

AIN0-AIN0G (Volts)	**ADC0H:ADC0L**
VREF * (65535/65536)	0xFFFF
VREF / 2	0x8000
VREF * (32767/65536)	0x7FFF
0	0x0000

Example: ADC0 Data Word Conversion Map, AIN0-AIN1 Differential Input Pair (AMX0SL = 0x40)

AIN0-AIN1 (Volts)	**ADC0H:ADC0L**
VREF * (32767/32768)	0x7FFF
VREF / 2	0x4000
VREF * (1/32768)	0x0001
0	0x0000
-VREF * (1/32768)	0xFFFF
-VREF / 2	0xC000
-VREF	0x8000

$$Code = Vin \times \frac{Gain}{VREF} \times 2^n$$; 'n' = 16 for Single-Ended; 'n'=15 for Differential.

Figure 7.6. AMX2SL: AMUX2 Channel Select Register

SFR Page: 2
SFR Address: 0xBB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AMX2AD3	AMX2AD2	AMX2AD1	AMX2AD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7-4: UNUSED. Read = 0000b; Write = don't care.
Bits 3-0: AMX2AD3-0: AMX2 Address Bits.
0000-1111b: ADC input multiplexer channel selected per chart below.

AMX2AD3-0	Single-Ended Measurement		AMX2AD3-0	Differential Measurement	
0000	AIN2.0	AIN01IC = 0	0000	+(AIN2.0) -(AIN2.1)	AIN01IC = 1
0001	AIN2.1		0001	+(AIN2.1) -(AIN2.0)	
0010	AIN2.2	AIN23IC = 0	0010	+(AIN2.2) -(AIN2.3)	AIN23IC = 1
0011	AIN2.3		0011	+(AIN2.3) -(AIN2.2)	
0100	AIN2.4	AIN45IC = 0	0100	+(AIN2.4) -(AIN2.5)	AIN45IC = 1
0101	AIN2.5		0101	+(AIN2.5) -(AIN2.4)	
0110	AIN2.6	AIN67IC = 0	0110	+(AIN2.6) -(AIN2.7)	AIN67IC = 1
0111	AIN2.7		0111	+(AIN2.7) -(AIN2.6)	
1xxx	Temperature Sensor		1xxx	-	

Table 7.1. ADC2 Electrical Characteristics

VDD = 3.0 V, VREF = 2.40 V (REFSL=0), PGA Gain = 1, -40°C to +85°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			10		bits
Integral Nonlinearity			±0.5	±1	LSB
Differential Nonlinearity	Guaranteed Monotonic		±0.5	±1	LSB
Offset Error		-12	1	12	LSB
Full Scale Error	Differential mode	-15	-5	5	LSB
Offset Temperature Coefficient			3.6		ppm/°C
DYNAMIC PERFORMANCE (10 kHz sine-wave Differential input, 1 dB below Full Scale, 200 ksps)					
Signal-to-Noise Plus Distortion		53	55.5		dB
Total Harmonic Distortion	Up to the 5th harmonic		-67		dB
Spurious-Free Dynamic Range			78		dB
Conversion Rate					
SAR Conversion Clock				3	MHz
Conversion Time in SAR Clocks		10			clocks
Track/Hold Acquisition Time		300			ns
Throughput Rate				200	ksps
Analog Inputs					
ADC Input Voltage Range	Single Ended (AIN+ - AGND) Differential (AIN+ - AIN-)	0 -VREF		VREF VREF	V V
Absolute Pin Voltage with respect to AGND	Single Ended or Differential	0		AV+	V
Input Capacitance			5		pF
Temperature Sensor					
Linearity			±0.2		°C
Offset	Temp = 0 °C		776		mV
Offset Error (Note 1)	Temp = 0 °C		±8.9		mV
Slope			2.89		mV/°C
Slope Error (Note 1)			±63		µV/°C
Power Specifications					
Power Supply Current (VDD supplied to ADC2)	Operating Mode, 200 ksps		400	900	µA
Power Supply Rejection			±0.3		mV/V
Note 1: Represents one standard deviation from the mean value.					

Figure 8.4. DAC0CN: DAC0 Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
DAC0EN	-	-	DAC0MD1	DAC0MD0	DAC0DF2	DAC0DF1	DAC0DF0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD4
SFR Page: 0

Bit7: DAC0EN: DAC0 Enable Bit.
0: DAC0 Disabled. DAC0 Output pin is disabled; DAC0 is in low-power shutdown mode.
1: DAC0 Enabled. DAC0 Output pin is active; DAC0 is operational.

Bits6-5: UNUSED. Read = 00b; Write = don't care.

Bits4-3: DAC0MD1-0: DAC0 Mode Bits.
00: DAC output updates occur on a write to DAC0H.
01: DAC output updates occur on Timer 3 overflow.
10: DAC output updates occur on Timer 4 overflow.
11: DAC output updates occur on Timer 2 overflow.

Bits2-0: DAC0DF2-0: DAC0 Data Format Bits:

000: The most significant nibble of the DAC0 Data Word is in DAC0H[3:0], while the least significant byte is in DAC0L.

DAC0H								DAC0L							
				MSB											LSB

001: The most significant 5-bits of the DAC0 Data Word is in DAC0H[4:0], while the least significant 7-bits are in DAC0L[7:1].

DAC0H								DAC0L							
			MSB											LSB	

010: The most significant 6-bits of the DAC0 Data Word is in DAC0H[5:0], while the least significant 6-bits are in DAC0L[7:2].

DAC0H								DAC0L							
		MSB											LSB		

011: The most significant 7-bits of the DAC0 Data Word is in DAC0H[6:0], while the least significant 5-bits are in DAC0L[7:3].

DAC0H								DAC0L							
	MSB											LSB			

1xx: The most significant 8-bits of the DAC0 Data Word is in DAC0H[7:0], while the least significant 4-bits are in DAC0L[7:4].

DAC0H								DAC0L							
MSB											LSB				

Figure 12.3. CPTnCN: Comparator 0, 1, and 2 Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CPnEN	CPnOUT	CPnRIF	CPnFIF	CPnHYP1	CPnHYP0	CPnHYN1	CPnHYN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: CPT0CN: 0x88; CPT1CN: 0x88; CPT2CN: 0x88
SFR Pages: CPT0CN: page 1; CPT1CN: page 2; CPT2CN: page 3

Bit7: CPnEN: Comparator Enable Bit. **(Please see note below.)**
0: Comparator Disabled.
1: Comparator Enabled.

Bit6: CPnOUT: Comparator Output State Flag.
0: Voltage on CPn+ < CPn-.
1: Voltage on CPn+ > CPn-.

Bit5: CPnRIF: Comparator Rising-Edge Interrupt Flag.
0: No Comparator Rising Edge Interrupt has occurred since this flag was last cleared.
1: Comparator Rising Edge Interrupt has occurred. Must be cleared by software.

Bit4: CPnFIF: Comparator Falling-Edge Interrupt Flag.
0: No Comparator Falling-Edge Interrupt has occurred since this flag was last cleared.
1: Comparator Falling-Edge Interrupt has occurred. Must be cleared by software.

Bits3-2: CPnHYP1-0: Comparator Positive Hysteresis Control Bits.
00: Positive Hysteresis Disabled.
01: Positive Hysteresis = 5 mV.
10: Positive Hysteresis = 10 mV.
11: Positive Hysteresis = 20 mV.

Bits1-0: CPnHYN1-0: Comparator Negative Hysteresis Control Bits.
00: Negative Hysteresis Disabled.
01: Negative Hysteresis = 5 mV.
10: Negative Hysteresis = 10 mV.
11: Negative Hysteresis = 20 mV.

NOTE: Upon enabling a comparator, the output of the comparator is not immediately valid. Before using a comparator as an interrupt or reset source, software should wait for a minimum of the specified “Power-up time” as specified in Table 12.1, “Comparator Electrical Characteristics,” on page 122.

Figure 13.11. SFRNEXT: SFR Next Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x85
SFR Page: All Pages

Bits7-0: SFR Page Stack Bits: SFR page context is retained upon interrupts/return from interrupts in a 3 byte SFR Page Stack: SFRPAGE is the first entry, SFRNEXT is the second, and SFR-LAST is the third entry. The SFR stack bytes may be used to alter the context in the SFR Page Stack, and will not cause the stack to ‘push’ or ‘pop’. Only interrupts and return from interrupt cause push and pop the SFR Page Stack.
Write: Sets the SFR Page contained in the second byte of the SFR Stack. This will cause the SFRPAGE SFR to have this SFR page value upon a return from interrupt.
Read: Returns the value of the SFR page contained in the second byte of the SFR stack. This is the value that will go to the SFR Page register upon a return from interrupt.

Figure 13.12. SFRLAST: SFR Last Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

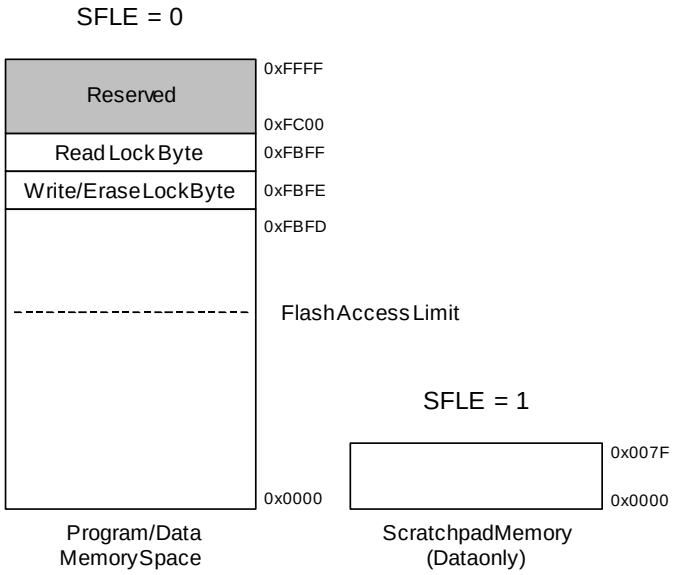
SFR Address: 0x86
SFR Page: All Pages

Bits7-0: SFR Page Stack Bits: SFR page context is retained upon interrupts/return from interrupts in a 3 byte SFR Page Stack: SFRPAGE is the first entry, SFRNEXT is the second, and SFR-LAST is the third entry. The SFR stack bytes may be used to alter the context in the SFR Page Stack, and will not cause the stack to ‘push’ or ‘pop’. Only interrupts and return from interrupt cause push and pop the SFR Page Stack.
Write:
Sets the SFR Page in the last entry of the SFR Stack. This will cause the SFRNEXT SFR to have this SFR page value upon a return from interrupt.
Read:
Returns the value of the SFR page contained in the last entry of the SFR stack.

Figure 16.1. C8051F060/1/2/3/4/5 Flash Program Memory Map and Security Bytes

Read and Write/Erase Security Bits
(Bit 7 is MSB)

Bit	Memory Block
7	0xE000-0xFBFD
6	0xC000-0xDFFF
5	0xA000-0xBFFF
4	0x8000-0x9FFF
3	0x6000-0x7FFF
2	0x4000-0x5FFF
1	0x2000-0x3FFF
0	0x0000-0x1FFF



Flash Read Lock Byte

Bits7-0: Each bit locks a corresponding block of memory. (Bit7 is MSB).

0: Read operations are locked (disabled) for corresponding block across the JTAG interface.

1: Read operations are unlocked (enabled) for corresponding block across the JTAG interface.

Flash Write/Erase Lock Byte

Bits7-0: Each bit locks a corresponding block of memory.

0: Write/Erase operations are locked (disabled) for corresponding block across the JTAG interface.

1: Write/Erase operations are unlocked (enabled) for corresponding block across the JTAG interface.

NOTE: When the block containing the security bytes is locked, the security bytes may be written but not erased.

Flash Access Limit

The Flash Access Limit is defined by the setting of the FLACL register, as described in Figure 16.3. Firmware running at or above this address is prohibited from using the MOVX and MOVC instructions to read, write, or erase Flash locations below this address.

Table 17.1 lists the AC parameters for the External Memory Interface, and Figure 17.7 through Figure 17.12 show the timing diagrams for the different External Memory Interface modes and MOVX operations.

17.6.2.2.8-bit MOVX without Bank Select: EMI0CF[4:2] = ‘001’ or ‘011’.

Figure 17.11. Multiplexed 8-bit MOVX without Bank Select Timing

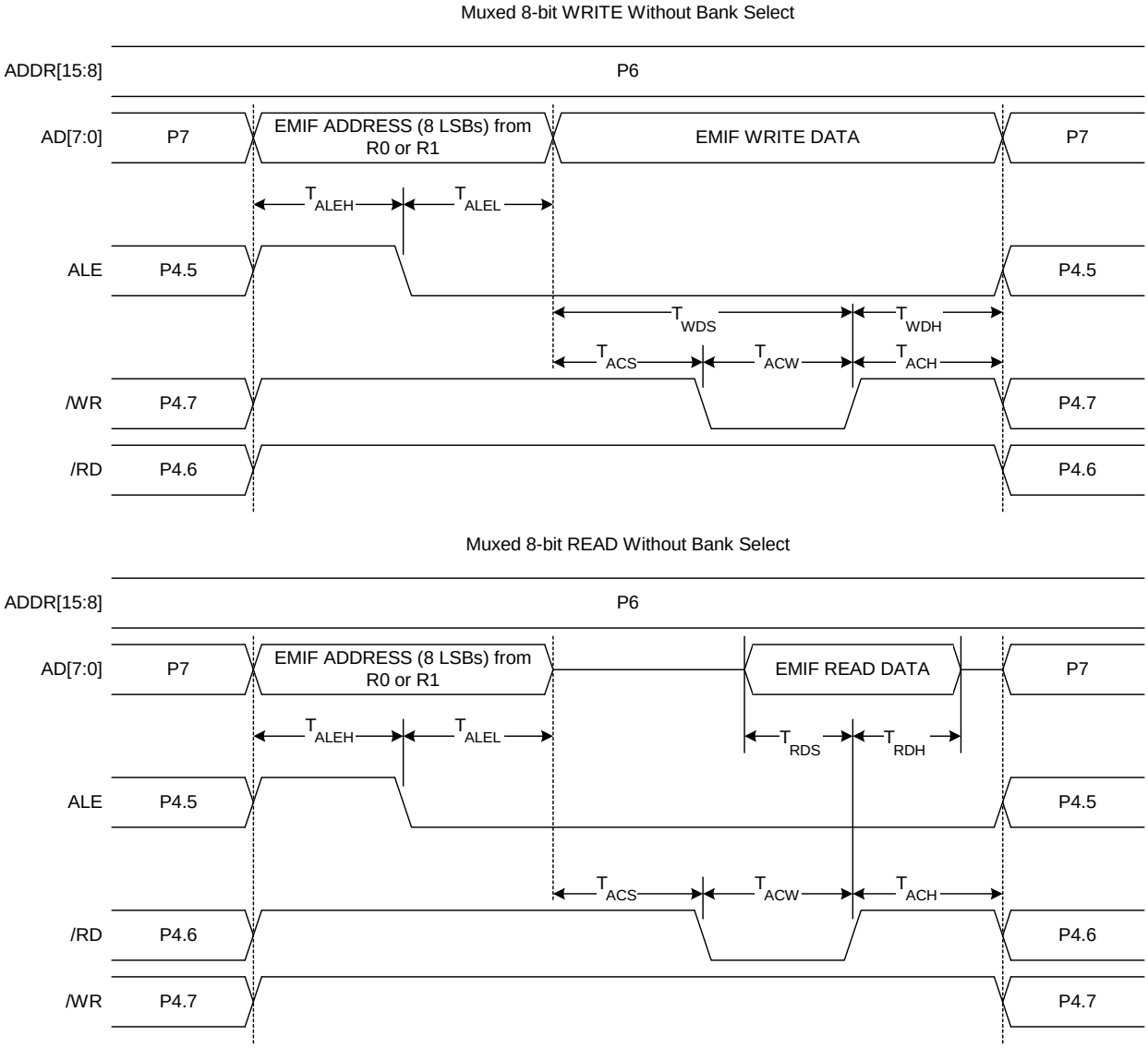


Figure 18.8. XBR3: Port I/O Crossbar Register 3

R	R	R	R/W	R/W	R/W	R/W	R/W	Reset Value
CTXOUT	-	-		CP2E	CNVST2E	T3EXE	T3E	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE4
SFR Page: F

Bit7: CTXOUT: CAN Transmit Pin (CTX) Output Mode.
0: CTX pin output mode is configured as open-drain.
1: CTX pin output mode is configured as push-pull.
Bit6-4: Reserved
Bit3: CP2E: CP2 Output Enable Bit.
0: CP2 unavailable at Port pin.
1: CP2 routed to Port pin.
Bit2: CNVST2E: ADC2 External Convert Start Input Enable Bit.
0: CNVST2 for ADC2 unavailable at Port pin.
1: CNVST2 for ADC2 routed to Port pin.
Bit1: T3EXE: T3EX Input Enable Bit.
0: T3EX unavailable at Port pin.
1: T3EX routed to Port pin.
Bit0: T3E: T3 Input Enable Bit.
0: T3 unavailable at Port pin.
1: T3 routed to Port pin.

18.2. Ports 4 through 7 (C8051F060/2/4/6 only)

All Port pins on Ports 4 through 7 can be accessed as General-Purpose I/O (GPIO) pins by reading and writing the associated Port Data registers (See Figure 18.19, Figure 18.21, Figure 18.23, and Figure 18.25), a set of SFRs which are byte-addressable. Note that Port 4 has only three pins: P4.5, P4.6, and P4.7. Note also that the Port 4, 5, 6, and 7 registers are located on SFR Page F. The SFRPAGE register must be set to 0x0F to access these Port registers.

A Read of a Port Data register (or Port bit) will always return the logic state present at the pin itself, regardless of whether the Crossbar has allocated the pin for peripheral use or not. An exception to this occurs during the execution of a *read-modify-write* instruction (ANL, ORL, XRL, CPL, INC, DEC, DJNZ, JBC, CLR, SETB, and the bitwise MOV write operation). During the *read* cycle of the *read-modify-write* instruction, it is the contents of the Port Data register, not the state of the Port pins themselves, which is read.

18.2.1. Configuring Ports which are not Pinned Out

Although P3, P4, P5, P6, and P7 are not brought out to pins on the C8051F061/3/5/7 devices, the Port Data registers are still present and can be used by software. Because the digital input paths also remain active, it is recommended that these pins not be left in a ‘floating’ state in order to avoid unnecessary power dissipation arising from the inputs floating to non-valid logic levels. This condition can be prevented by any of the following:

1. Leave the weak pull-up devices enabled by setting WEAKPUD (XBR2.7) to a logic 0.
2. Configure the output modes of P3, P4, P5, P6, and P7 to “Push-Pull” by writing 0xFF to the associated output mode register (PnMDOUT).
3. Force the output states of P3, P4, P5, P6, and P7 to logic 0 by writing zeros to the Port Data registers: P3 = 0x00, P4 = 0x00, P5 = 0x00, P6= 0x00, and P7 = 0x00.

18.2.2. Configuring the Output Modes of the Port Pins

The output mode of each port pin can be configured to be either Open-Drain or Push-Pull. In the Push-Pull configuration, a logic 0 in the associated bit in the Port Data register will cause the Port pin to be driven to GND, and a logic 1 will cause the Port pin to be driven to VDD. In the Open-Drain configuration, a logic 0 in the associated bit in the Port Data register will cause the Port pin to be driven to GND, and a logic 1 will cause the Port pin to assume a high-impedance state. The Open-Drain configuration is useful to prevent contention between devices in systems where the Port pin participates in a shared interconnection in which multiple outputs are connected to the same physical wire.

The output modes of the Port pins on Ports 4 through 7 are determined by the bits in their respective PnMDOUT Output Mode Registers. Each bit in PnMDOUT controls the output mode of its corresponding port pin (see Figure 18.20, Figure 18.22, Figure 18.24, and Figure 18.26). For example, to place Port pin 5.3 in push-pull mode (digital output), set P5MDOUT.3 to logic 1. All port pins default to open-drain mode upon device reset.

18.2.3. Configuring Port Pins as Digital Inputs

A Port pin is configured as a digital input by setting its output mode to “Open-Drain” and writing a logic 1 to the associated bit in the Port Data register. For example, P7.7 is configured as a digital input by setting P7MDOUT.7 to a logic 0 and P7.7 to a logic 1.

18.2.4. Weak Pull-ups

By default, each Port pin has an internal weak pull-up device enabled which provides a resistive connection (about 100 kΩ) between the pin and VDD. The weak pull-up devices can be globally disabled by writ-

21.5. Serial Clock Timing

Four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI0 Configuration Register (SPI0CFG). The CKPHA bit (SPI0CFG.5) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPI0CFG.4) selects between an active-high or active-low clock. Both master and slave devices must be configured to use the same clock phase and polarity. SPI0 should be disabled (by clearing the SPIEN bit, SPI0CN.0) when changing the clock phase or polarity. The clock and data line relationships for master mode are shown in Figure 21.5. For slave mode, the clock and data relationships are shown in Figure 21.6 and Figure 21.7. Note that CKPHA must be set to '0' on both the master and slave SPI when communicating between two of the following devices: C8051F04x, C8051F06x, C8051F12x, C8051F31x, C8051F32x, and C8051F33x

The SPI0 Clock Rate Register (SPI0CKR) as shown in Figure 21.10 controls the master mode serial clock frequency. This register is ignored when operating in slave mode. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency or 12.5 MHz, whichever is slower. When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS (in 4-wire slave mode), and the serial input data synchronously with the slave's system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the slave's system clock.

Figure 21.5. Master Mode Data/Clock Timing

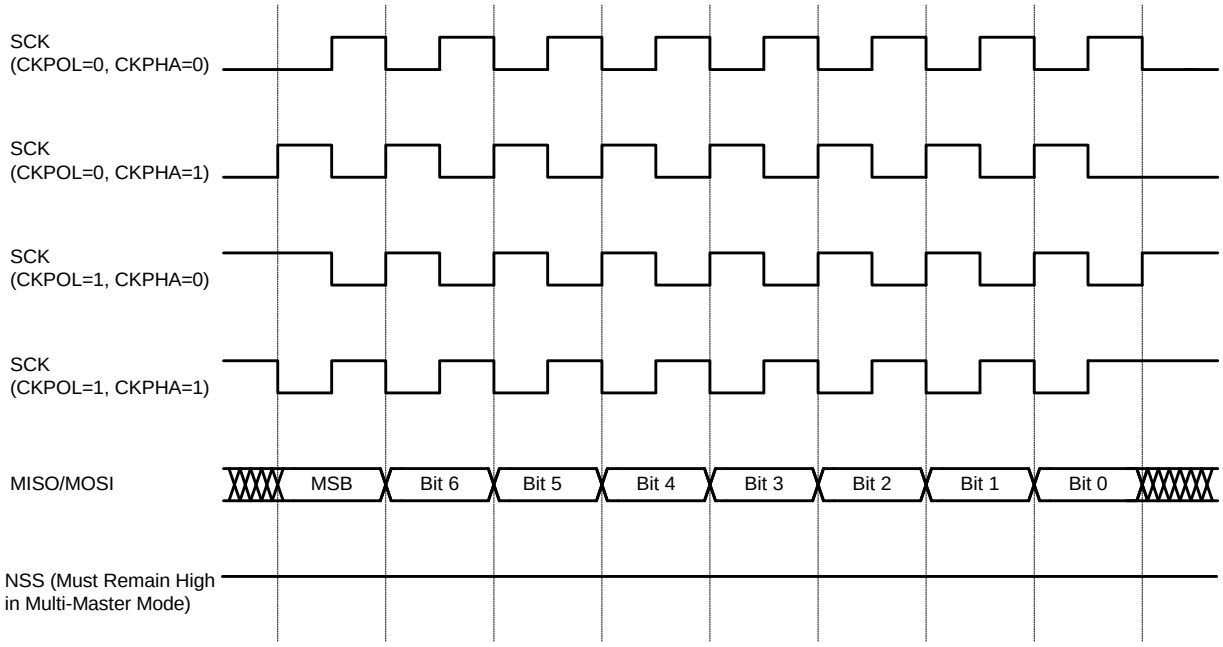


Figure 22.9. SSTA0: UART0 Status and Clock Selection Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
FE0	RXOV0	TXCOL0	SMOD0	S0TCLK1	S0TCLK0	S0RCLK1	S0RCLK0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x91
SFR Page: 0

Bit7: FE0: Frame Error Flag.†
This flag indicates if an invalid (low) STOP bit is detected.
0: Frame Error has not been detected.
1: Frame Error has been detected.

Bit6: RXOV0: Receive Overrun Flag.†
This flag indicates new data has been latched into the receive buffer before software has read the previous byte.
0: Receive overrun has not been detected.
1: Receive Overrun has been detected.

Bit5: TXCOL0: Transmit Collision Flag.†
This flag indicates user software has written to the SBUF0 register while a transmission is in progress.
0: Transmission Collision has not been detected.
1: Transmission Collision has been detected.

Bit4: SMOD0: UART0 Baud Rate Doubler Enable.
This bit enables/disables the divide-by-two function of the UART0 baud rate logic for configurations described in the UART0 section.
0: UART0 baud rate divide-by-two enabled.
1: UART0 baud rate divide-by-two disabled.

Bits3-2: UART0 Transmit Baud Rate Clock Selection Bits.

S0TCLK1	S0TCLK0	**Serial Transmit Baud Rate Clock Source**
0	0	Timer 1 generates UART0 TX Baud Rate
0	1	Timer 2 Overflow generates UART0 TX baud rate
1	0	Timer 3 Overflow generates UART0 TX baud rate
1	1	Timer 4 Overflow generates UART0 TX baud rate

Bits1-0: UART0 Receive Baud Rate Clock Selection Bits.

S0RCLK1	S0RCLK0	**Serial Receive Baud Rate Clock Source**
0	0	Timer 1 generates UART0 RX Baud Rate
0	1	Timer 2 Overflow generates UART0 RX baud rate
1	0	Timer 3 Overflow generates UART0 RX baud rate
1	1	Timer 4 Overflow generates UART0 RX baud rate

† Note: FE0, RXOV0, and TXCOL0 are flags only, and no interrupt is generated by these conditions.

25.1. PCA Counter/Timer

The 16-bit PCA counter/timer consists of two 8-bit SFRs: PCA0L and PCA0H. PCA0H is the high byte (MSB) of the 16-bit counter/timer and PCA0L is the low byte (LSB). Reading PCA0L automatically latches the value of PCA0H into a “snapshot” register; the following PCA0H read accesses this “snapshot” register. Reading the PCA0L Register first guarantees an accurate reading of the entire 16-bit PCA0 counter. Reading PCA0H or PCA0L does not disturb the counter operation. The CPS2-CPS0 bits in the PCA0MD register select the timebase for the counter/timer as shown in Table 25.1.

When the counter/timer overflows from 0xFFFF to 0x0000, the Counter Overflow Flag (CF) in PCA0MD is set to logic 1 and an interrupt request is generated if CF interrupts are enabled. Setting the ECF bit in PCA0MD to logic 1 enables the CF flag to generate an interrupt request. The CF bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software (Note: PCA0 interrupts must be globally enabled before CF interrupts are recognized. PCA0 interrupts are globally enabled by setting the EA bit (IE.7) and the EPCA0 bit in EIE1 to logic 1). Clearing the CIDL bit in the PCA0MD register allows the PCA to continue normal operation while the CPU is in Idle mode.

Table 25.1. PCA Timebase Input Options

CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)
1	0	0	System clock
1	0	1	External oscillator source divided by 8 (synchronized with system clock)

Figure 25.2. PCA Counter/Timer Block Diagram

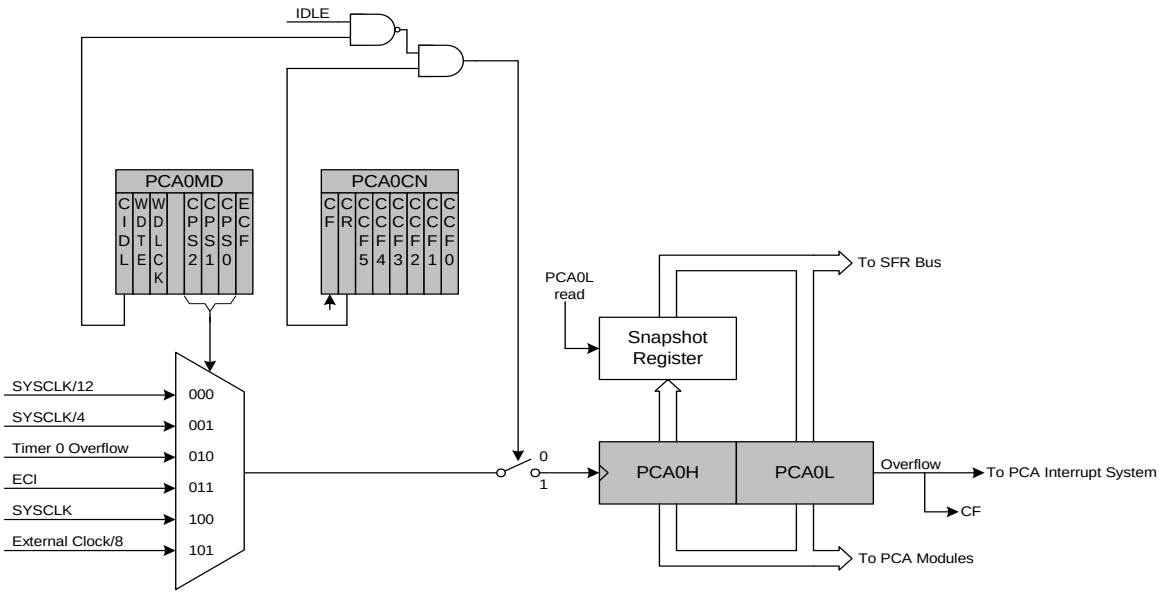


Figure 25.13. PCA0L: PCA0 Counter/Timer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF9
SFR Page: 0

Bits 7-0: PCA0L: PCA0 Counter/Timer Low Byte.
The PCA0L register holds the low byte (LSB) of the 16-bit PCA0 Counter/Timer.

Figure 25.14. PCA0H: PCA0 Counter/Timer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFA
SFR Page: 0

Bits 7-0: PCA0H: PCA0 Counter/Timer High Byte.
The PCA0H register holds the high byte (MSB) of the 16-bit PCA0 Counter/Timer.

26.1. Boundary Scan

The DR in the Boundary Scan path is a 126-bit shift register for the C8051F060/2/4/6 and a 118-bit shift register for the C8051F061/3/5/7. The Boundary DR provides control and observability of all the device pins as well as the SFR bus and Weak Pullup feature via the EXTEST and SAMPLE commands.

Table 26.1. Boundary Data Register Bit Definitions (C8051F060/2/4/6)

EXTEST provides access to both capture and update actions, while Sample only performs a capture.

Bit	Action	Target
0	Capture	Reset Enable from MCU
	Update	Reset Enable to /RST pin
1	Capture	Reset Input from /RST pin
	Update	Not used
2	Capture	CAN RX Output Enable to pin
	Update	CAN RX Output Enable to pin
3	Capture	CAN RX Input from pin
	Update	CAN RX Output to pin
4	Capture	CAN TX Output Enable to pin
	Update	CAN TX Output Enable to pin
5	Capture	CAN TX Input from pin
	Update	CAN TX Output to pin
6	Capture	External Clock from XTAL1 pin
	Update	Not used
7	Capture	Weak Pullup Enable from MCU
	Update	Weak Pullup Enable to Port Pins
8, 10, 12, 14, 16, 18, 20, 22	Capture	P0.n output enable from MCU (e.g. Bit 8 = P0.0, Bit 10 = P0.1, etc.)
	Update	P0.n output enable to pin (e.g. Bit 8 = P0.0oe, Bit 10 = P0.1oe, etc.)
9, 11, 13, 15, 17, 19, 21, 23	Capture	P0.n input from pin (e.g. Bit 9 = P0.0, Bit 11 = P0.1, etc.)
	Update	P0.n output to pin (e.g. Bit 9 = P0.0, Bit 11 = P0.1, etc.)
24, 26, 28, 30, 32, 34, 36, 38	Capture	P1.n output enable from MCU (follows P0.n numbering scheme)
	Update	P1.n output enable to pin (follows P0.n numbering scheme)
25, 27, 29, 31, 33, 35, 37, 39	Capture	P1.n input from pin (follows P0.n numbering scheme)
	Update	P1.n output to pin (follows P0.n numbering scheme)
40, 42, 44, 46, 48, 50, 52, 54	Capture	P2.n output enable from MCU (follows P0.n numbering scheme)
	Update	P2.n output enable to pin (follows P0.n numbering scheme)
41, 43, 45, 47, 49, 51, 53, 55	Capture	P2.n input from pin (follows P0.n numbering scheme)
	Update	P2.n output to pin (follows P0.n numbering scheme)
56, 58, 60, 62, 64, 66, 68, 70	Capture	P3.n output enable from MCU (follows P0.n numbering scheme)
	Update	P3.n output enable to pin (follows P0.n numbering scheme)
57, 59, 61, 63, 65, 67, 69, 71	Capture	P3.n input from pin (follows P0.n numbering scheme)
	Update	P3.n output to pin (follows P0.n numbering scheme)
72, 74, 76	Capture	P4.5, P4.6, P4.7 (respectively) output enable from MCU
	Update	P4.5, P4.6, P4.7 (respectively) output enable to pin
73, 75, 77	Capture	P4.5, P4.6, P4.7 (respectively) input from pin
	Update	P4.5, P4.6, P4.7 (respectively) output to pin
78, 80, 82, 84, 86, 88, 90, 92	Capture	P5.n output enable from MCU (follows P0.n numbering scheme)
	Update	P5.n output enable to pin (follows P0.n numbering scheme)