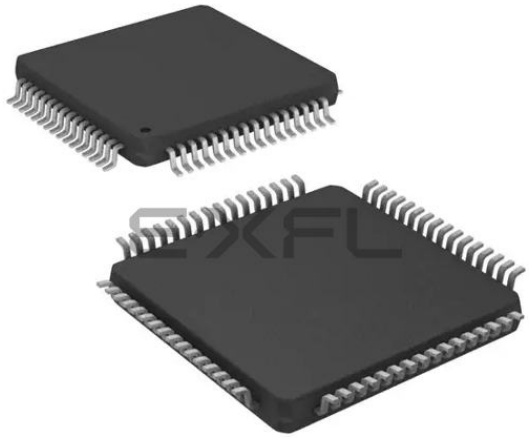

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Details	
Product Status	Not For New Designs
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Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f065-gq

Table 4.1. Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	F060	F061	F064	F065		
	F062	F063	F066	F067		
VRGND0	20	14	20	14	A In	ADC0 Voltage Reference Ground. This pin should be grounded if using the ADC.
VBGAP0	22	16	22	16	A Out	ADC0 Bandgap Bypass Pin.
VREF1	6	2	6	2	A I/O	Bandgap Voltage Reference Output for ADC1. ADC1 Voltage Reference Input.
VRGND1	7	3	7	3	A In	ADC1 Voltage Reference Ground. This pin should be grounded if using the ADC.
VBGAP1	5	1	5	1	A Out	ADC1 Bandgap Bypass Pin.
VREF2	2				A In	ADC2 Voltage Reference Input.
		62			A In	ADC2, DAC0, and DAC1 Voltage Reference Input.
VREFD	3				A In	DAC0 and DAC1 Voltage Reference Input.
AIN0	18	12	18	12	A In	ADC0 Signal Input (See ADC0 Specification for complete description).
AIN0G	19	13	19	13	A In	ADC0 DC Bias Input (See ADC0 Specification for complete description).
AIN1	9	5	9	5	A In	ADC1 Signal Input (See ADC1 Specification for complete description).
AIN1G	8	4	8	4	A In	ADC1 DC Bias Input (See ADC1 Specification for complete description).
CNVSTR0	15	9	15	9	D In	External Conversion Start Source for ADC0
CNVSTR1	12	8	12	8	D In	External Conversion Start Source for ADC1
CANTX	94	59			D Out	Controller Area Network Transmit Output.
CANRX	95	60			D In	Controller Area Network Receive Input.
DAC0	25	17			A Out	Digital to Analog Converter 0 Voltage Output. (See DAC Specification for complete description).
DAC1	1	64			A Out	Digital to Analog Converter 1 Voltage Output. (See DAC Specification for complete description).
P0.0	62	51	62	51	D I/O	Port 0.0. See Port Input/Output section for complete description.
P0.1	61	50	61	50	D I/O	Port 0.1. See Port Input/Output section for complete description.
P0.2	60	49	60	49	D I/O	Port 0.2. See Port Input/Output section for complete description.
P0.3	59	48	59	48	D I/O	Port 0.3. See Port Input/Output section for complete description.
P0.4	58	47	58	47	D I/O	Port 0.4. See Port Input/Output section for complete description.

Figure 5.6. AMX0SL: AMUX Configuration Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	DIFFSEL	-	-	-	-	-	-	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBB
SFR Page: 0

Bit 7: RESERVED. Write to 0b.
Bit 6: DIFFSEL: Fully Differential Conversion Mode Select Bit.
0: Operate In Single-Ended Mode.
1: Operate In Differential Mode.
Bit 5-0: RESERVED. Write to 000000b.

NOTE: For single-ended mode, the ADC0 Data Word is stored in ADC0H and ADC0L, while the ADC1 Data Word is stored in ADC1H and ADC1L.
In differential mode, the combined ADC Data Word is stored in ADC0H and ADC0L, and is a 2’s complement number. ADC1’s Data Word (single-ended) is also stored in ADC1H and ADC1L.

Figure 5.16. ADC1H: ADC1 Data Word MSB Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBF
SFR Page: 1

Bits 7-0: ADC1 Data Word High-Order Bits.

Figure 5.17. ADC1L: ADC1 Data Word LSB Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBE
SFR Page: 1

Bits 7-0: ADC1 Data Word Low-Order Bits.

Figure 5.18. ADC1 Data Word Example

16-bit ADC1 Data Word appears in the ADC1 Data Word Registers as follows:

Example: ADC1 Data Word Conversion Map, AIN1 Input in Single-Ended Mode (AMX1SL = 0x00)

AIN1-AIN1G (Volts)	**ADC1H:ADC1L**
VREF * (65535/65536)	0xFFFF
VREF / 2	0x8000
VREF * (32767/65536)	0x7FFF
0	0x0000

$$Code = Vin \times \frac{Gain}{VREF} \times 2^n \quad \text{; 'n' = 16}$$

For differential mode, the differential data word appears in ADC0H and ADC0L. The single-ended ADC1 results are always present in ADC1H and ADC1L, regardless of the operating mode.

6.2. DMA0 Instruction Format

DMA instructions can request single-ended data from both ADC0 and ADC1, as well as the differential combination of the two ADC inputs. The instruction format is identical to the DMA0IDT register, shown in Figure 6.7. Depending on which bits are set to ‘1’ in the instruction word, either 2 or 4 bytes of data will be written to XRAM for each DMA instruction cycle (excluding End-Of-Operation instructions). Table 6.1 details all of the valid DMA instructions. Instructions not listed in the table are not valid DMA instructions, and should not be used. Note that the ADCs can be independently controlled by the microcontroller when their outputs are not requested by the DMA.

Table 6.1. DMA0 Instruction Set

Instruction Word	Description	First Data Written to XRAM (2 bytes)	Second Data Written to XRAM (2 bytes)
00000000b	End-Of-Operation	none	none
10000000b	End-Of-Operation with Continuous Conversion	none	none
x0010000b	Retrieve ADC0 Data	ADC0H:ADC0L	none
x0100000b	Retrieve ADC1 Data	ADC1H:ADC1L	none
x0110000b	Retrieve ADC0 and ADC1 Data	ADC0H:ADC0L	ADC1H:ADC1L
x10x0000b	Retrieve Differential Data	ADC0H:ADC0L (differential result from both ADCs)	none
x11x0000b	Retrieve Differential and ADC1 Data	ADC0H:ADC0L (differential result from both ADCs)	ADC1H:ADC1L

6.3. XRAM Addressing and Setup

The DMA Interface can be configured to access either on-chip or off-chip XRAM. Any writes to on-chip XRAM by the DMA Control Logic occur when the processor core is not accessing the on-chip XRAM. This ensures that the DMA will not interfere with processor instruction timing.

Off-chip XRAM access (only available on the C8051F060/2/4/6) is controlled by the DMA0HLT bit in DMA0CF (DMA Configuration Register, Figure 6.5). The DMA will have full access to off-chip XRAM when this bit is ‘0’, and the processor core will have full access to off-chip XRAM when this bit is ‘1’. The DMA0HLT bit should be controlled in software when both the processor core and the DMA Interface require access to off-chip XRAM data space. Before setting DMA0HLT to ‘1’, the software should check the DMA0XBY bit to ensure that the DMA is not currently accessing off-chip XRAM. The processor core cannot access off-chip XRAM while DMA0HLT is ‘0’. The processor will continue as though it was able to perform the desired memory access, but the data will not be written to or read from off-chip XRAM. When the processor core is finished accessing off-chip XRAM, DMA0HLT should be set back to ‘0’in software to return control to the DMA Interface. The DMA Control Logic will wait until DMA0HLT is ‘0’ before writing data to off-chip XRAM. If new data becomes available to the DMA Interface before the previous data has been written, an overflow condition will occur, and the new data word may be lost.

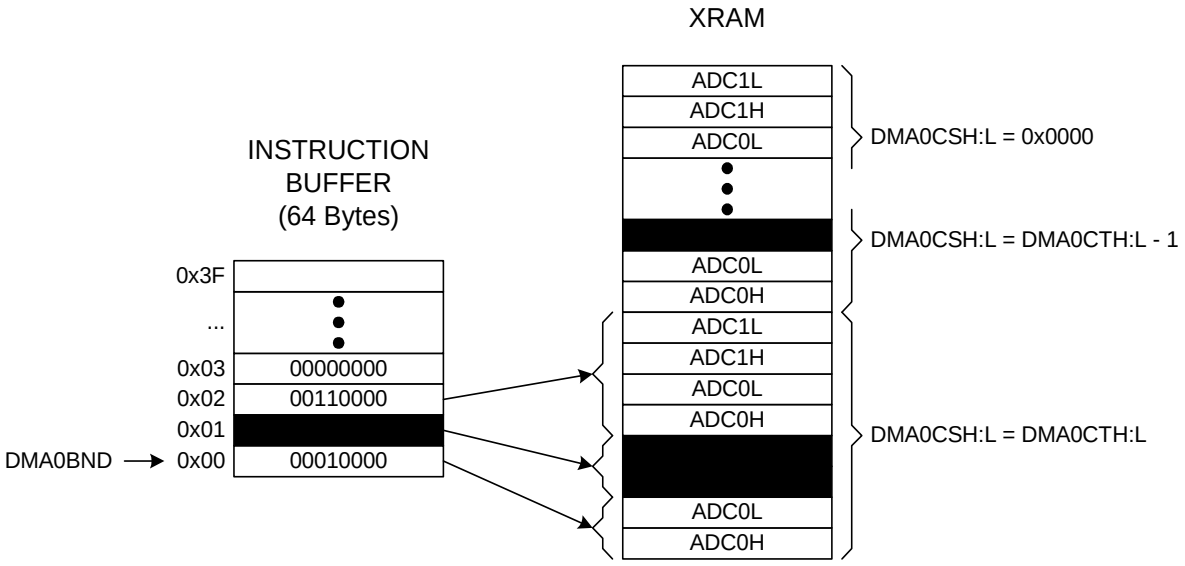
The Data Address Pointer Registers (DMA0DSH and DMA0DSL) contain the 16-bit XRAM address location where the DMA interface will write data. When the DMA is initially enabled, the DMA Data Address

Pointer Registers are initialized to the values contained in the DMA Data Address Beginning Registers (DMA0DAH and DMA0DAL). The Data Address Pointer Registers are automatically incremented by 2 or 4 after each data write by the DMA interface.

6.4. Instruction Execution in Mode 0

When the DMA interface begins an operation cycle, the DMA Instruction Status Register (DMA0ISW, Figure 6.9) is loaded with the address contained in the DMA Instruction Boundary Register (DMA0BND, Figure 6.8). The instruction is fetched from the Instruction Buffer, and the DMA Control Logic waits for data from the appropriate ADC(s). The DMA will execute each instruction once, and then increment DMA0ISW to the next instruction address. When the current DMA instruction is an End of Operation instruction, the Instruction Status Register is reset to the Instruction Boundary Register. If the Continuous Conversion bit (bit 7, CCNV) in the End of Operation instruction word is set to '1', the Repeat Counter is ignored, and the DMA will continue to execute instructions indefinitely. When CCNV is set to '0', the Repeat Counter (registers DMA0CSH and DMA0CSL) is decremented, and the DMA will continue to execute instructions until the Repeat Counter reaches 0x0000. The Repeat Counter is initialized with the Repeat Counter Limit value (registers DMA0CTH and DMA0CTL) at the beginning of the DMA operation. An example of Mode 0 operation is shown in Figure 6.2.

Figure 6.2. DMA Mode 0 Operation



7.2.2. Tracking Modes

The AD2TM bit in register ADC2CN controls the ADC2 track-and-hold mode. In its default state, the ADC2 input is continuously tracked, except when a conversion is in progress. When the AD2TM bit is logic 1, ADC2 operates in low-power track-and-hold mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR2 signal is used to initiate conversions in low-power tracking mode, ADC2 tracks only when CNVSTR2 is low; conversion begins on the rising edge of CNVSTR2 (see Figure 7.3). Tracking can also be disabled (shutdown) when the device is in low power standby or sleep modes. Low-power track-and-hold mode is also useful when AMUX settings are frequently changed, due to the settling time requirements described in Section "7.2.3. Settling Time Requirements" on page 91.

Figure 7.3. 10-Bit ADC Track and Conversion Example Timing

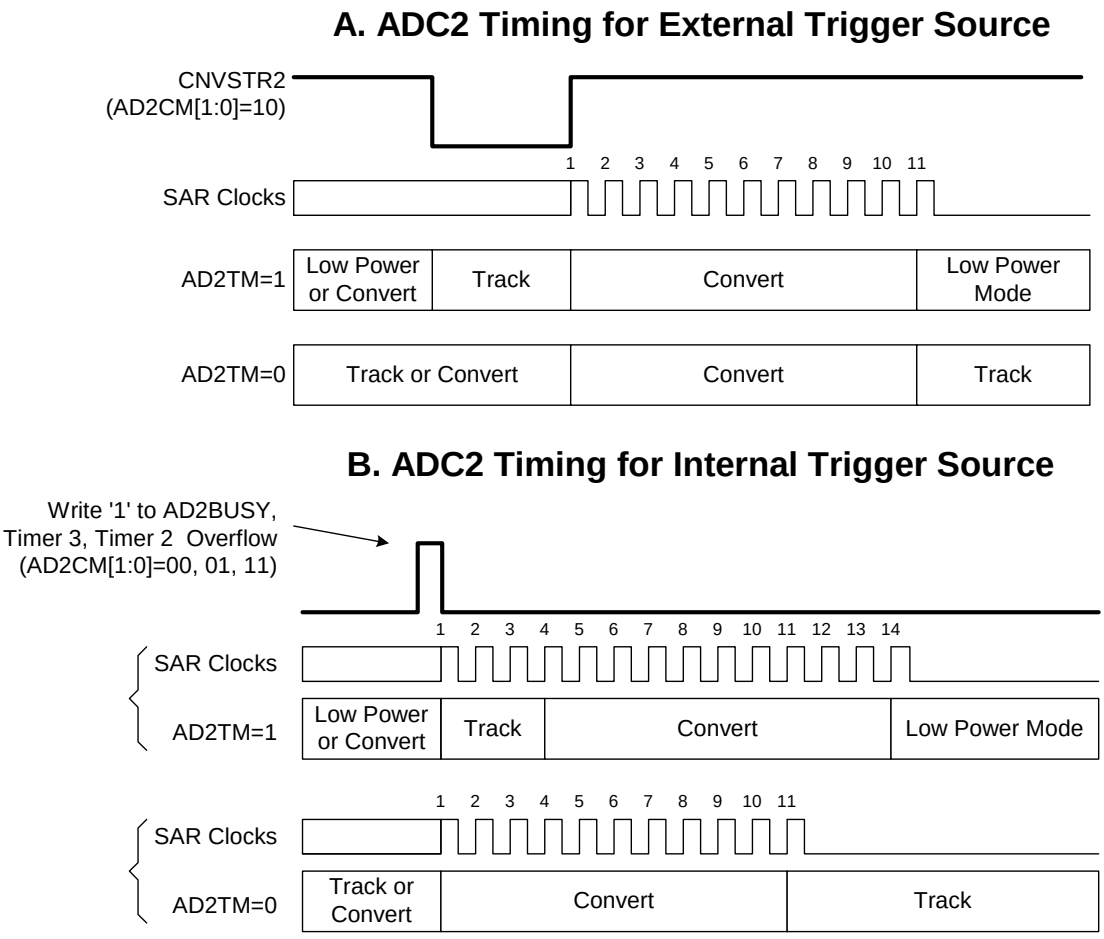


Table 12.1. Comparator Electrical Characteristics

VDD = 3.0 V, -40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Response Time, Mode 0	CPn+ - CPn- = 100 mV		100		ns
	CPn+ - CPn- = 10 mV		250		ns
Response Time, Mode 1	CPn+ - CPn- = 100 mV		175		ns
	CPn+ - CPn- = 10 mV		500		ns
Response Time, Mode 2	CPn+ - CPn- = 100 mV		320		ns
	CPn+ - CPn- = 10 mV		1100		ns
Response Time, Mode 3	CPn+ - CPn- = 100 mV		1050		ns
	CPn+ - CPn- = 10 mV		5200		ns
Common-Mode Rejection Ratio			1.5	4	mV/V
Positive Hysteresis 1	CPnHYP1-0 = 00		0	1	mV
Positive Hysteresis 2	CPnHYP1-0 = 01	3	5	7	mV
Positive Hysteresis 3	CPnHYP1-0 = 10	7	10	15	mV
Positive Hysteresis 4	CPnHYP1-0 = 11	15	20	25	mV
Negative Hysteresis 1	CPnHYN1-0 = 00		0	1	mV
Negative Hysteresis 2	CPnHYN1-0 = 01	3	5	7	mV
Negative Hysteresis 3	CPnHYN1-0 = 10	7	10	15	mV
Negative Hysteresis 4	CPnHYN1-0 = 11	15	20	25	mV
Inverting or Non-Inverting Input Voltage Range		-0.25		VDD + 0.25	V
Input Capacitance			7		pF
Input Bias Current		-5	0.001	+5	nA
Input Offset Voltage		-5		+5	mV
Power Supply					
Power Supply Rejection			0.1	1	mV/V
Power-up Time			10		µs
Supply Current at DC	Mode 0		7.6		µA
	Mode 1		3.2		µA
	Mode 2		1.3		µA
	Mode 3		0.4		µA

Table 13.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page No.
REF0CN	0xD1	0	Voltage Reference Control 0	page 62
REF1CN	0xD1	1	Voltage Reference Control 1	page 62
REF2CN	0xD1	2	Voltage Reference Control 2	page 112[*2], page 114[*3], page 116[*5]
RSTSRC	0xEF	0	Reset Source	page 168
SADDR0	0xA9	0	UART 0 Slave Address	page 276
SADEN0	0xB9	0	UART 0 Slave Address Enable	page 276
SBUF0	0x99	0	UART 0 Data Buffer	page 276
SBUF1	0x99	1	UART 1 Data Buffer	page 283
SCON0	0x98	0	UART 0 Control	page 274
SCON1	0x98	1	UART 1 Control	page 282
SFRLAST	0x86	All Pages	SFR Page Stack Access Register	page 140
SFRNEXT	0x85	All Pages	SFR Page Register	page 140
SFRPAGE	0x84	All Pages	SFR Page Register	page 139
SFRPGCN	0x96	F	SFR Page Control Register	page 139
SMB0ADR	0xC3	0	SMBus Slave Address	page 246
SMB0CN	0xC0	0	SMBus Control	page 243
SMB0CR	0xCF	0	SMBus Clock Rate	page 244
SMB0DAT	0xC2	0	SMBus Data	page 245
SMB0STA	0xC1	0	SMBus Status	page 247
SP	0x81	All Pages	Stack Pointer	page 148
SPI0CFG	0x9A	0	SPI Configuration	page 258
SPI0CKR	0x9D	0	SPI Clock Rate Control	page 260
SPI0CN	0xF8	0	SPI Control	page 259
SPI0DAT	0x9B	0	SPI Data	page 261
SSTA0	0x91	0	UART 0 Status	page 275
TCON	0x88	0	Timer/Counter Control	page 291
TH0	0x8C	0	Timer/Counter 0 High	page 294
TH1	0x8D	0	Timer/Counter 1 High	page 294
TL0	0x8A	0	Timer/Counter 0 Low	page 294
TL1	0x8B	0	Timer/Counter 1 Low	page 294
TMOD	0x89	0	Timer/Counter Mode	page 292
TMR2CF	0xC9	0	Timer/Counter 2 Configuration	page 300
TMR2CN	0xC8	0	Timer/Counter 2 Control	page 299
TMR2H	0xCD	0	Timer/Counter 2 High	page 302
TMR2L	0xCC	0	Timer/Counter 2 Low	page 301
TMR3CF	0xC9	1	Timer/Counter 3 Configuration	page 300
TMR3CN	0xC8	1	Timer/Counter 3 Control	page 299
TMR3H	0xCD	1	Timer/Counter 3 High	page 302
TMR3L	0xCC	1	Timer/Counter 3 Low	page 301
TMR4CF	0xC9	2	Timer/Counter 4 Configuration	page 300
TMR4CN	0xC8	2	Timer/Counter 4 Control	page 299
TMR4H	0xCD	2	Timer/Counter 4 High	page 302

13.3. Interrupt Handler

The CIP-51 includes an extended interrupt system supporting a total of 22 interrupt sources with two priority levels. The allocation of interrupt sources between on-chip peripherals and external inputs pins varies according to the specific version of the device. Each interrupt source has one or more associated interrupt-pending flag(s) located in an SFR. When a peripheral or external source meets a valid interrupt condition, the associated interrupt-pending flag is set to logic 1.

If interrupts are enabled for the source, an interrupt request is generated when the interrupt-pending flag is set. As soon as execution of the current instruction is complete, the CPU generates an LCALL to a predetermined address to begin execution of an interrupt service routine (ISR). Each ISR must end with an RETI instruction, which returns program execution to the next instruction that would have been executed if the interrupt request had not occurred. If interrupts are not enabled, the interrupt-pending flag is ignored by the hardware and program execution continues as normal. (The interrupt-pending flag is set to logic 1 regardless of the interrupt's enable/disable state.)

Each interrupt source can be individually enabled or disabled through the use of an associated interrupt enable bit in an SFR (IE-EIE2). However, interrupts must first be globally enabled by setting the EA bit (IE.7) to logic 1 before the individual interrupt enables are recognized. Setting the EA bit to logic 0 disables all interrupt sources regardless of the individual interrupt-enable settings.

Some interrupt-pending flags are automatically cleared by the hardware when the CPU vectors to the ISR. However, most are not cleared by the hardware and must be cleared by software before returning from the ISR. If an interrupt-pending flag remains set after the CPU completes the return-from-interrupt (RETI) instruction, a new interrupt request will be generated immediately and the CPU will re-enter the ISR after the completion of the next instruction.

13.3.1. MCU Interrupt Sources and Vectors

The MCUs support 22 interrupt sources. Software can simulate an interrupt event by setting any interrupt-pending flag to logic 1. If interrupts are enabled for the flag, an interrupt request will be generated and the CPU will vector to the ISR address associated with the interrupt-pending flag. MCU interrupt sources, associated vector addresses, priority order and control bits are summarized in Table 13.4. Refer to the datasheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

13.3.2. External Interrupts

The external interrupt sources (/INT0 and /INT1) are configurable as active-low level-sensitive or active-low edge-sensitive inputs depending on the setting of bits IT0 (TCON.0) and IT1 (TCON.2). IE0 (TCON.1) and IE1 (TCON.3) serve as the interrupt-pending flag for the /INT0 and /INT1 external interrupts, respectively. If an /INT0 or /INT1 external interrupt is configured as edge-sensitive, the corresponding interrupt-pending flag is automatically cleared by the hardware when the CPU vectors to the ISR. When configured as level sensitive, the interrupt-pending flag follows the state of the external interrupt's input pin. The external interrupt source must hold the input active until the interrupt request is recognized. It must then deactivate the interrupt request before execution of the ISR completes or another interrupt request will be generated.

Figure 14.4. RSTSRC: Reset Source Register

R	R/W	R/W	R/W	R	R/W	R/W	R/W	Reset Value
-	CNVRSEF	C0RSEF	SWRSEF	WDTRSF	MCDRSF	PORSF	PINRSF	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xEF
SFR Page: 0

Bit7: Reserved.

Bit6: CNVRSEF: Convert Start Reset Source Enable and Flag
Write: 0: CNVSTR2 is not a reset source.
1: CNVSTR2 is a reset source (active low).
Read: 0: Source of prior reset was not CNVSTR2.
1: Source of prior reset was CNVSTR2.

Bit5: C0RSEF: Comparator0 Reset Enable and Flag.
Write: 0: Comparator0 is not a reset source.
1: Comparator0 is a reset source (active low).
Read: 0: Source of last reset was not Comparator0.
1: Source of last reset was Comparator0.

Bit4: SWRSF: Software Reset Force and Flag.
Write: 0: No effect.
1: Forces an internal reset. /RST pin is not effected.
Read: 0: Source of last reset was not a write to the SWRSF bit.
1: Source of last reset was a write to the SWRSF bit.

Bit3: WDTRSF: Watchdog Timer Reset Flag.
0: Source of last reset was not WDT timeout.
1: Source of last reset was WDT timeout.

Bit2: MCDRSF: Missing Clock Detector Flag.
Write: 0: Missing Clock Detector disabled.
1: Missing Clock Detector enabled; triggers a reset if a missing clock condition is detected.
Read: 0: Source of last reset was not a Missing Clock Detector timeout.
1: Source of last reset was a Missing Clock Detector timeout.

Bit1: PORSF: Power-On Reset Flag.
Write: If the VDD monitor circuitry is enabled (by tying the MONEN pin to a logic high state), this bit can be written to select or de-select the VDD monitor as a reset source.
0: De-select the VDD monitor as a reset source.
1: Select the VDD monitor as a reset source.
Important: At power-on, the VDD monitor is enabled/disabled using the external VDD monitor enable pin (MONEN). The PORSF bit does not disable or enable the VDD monitor circuit. It simply selects the VDD monitor as a reset source.
Read: This bit is set whenever a power-on reset occurs. This may be due to a true power-on reset or a VDD monitor reset. In either case, data memory should be considered indeterminate following the reset.
0: Source of last reset was not a power-on or VDD monitor reset.
1: Source of last reset was a power-on or VDD monitor reset.
Note: When this flag is read as '1', all other reset flags are indeterminate.

Bit0: PINRSF: HW Pin Reset Flag.
Write: 0: No effect.
1: Forces a Power-On Reset. /RST is driven low.
Read: 0: Source of prior reset was not /RST pin.
1: Source of prior reset was /RST pin.

Figure 17.1. EMI0CN: External Memory Interface Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PGSEL7	PGSEL6	PGSEL5	PGSEL4	PGSEL3	PGSEL2	PGSEL1	PGSEL0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA2
SFR Page: 0

Bits7-0: PGSEL[7:0]: XRAM Page Select Bits.
The XRAM Page Select Bits provide the high byte of the 16-bit external data memory address when using an 8-bit MOVX command, effectively selecting a 256-byte page of RAM.
0x00: 0x0000 to 0x00FF
0x01: 0x0100 to 0x01FF
...
0xFE: 0xFE00 to 0xFEFF
0xFF: 0xFF00 to 0xFFFF

Figure 17.2. EMI0CF: External Memory Configuration

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	PRTSEL	EMD2	EMD1	EMD0	EALE1	EALE0	00000011
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA3
SFR Page: 0

Bits7-6: Unused. Read = 00b. Write = don't care.
Bit5: PRTSEL: EMIF Port Select.
0: EMIF not mapped to port pins.
1: EMIF active on P4-P7.
Bit4: EMD2: EMIF Multiplex Mode Select.
0: EMIF operates in multiplexed address/data mode.
1: EMIF operates in non-multiplexed mode (separate address and data pins).
Bits3-2: EMD1-0: EMIF Operating Mode Select.
These bits control the operating mode of the External Memory Interface.
00: Internal Only: MOVX accesses on-chip XRAM only. All effective addresses alias to on-chip memory space.
01: Split Mode without Bank Select: Accesses below the 4 kB boundary are directed on-chip. Accesses above the 4 kB boundary are directed off-chip. 8-bit off-chip MOVX operations use the current contents of the Address High port latches to resolve upper address byte. Note that in order to access off-chip space, EMI0CN must be set to a page that is not contained in the on-chip address space.
10: Split Mode with Bank Select: Accesses below the 4 kB boundary are directed on-chip. Accesses above the 4 kB boundary are directed off-chip. 8-bit off-chip MOVX operations use the contents of EMI0CN to determine the high-byte of the address.
11: External Only: MOVX accesses off-chip XRAM only. On-chip XRAM is not visible to the CPU.
Bits1-0: EALE1-0: ALE Pulse-Width Select Bits (only has effect when EMD2 = 0).
00: ALE high and ALE low pulse width = 1 SYSCLK cycle.
01: ALE high and ALE low pulse width = 2 SYSCLK cycles.
10: ALE high and ALE low pulse width = 3 SYSCLK cycles.
11: ALE high and ALE low pulse width = 4 SYSCLK cycles.

17.4. Multiplexed and Non-multiplexed Selection

The External Memory Interface is capable of acting in a Multiplexed mode or a Non-multiplexed mode, depending on the state of the EMD2 (EMI0CF.4) bit.

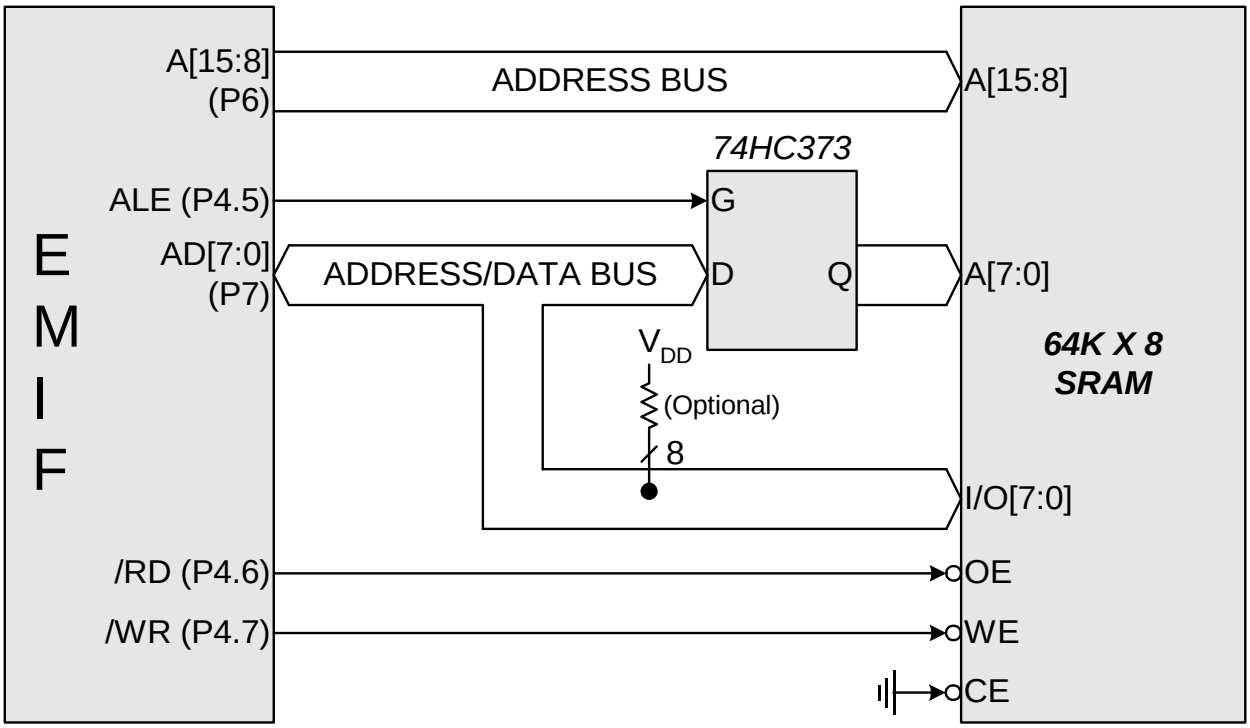
17.4.1. Multiplexed Configuration

In Multiplexed mode, the Data Bus and the lower 8-bits of the Address Bus share the same Port pins: AD[7:0]. In this mode, an external latch (74HC373 or equivalent logic gate) is used to hold the lower 8-bits of the RAM address. The external latch is controlled by the ALE (Address Latch Enable) signal, which is driven by the External Memory Interface logic. An example of a Multiplexed Configuration is shown in Figure 17.3.

In Multiplexed mode, the external MOVX operation can be broken into two phases delineated by the state of the ALE signal. During the first phase, ALE is high and the lower 8-bits of the Address Bus are presented to AD[7:0]. During this phase, the address latch is configured such that the 'Q' outputs reflect the states of the 'D' inputs. When ALE falls, signaling the beginning of the second phase, the address latch outputs remain fixed and are no longer dependent on the latch inputs. Later in the second phase, the Data Bus controls the state of the AD[7:0] port at the time /RD or /WR is asserted.

See Section "17.6.2. Multiplexed Mode" on page 199 for more information.

Figure 17.3. Multiplexed Configuration Example



17.5.3. Split Mode with Bank Select

When EMI0CF.[3:2] are set to ‘10’, the XRAM memory map is split into two areas, on-chip space and off-chip space.

- Effective addresses below the 4 kB boundary will access on-chip XRAM space.
- Effective addresses beyond the 4 kB boundary will access off-chip space.
- 8-bit MOVX operations use the contents of EMI0CN to determine whether the memory access is on-chip or off-chip. The upper 8-bits of the Address Bus A[15:8] are determined by EMI0CN, and the lower 8-bits of the Address Bus A[7:0] are determined by R0 or R1. All 16-bits of the Address Bus A[15:0] are driven in “Bank Select” mode.
- 16-bit MOVX operations use the contents of DPTR to determine whether the memory access is on-chip or off-chip, and the full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

17.5.4. External Only

When EMI0CF[3:2] are set to ‘11’, all MOVX operations are directed to off-chip space. On-chip XRAM is not visible to the CPU. This mode is useful for accessing off-chip memory located between 0x0000 and the 4 kB boundary.

- 8-bit MOVX operations ignore the contents of EMI0CN. The upper Address bits A[15:8] are not driven (identical behavior to an off-chip access in “Split Mode without Bank Select” described above). This allows the user to manipulate the upper address bits at will by setting the Port state directly. The lower 8-bits of the effective address A[7:0] are determined by the contents of R0 or R1.
- 16-bit MOVX operations use the contents of DPTR to determine the effective address A[15:0]. The full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

Figure 21.2. Multiple-Master Mode Connection Diagram

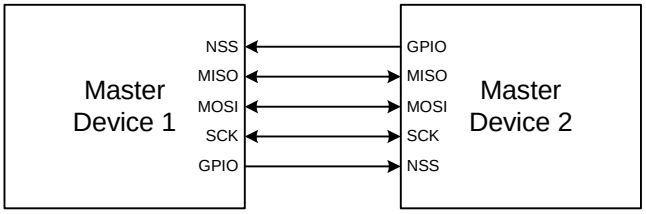


Figure 21.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram

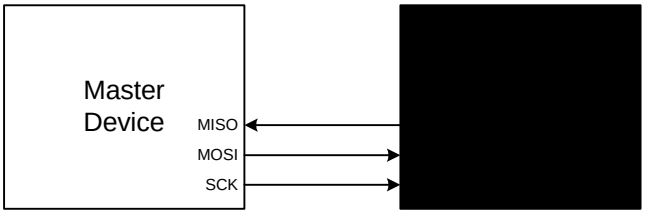


Figure 21.4. 4-Wire Single Master Mode and 4-Wire Slave Mode Connection Diagram

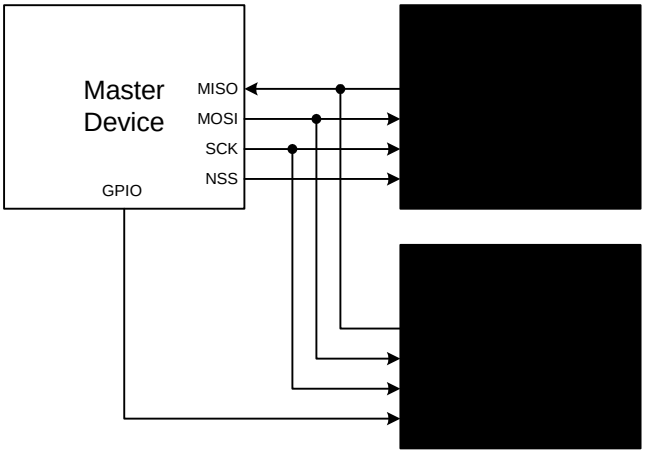


Table 22.2. Oscillator Frequencies for Standard Baud Rates

Oscillator frequency (MHz)	Divide Factor	Timer 1 Reload Value*	Timer 2, 3, or 4 Reload Value	Resulting Baud Rate (Hz)**
24.0	208	0xF3	0xFFF3	115200 (115384)
22.1184	192	0xF4	0xFFF4	115200
18.432	160	0xF6	0xFFF6	115200
11.0592	96	0xFA	0xFFFA	115200
3.6864	32	0xFE	0xFFFE	115200
1.8432	16	0xFF	0xFFFF	115200
24.0	832	0xCC	0xFFCC	28800 (28846)
22.1184	768	0xD0	0xFFD0	28800
18.432	640	0xD8	0xFFD8	28800
11.0592	348	0xE8	0xFFE8	28800
3.6864	128	0xF8	0xFFF8	28800
1.8432	64	0xFC	0xFFFC	28800
24.0	2496	0x64	0xFF64	9600 (9615)
22.1184	2304	0x70	0xFF70	9600
18.432	1920	0x88	0xFF88	9600
11.0592	1152	0xB8	0xFFB8	9600
3.6864	384	0xE8	0xFFE8	9600
1.8432	192	0xF4	0xFFF4	9600

* Assumes SMOD0=1 and T1M=1.

** Numbers in parenthesis show the actual baud rate.

25.2.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA0 counter/timer is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1 and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to '0'; writing to PCA0CPHn sets ECOMn to '1'.

Figure 25.5. PCA Software Timer Mode Diagram

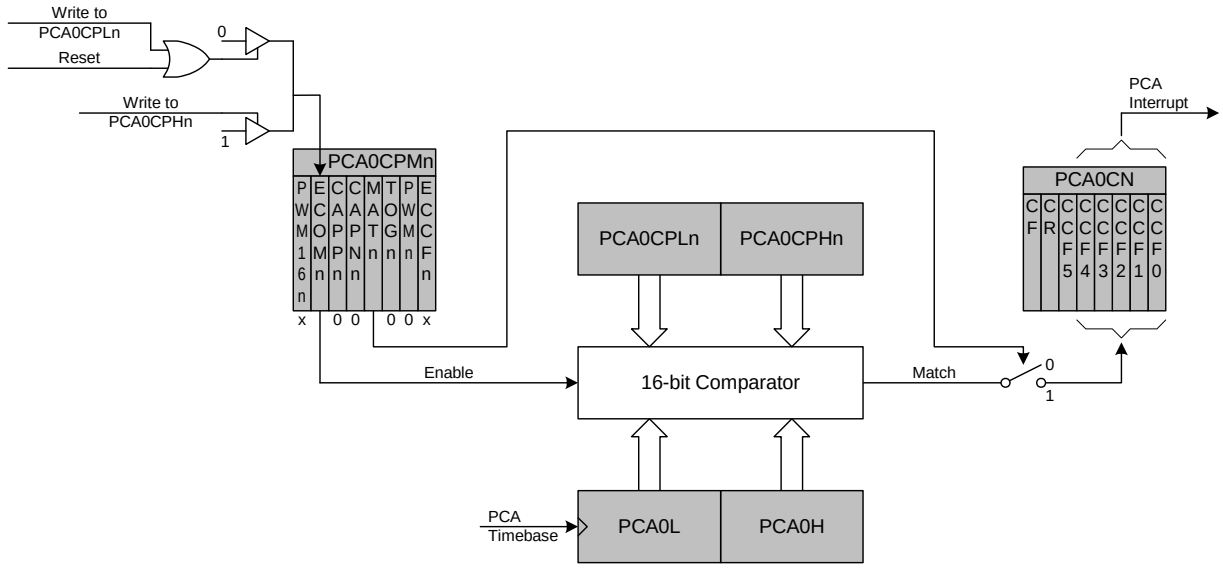


Figure 25.13. PCA0L: PCA0 Counter/Timer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF9
SFR Page: 0

Bits 7-0: PCA0L: PCA0 Counter/Timer Low Byte.
The PCA0L register holds the low byte (LSB) of the 16-bit PCA0 Counter/Timer.

Figure 25.14. PCA0H: PCA0 Counter/Timer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFA
SFR Page: 0

Bits 7-0: PCA0H: PCA0 Counter/Timer High Byte.
The PCA0H register holds the high byte (MSB) of the 16-bit PCA0 Counter/Timer.

Figure 26.3. FLASHCON: JTAG Flash Control Register

								Reset Value
SFLE	WRMD2	WRMD1	WRMD0	RDMD3	RDMD2	RDMD1	RDMD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

This register determines how the Flash interface logic will respond to reads and writes to the FLASHDAT Register.

Bit7: SFLE: Scratchpad Flash Memory Access Enable
When this bit is set, Flash reads and writes through the JTAG port are directed to the 128-byte Scratchpad Flash sector. When SFLE is set to logic 1, Flash accesses out of the address range 0x00-0x7F should not be attempted. Reads/Writes out of this range will yield undefined results.
0: Flash access from JTAG directed to the Program/Data Flash sector.
1: Flash access from JTAG directed to the Scratchpad sector.

Bits6-4: WRMD2-0: Write Mode Select Bits.
The Write Mode Select Bits control how the interface logic responds to writes to the FLASHDAT Register per the following values:
000: A FLASHDAT write replaces the data in the FLASHDAT register, but is otherwise ignored.
001: A FLASHDAT write initiates a write of FLASHDAT into the memory address by the FLASHADR register. FLASHADR is incremented by one when complete.
010: A FLASHDAT write initiates an erasure (sets all bytes to 0xFF) of the Flash page containing the address in FLASHADR. The data written must be 0xA5 for the erase to occur. FLASHADR is not affected. If FLASHADR = 0x7BFE - 0x7BFF, the entire user space will be erased (i.e. entire Flash memory except for Reserved area 0x7C00 - 0x7FFF).
(All other values for WRMD2-0 are reserved.)

Bits3-0: RDMD3-0: Read Mode Select Bits.
The Read Mode Select Bits control how the interface logic responds to reads to the FLASHDAT Register per the following values:
0000: A FLASHDAT read provides the data in the FLASHDAT register, but is otherwise ignored.
0001: A FLASHDAT read initiates a read of the byte addressed by the FLASHADR register if no operation is currently active. This mode is used for block reads.
0010: A FLASHDAT read initiates a read of the byte addressed by FLASHADR only if no operation is active and any data from a previous read has already been read from FLASHDAT. This mode allows single bytes to be read (or the last byte of a block) without initiating an extra read.
(All other values for RDMD3-0 are reserved.)