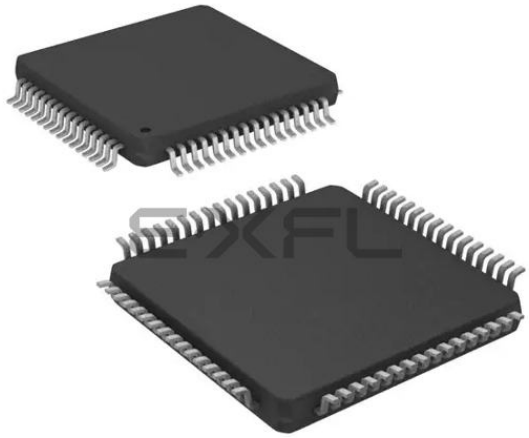

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f065r

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F06x family of devices utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The core has all the peripherals included with a standard 8052, including five 16-bit counter/timers, two full-duplex UARTs, 256 bytes of internal RAM, 128 byte Special Function Register (SFR) address space, and bit-addressable I/O Ports.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.5 shows a comparison of peak throughputs of various 8-bit microcontroller cores with their maximum system clocks.

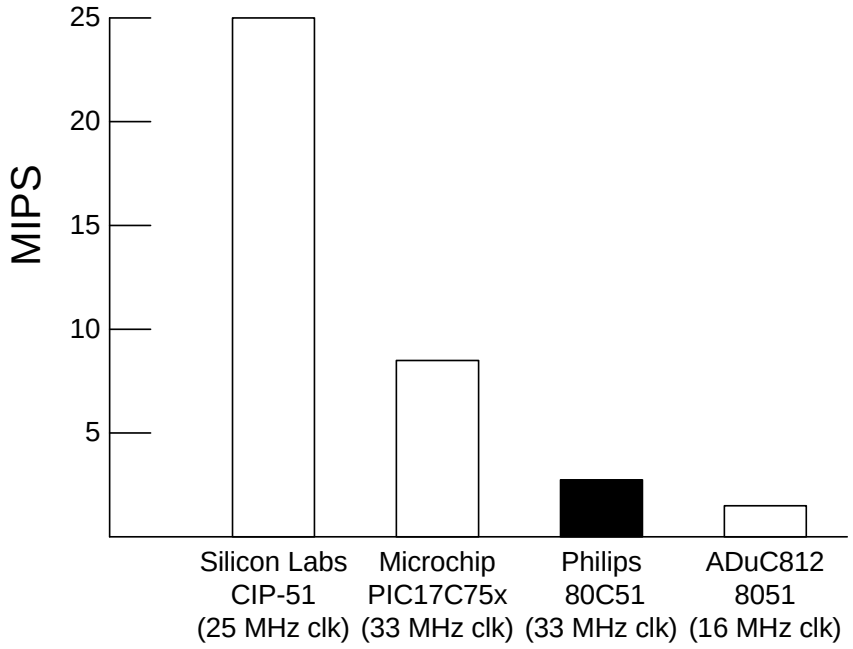


Figure 1.5. Comparison of Peak MCU Execution Speeds

Table 4.1. Pin Definitions (Continued)

Name	Pin Numbers				Type	Description
	F060	F061	F064	F065		
	F062	F063	F066	F067		
VRGND0	20	14	20	14	A In	ADC0 Voltage Reference Ground. This pin should be grounded if using the ADC.
VBGAP0	22	16	22	16	A Out	ADC0 Bandgap Bypass Pin.
VREF1	6	2	6	2	A I/O	Bandgap Voltage Reference Output for ADC1. ADC1 Voltage Reference Input.
VRGND1	7	3	7	3	A In	ADC1 Voltage Reference Ground. This pin should be grounded if using the ADC.
VBGAP1	5	1	5	1	A Out	ADC1 Bandgap Bypass Pin.
VREF2	2				A In	ADC2 Voltage Reference Input.
		62			A In	ADC2, DAC0, and DAC1 Voltage Reference Input.
VREFD	3				A In	DAC0 and DAC1 Voltage Reference Input.
AIN0	18	12	18	12	A In	ADC0 Signal Input (See ADC0 Specification for complete description).
AIN0G	19	13	19	13	A In	ADC0 DC Bias Input (See ADC0 Specification for complete description).
AIN1	9	5	9	5	A In	ADC1 Signal Input (See ADC1 Specification for complete description).
AIN1G	8	4	8	4	A In	ADC1 DC Bias Input (See ADC1 Specification for complete description).
CNVSTR0	15	9	15	9	D In	External Conversion Start Source for ADC0
CNVSTR1	12	8	12	8	D In	External Conversion Start Source for ADC1
CANTX	94	59			D Out	Controller Area Network Transmit Output.
CANRX	95	60			D In	Controller Area Network Receive Input.
DAC0	25	17			A Out	Digital to Analog Converter 0 Voltage Output. (See DAC Specification for complete description).
DAC1	1	64			A Out	Digital to Analog Converter 1 Voltage Output. (See DAC Specification for complete description).
P0.0	62	51	62	51	D I/O	Port 0.0. See Port Input/Output section for complete description.
P0.1	61	50	61	50	D I/O	Port 0.1. See Port Input/Output section for complete description.
P0.2	60	49	60	49	D I/O	Port 0.2. See Port Input/Output section for complete description.
P0.3	59	48	59	48	D I/O	Port 0.3. See Port Input/Output section for complete description.
P0.4	58	47	58	47	D I/O	Port 0.4. See Port Input/Output section for complete description.

Table 5.2. 16-Bit ADC0 and ADC1 Electrical Characteristics

VDD = 3.0 V, AV+ = 3.0 V, AVDD = 3.0 V, VREF = 2.50 V (REFBE=0), -40 to +85 °C unless otherwise specified

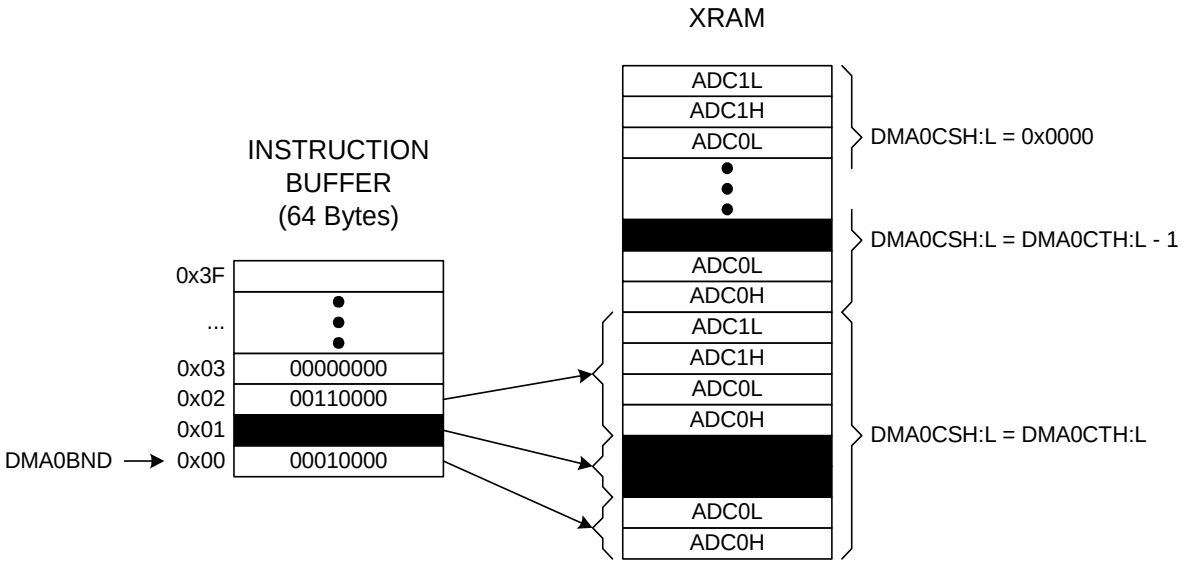
Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			16		bits
Integral Nonlinearity (C8051F060/1/4/5/6/7)	Single-Ended Differential		±0.75 ±0.5	±2 ±1	LSB
Integral Nonlinearity (C8051F062/3)	Single-Ended Differential		±1.5 ±1	±4 ±2	LSB
Differential Nonlinearity	Guaranteed Monotonic		±0.5		LSB
Offset Error			0.1		mV
Full Scale Error			0.008		%F.S.
Gain Temperature Coefficient			0.5		ppm/°C
Dynamic Performance (Sampling Rate = 1 Msps, AVDD, AV+ = 3.3V)					
Signal-to-Noise Plus Distortion	Fin = 10 kHz, Single-Ended Fin = 100 kHz, Single-Ended Fin = 10 kHz, Differential Fin = 100 kHz, Differential		86 84 89 88		dB dB dB dB
Total Harmonic Distortion	Fin = 10 kHz, Single-Ended Fin = 100 kHz, Single-Ended Fin = 10 kHz, Differential Fin = 100 kHz, Differential		96 84 103 93		dB dB dB dB
Spurious-Free Dynamic Range	Fin = 10 kHz, Single-Ended Fin = 100 kHz, Single-Ended Fin = 10 kHz, Differential Fin = 100 kHz, Differential		97 88 104 99		dB dB dB dB
CMRR	Fin = 10 kHz		86		dB
Channel Isolation			100		dB
Timing					
SAR Clock Frequency				25	MHz
Conversion Time in SAR Clocks		18			clocks
Track/Hold Acquisition Time		280			ns
Throughput Rate				1	Msps
Aperture Delay	External CNVST Signal		1.5		ns
RMS Aperture Jitter	External CNVST Signal		5		ps
Analog Inputs					
Input Voltage Range	Single-Ended (AINn - AINnG) Differential (AIN0 - AIN1)	0 -VREF		VREF VREF	V V
Input Capacitance			80		pF

Pointer Registers are initialized to the values contained in the DMA Data Address Beginning Registers (DMA0DAH and DMA0DAL). The Data Address Pointer Registers are automatically incremented by 2 or 4 after each data write by the DMA interface.

6.4. Instruction Execution in Mode 0

When the DMA interface begins an operation cycle, the DMA Instruction Status Register (DMA0ISW, Figure 6.9) is loaded with the address contained in the DMA Instruction Boundary Register (DMA0BND, Figure 6.8). The instruction is fetched from the Instruction Buffer, and the DMA Control Logic waits for data from the appropriate ADC(s). The DMA will execute each instruction once, and then increment DMA0ISW to the next instruction address. When the current DMA instruction is an End of Operation instruction, the Instruction Status Register is reset to the Instruction Boundary Register. If the Continuous Conversion bit (bit 7, CCNV) in the End of Operation instruction word is set to '1', the Repeat Counter is ignored, and the DMA will continue to execute instructions indefinitely. When CCNV is set to '0', the Repeat Counter (registers DMA0CSH and DMA0CSL) is decremented, and the DMA will continue to execute instructions until the Repeat Counter reaches 0x0000. The Repeat Counter is initialized with the Repeat Counter Limit value (registers DMA0CTH and DMA0CTL) at the beginning of the DMA operation. An example of Mode 0 operation is shown in Figure 6.2.

Figure 6.2. DMA Mode 0 Operation



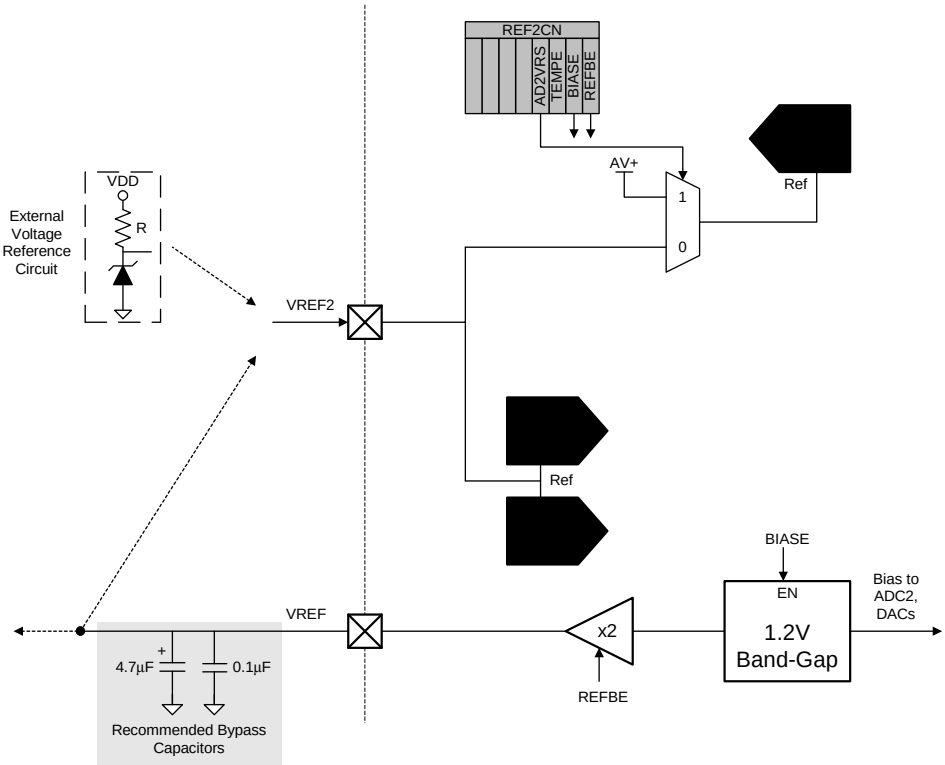
10. Voltage Reference 2 (C8051F061/3)

The internal voltage reference circuit consists of a 1.2 V, temperature stable bandgap voltage reference generator and a gain-of-two output buffer amplifier. The internal reference may be routed via the VREF pin to external system components or to the VREF2 input pin shown in Figure 10.1. The maximum load seen by the VREF pin must be less than 200 µA to AGND. Bypass capacitors of 0.1 µF and 4.7 µF are recommended from the VREF pin to AGND, as shown in Figure 10.1.

The VREF2 pin provides a voltage reference input for ADC2 and the DACs. ADC2 may also reference the analog power supply voltage, via the VREF multiplexers shown in Figure 10.1.

The Reference Control Register 2, REF2CN (defined in Figure 10.2) enables/disables the internal reference generator and selects the reference input for ADC2. The BIASE bit in REF2CN enables the on-board reference generator while the REFBE bit enables the gain-of-two buffer amplifier which drives the VREF pin. When disabled, the supply current drawn by the bandgap and buffer amplifier falls to less than 1 µA (typical) and the output of the buffer amplifier enters a high impedance state. If the internal bandgap is used as the reference voltage generator, BIASE and REFBE must both be set to logic 1. If the internal reference is not used, REFBE may be set to logic 0. Note that the BIASE bit must be set to logic 1 if ADC2 or either DAC is used, regardless of the voltage reference used. If neither ADC2 nor the DACs are being used, both of these bits can be set to logic 0 to conserve power. Bit AD2VRS selects between VREF2 and AV+ for the ADC2 voltage reference source. The electrical specifications for the Voltage Reference are given in Table 10.1.

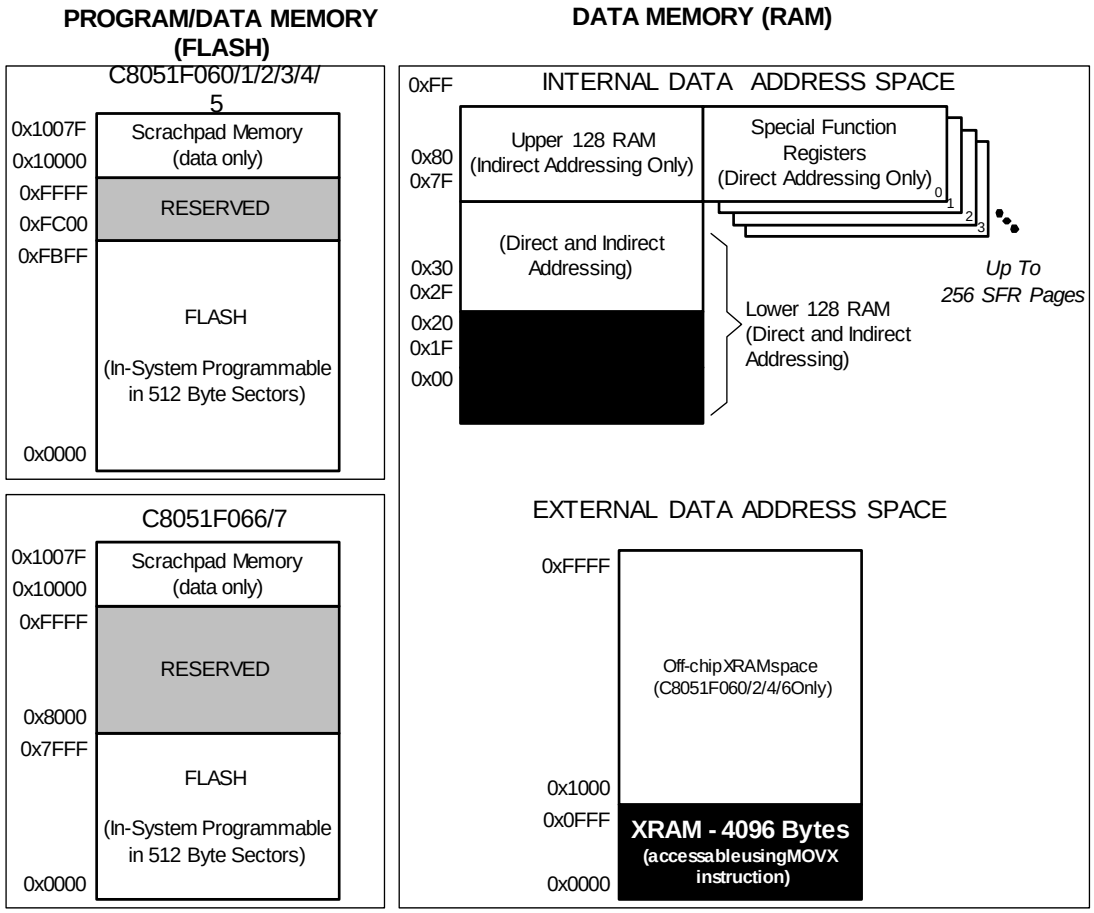
Figure 10.1. Voltage Reference Functional Block Diagram



13.2. Memory Organization

The memory organization of the CIP-51 System Controller is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. There are 256 bytes of internal data memory and 64 k bytes (C8051F060/1/2/3/4/5) or 32 k bytes (C8051F066/7) of internal program memory address space implemented within the CIP-51. The CIP-51 memory organization is shown in Figure 13.2.

Figure 13.2. Memory Map

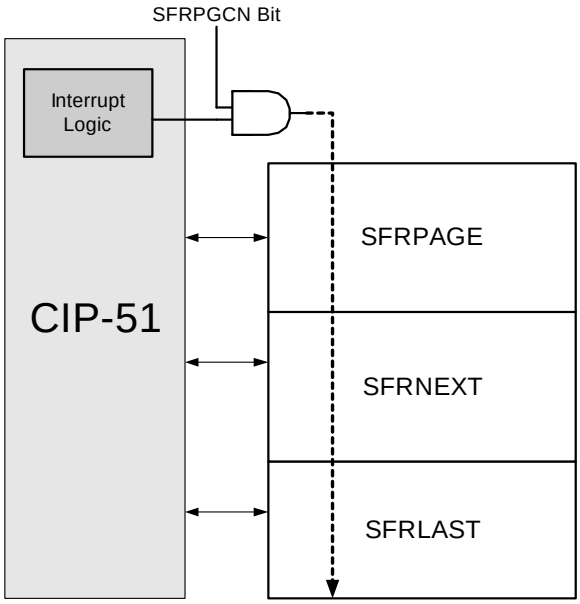


13.2.1. Program Memory

The CIP-51 has a 64 k byte program memory space. The C8051F060/1/2/3/4/5 devices implement 64 k bytes of this program memory space as in-system re-programmable Flash memory, organized in a contiguous block from addresses 0x0000 to 0xFFFF. Note: 1024 bytes (0xFC00 to 0xFFFF) of this memory are reserved, and are not available for user program storage. The C8051F066/7 implement 32 k bytes of this program memory space as in-system re-programmable Flash memory, organized in a contiguous block from addresses 0x0000 to 0x7FFF.

Program memory is normally assumed to be read-only (using the MOVC instruction). However, the CIP-51 can write to program memory by enabling Flash writes, and using the MOVX instruction. This feature provides a mechanism for the CIP-51 to update program code and use the program memory space for non-volatile data storage. Refer to Section “16. Flash Memory” on page 177 for further details.

Figure 13.3. SFR Page Stack



Automatic hardware switching of the SFR Page on interrupts may be enabled or disabled as desired using the SFR Automatic Page Control Enable Bit located in the SFR Page Control Register (SFRPGCN). This function defaults to ‘enabled’ upon reset. In this way, the autoswitching function will be enabled unless disabled in software.

A summary of the SFR locations (address and SFR page) is provided in Table 13.2. in the form of an SFR memory map. Each memory location in the map has an SFR page row, denoting the page in which that SFR resides. Note that certain SFRs are accessible from ALL SFR pages, and are denoted by the “**(ALL PAGES)**” designation. For example, the Port I/O registers P0, P1, P2, and P3 all have the “**(ALL PAGES)**” designation, indicating these SFRs are accessible from all SFR pages regardless of the SFRPAGE register value.

13.3.5. Interrupt Register Descriptions

The SFRs used to enable the interrupt sources and set their priority level are described below. Refer to the datasheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

Figure 13.19. IE: Interrupt Enable

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
EA	IEGF0	ET2	ES0	ET1	EX1	ET0	EX0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xA8
SFR Page: All Pages

Bit7: EA: Enable All Interrupts.
This bit globally enables/disables all interrupts. It overrides the individual interrupt mask settings.
0: Disable all interrupt sources.
1: Enable each interrupt according to its individual mask setting.

Bit6: IEGF0: General Purpose Flag 0.
This is a general purpose flag for use under software control.

Bit5: ET2: Enabler Timer 2 Interrupt.
This bit sets the masking of the Timer 2 interrupt.
0: Disable Timer 2 interrupt.
1: Enable interrupt requests generated by the TF2 flag.

Bit4: ES0: Enable UART0 Interrupt.
This bit sets the masking of the UART0 interrupt.
0: Disable UART0 interrupt.
1: Enable UART0 interrupt.

Bit3: ET1: Enable Timer 1 Interrupt.
This bit sets the masking of the Timer 1 interrupt.
0: Disable all Timer 1 interrupt.
1: Enable interrupt requests generated by the TF1 flag.

Bit2: EX1: Enable External Interrupt 1.
This bit sets the masking of external interrupt 1.
0: Disable external interrupt 1.
1: Enable interrupt requests generated by the /INT1 pin.

Bit1: ET0: Enable Timer 0 Interrupt.
This bit sets the masking of the Timer 0 interrupt.
0: Disable all Timer 0 interrupt.
1: Enable interrupt requests generated by the TF0 flag.

Bit0: EX0: Enable External Interrupt 0.
This bit sets the masking of external interrupt 0.
0: Disable external interrupt 0.
1: Enable interrupt requests generated by the /INT0 pin.

17.6.1. Non-multiplexed Mode

17.6.1.1.16-bit MOVX: EMI0CF[4:2] = ‘101’, ‘110’, or ‘111’.

Figure 17.7. Non-multiplexed 16-bit MOVX Timing

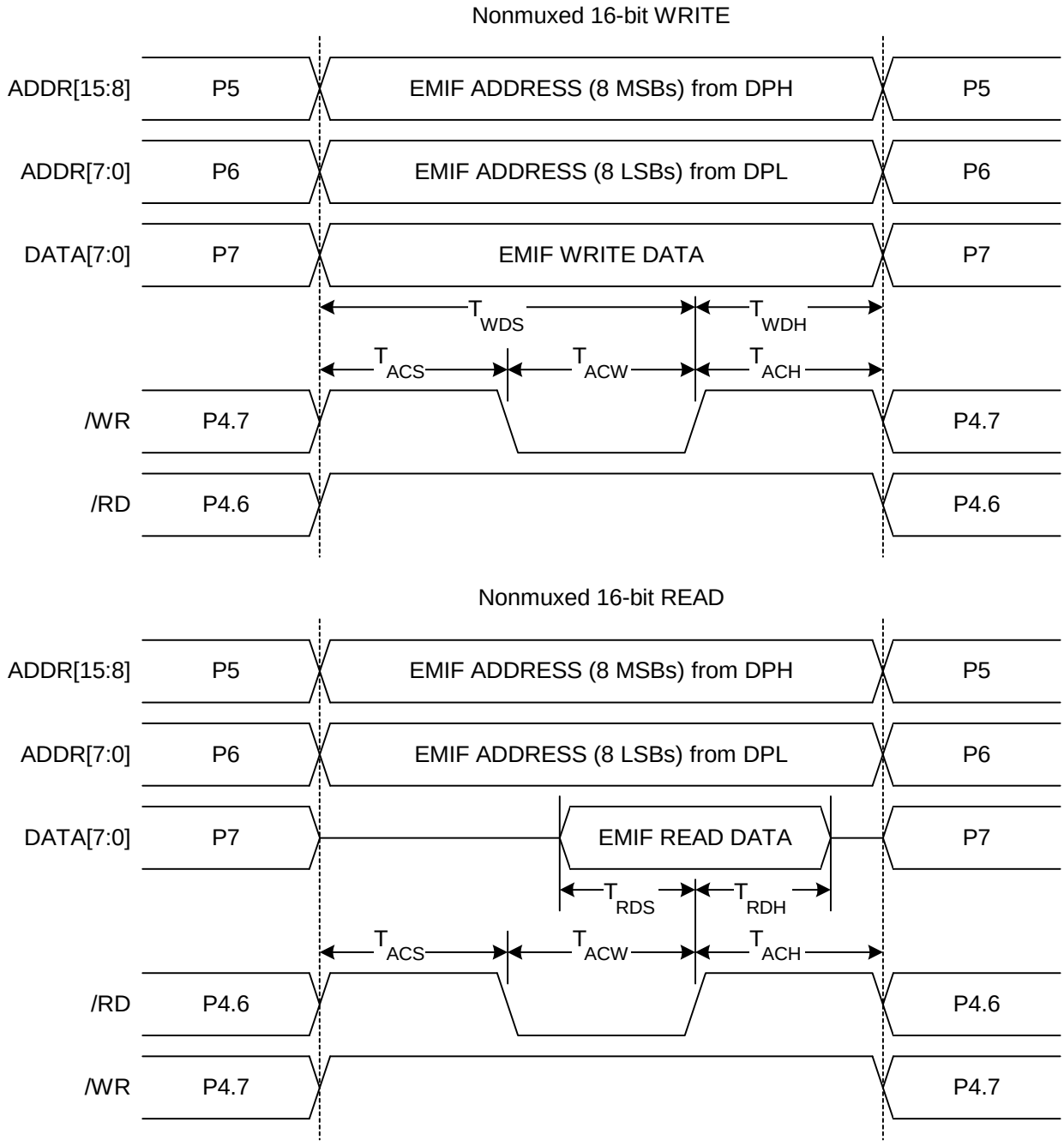


Table 19.1. CAN Register Index and Reset Values (Continued)

CAN Register Index	Register name	Reset Value	Notes
0x59	Message Valid 2	0x0000	Message valid flags for message objects (read only)

Figure 19.3. CAN0DATH: CAN Data Access Register High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD9
SFR Page: 1

Bit7-0: CAN0DATH: CAN Data Access Register High Byte.
The CAN0DAT Registers are used to read/write register values and data to and from the CAN Registers pointed to with the index number in the CAN0ADR Register.
The CAN0ADR Register is used to point the [CAN0DATH:CAN0DATL] to a desired CAN Register. The desired CAN Register's index number is moved into CAN0ADR. The CAN0DAT Register can then read/write to and from the CAN Register.

Figure 19.4. CAN0DATL: CAN Data Access Register Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD8
SFR Page: 1

Bit7-0: CAN0DATL: CAN Data Access Register Low Byte.
The CAN0DAT Registers are used to read/write register values and data to and from the CAN Registers pointed to with the index number in the CAN0ADR Register.
The CAN0ADR Register is used to point the [CAN0DATH:CAN0DATL] to a desired CAN Register. The desired CAN Register's index number is moved into CAN0ADR. The CAN0DAT Register can then read/write to and from the CAN Register.

Table 20.1. SMB0STA Status Codes and States

	0x60	Own slave address + W received. ACK transmitted.	Wait for data.
	0x68	Arbitration lost in sending SLA + R/W as master. Own address + W received. ACK transmitted.	Save current data for retry when bus is free. Wait for data.
	0x70	General call address received. ACK transmitted.	Wait for data.
	0x78	Arbitration lost in sending SLA + R/W as master. General call address received. ACK transmitted.	Save current data for retry when bus is free.
	0x80	Data byte received. ACK transmitted.	Read SMB0DAT. Wait for next byte or STOP.
	0x88	Data byte received. NACK transmitted.	Set STO to reset SMBus.
	0x90	Data byte received after general call address. ACK transmitted.	Read SMB0DAT. Wait for next byte or STOP.
	0x98	Data byte received after general call address. NACK transmitted.	Set STO to reset SMBus.
	0xA0	STOP or repeated START received.	No action necessary.
	0xA8	Own address + R received. ACK transmitted.	Load SMB0DAT with data to transmit.
	0xB0	Arbitration lost in transmitting SLA + R/W as master. Own address + R received. ACK transmitted.	Save current data for retry when bus is free. Load SMB0DAT with data to transmit.
	0xB8	Data byte transmitted. ACK received.	Load SMB0DAT with data to transmit.
	0xC0	Data byte transmitted. NACK received.	Wait for STOP.
	0xC8	Last data byte transmitted (AA=0). ACK received.	Set STO to reset SMBus.
	0xD0	SCL Clock High Timer per SMB0CR timed out	Set STO to reset SMBus.
	0x00	Bus Error (illegal START or STOP)	Set STO to reset SMBus.
	0xF8	Idle	State does not set SI.

Figure 21.10. SPI0CKR: SPI0 Clock Rate Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x9D
SFR Page: 0

Bits 7-0: SCR7-SCR0: SPI0 Clock Rate.
These bits determine the frequency of the SCK output when the SPI0 module is configured for master mode operation. The SCK clock frequency is a divided version of the system clock, and is given in the following equation, where *SYSCLK* is the system clock frequency and *SPI0CKR* is the 8-bit value held in the SPI0CKR register.

$$f_{SCK} = \frac{SYSCLK}{2 \times (SPI0CKR + 1)}$$

for 0 <= SPI0CKR <= 255

Example: If SYSCLK = 2 MHz and SPI0CKR = 0x04,

$$f_{SCK} = \frac{2000000}{2 \times (4 + 1)}$$

$$f_{SCK} = 200kHz$$

Figure 21.11. SPI0DAT: SPI0 Data Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x9B
SFR Page: 0

Bits 7-0: SPI0DAT: SPI0 Transmit and Receive Data.
The SPI0DAT register is used to transmit and receive SPI0 data. Writing data to SPI0DAT places the data into the transmit buffer and initiates a transfer when in Master Mode. A read of SPI0DAT returns the contents of the receive buffer.

22.1.3. Mode 2: 9-Bit UART, Fixed Baud Rate

Mode 2 provides asynchronous, full-duplex communication using a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. Mode 2 supports multiprocessor communications and hardware address recognition (see Section 22.2). On transmit, the ninth data bit is determined by the value in TB80 (SCON0.3). It can be assigned the value of the parity flag P in the PSW or used in multiprocessor communications. On receive, the ninth data bit goes into RB80 (SCON0.2) and the stop bit is ignored.

Data transmission begins when an instruction writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if RI0 is logic 0 and one of the following requirements are met:

1. SM20 is logic 0
2. SM20 is logic 1, the received 9th bit is logic 1, and the received address matches the UART0 address as described in Section 22.2.

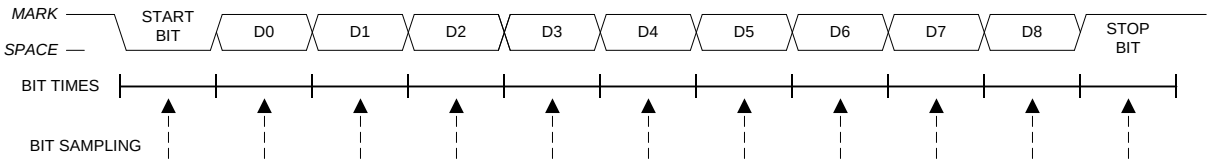
If the above conditions are satisfied, the eight bits of data are stored in SBUF0, the ninth bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either TI0 or RI0 are set.

The baud rate in Mode 2 is either SYSCLK / 32 or SYSCLK / 64, according to the value of the SMOD0 bit in register SSTA0.

Equation 22.5. Mode 2 Baud Rate

$$BaudRate = 2^{SMOD0} \times \left(\frac{SYSCLK}{64}\right)$$

Figure 22.5. UART0 Modes 2 and 3 Timing Diagram



23. UART1

UART1 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates (details in Section “23.1. Enhanced Baud Rate Generation” on page 278). Received data buffering allows UART1 to start reception of a second incoming data byte before software has finished reading the previous data byte.

UART1 has two associated SFRs: Serial Control Register 1 (SCON1) and Serial Data Buffer 1 (SBUF1). The single SBUF1 location provides access to both transmit and receive registers. Reading SBUF1 accesses the buffered Receive register; writing SBUF1 accesses the Transmit register.

With UART1 interrupts enabled, an interrupt is generated each time a transmit is completed (TI1 is set in SCON1), or a data byte has been received (RI1 is set in SCON1). The UART1 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software, allowing software to determine the cause of the UART1 interrupt (transmit complete or receive complete).

Figure 23.1. UART1 Block Diagram

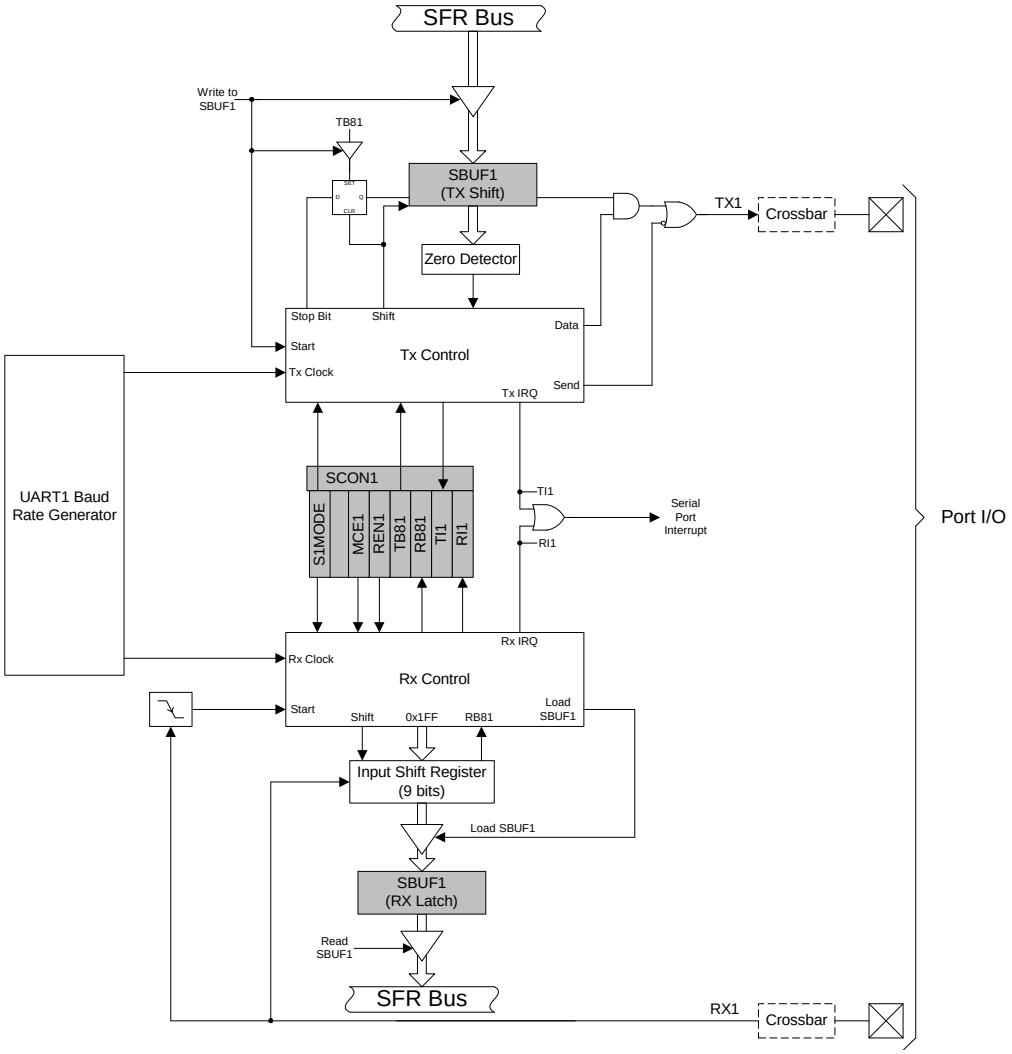


Figure 23.8. SBUF1: Serial (UART1) Port Data Buffer Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x99
SFR Page: 1

Bits7-0: SBUF1[7:0]: Serial Data Buffer Bits 7-0 (MSB-LSB).
This SFR accesses two registers; a transmit shift register and a receive latch register. When data is written to SBUF1, it goes to the transmit shift register and is held for serial transmission. Writing a byte to SBUF1 is what initiates the transmission. A read of SBUF1 returns the contents of the receive latch.

Figure 26.3. FLASHCON: JTAG Flash Control Register

								Reset Value
SFLE	WRMD2	WRMD1	WRMD0	RDMD3	RDMD2	RDMD1	RDMD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

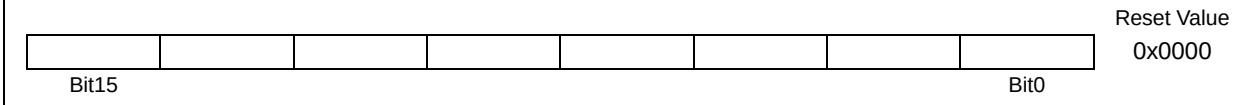
This register determines how the Flash interface logic will respond to reads and writes to the FLASHDAT Register.

Bit7: SFLE: Scratchpad Flash Memory Access Enable
When this bit is set, Flash reads and writes through the JTAG port are directed to the 128-byte Scratchpad Flash sector. When SFLE is set to logic 1, Flash accesses out of the address range 0x00-0x7F should not be attempted. Reads/Writes out of this range will yield undefined results.
0: Flash access from JTAG directed to the Program/Data Flash sector.
1: Flash access from JTAG directed to the Scratchpad sector.

Bits6-4: WRMD2-0: Write Mode Select Bits.
The Write Mode Select Bits control how the interface logic responds to writes to the FLASHDAT Register per the following values:
000: A FLASHDAT write replaces the data in the FLASHDAT register, but is otherwise ignored.
001: A FLASHDAT write initiates a write of FLASHDAT into the memory address by the FLASHADR register. FLASHADR is incremented by one when complete.
010: A FLASHDAT write initiates an erasure (sets all bytes to 0xFF) of the Flash page containing the address in FLASHADR. The data written must be 0xA5 for the erase to occur. FLASHADR is not affected. If FLASHADR = 0x7BFE - 0x7BFF, the entire user space will be erased (i.e. entire Flash memory except for Reserved area 0x7C00 - 0x7FFF).
(All other values for WRMD2-0 are reserved.)

Bits3-0: RDMD3-0: Read Mode Select Bits.
The Read Mode Select Bits control how the interface logic responds to reads to the FLASHDAT Register per the following values:
0000: A FLASHDAT read provides the data in the FLASHDAT register, but is otherwise ignored.
0001: A FLASHDAT read initiates a read of the byte addressed by the FLASHADR register if no operation is currently active. This mode is used for block reads.
0010: A FLASHDAT read initiates a read of the byte addressed by FLASHADR only if no operation is active and any data from a previous read has already been read from FLASHDAT. This mode allows single bytes to be read (or the last byte of a block) without initiating an extra read.
(All other values for RDMD3-0 are reserved.)

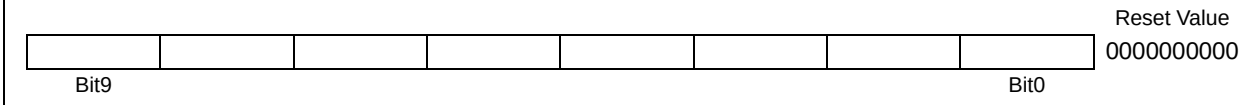
Figure 26.5. FLASHADR: JTAG Flash Address Register



This register holds the address for all JTAG Flash read, write, and erase operations. This register auto-increments
after each read or write, regardless of whether the operation succeeded or failed.

Bits15-0: Flash Operation 16-bit Address.

Figure 26.4. FLASHDAT: JTAG Flash Data Register



This register is used to read or write data to the Flash memory across the JTAG interface.

Bits9-2: DATA7-0: Flash Data Byte.
Bit1: FAIL: Flash Fail Bit.
0: Previous Flash memory operation was successful.
1: Previous Flash memory operation failed. Usually indicates the associated memory location was locked.
Bit0: BUSY: Flash Busy Bit.
0: Flash interface logic is not busy.
1: Flash interface logic is processing a request. Reads or writes while BUSY = 1 will not initiate another operation

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