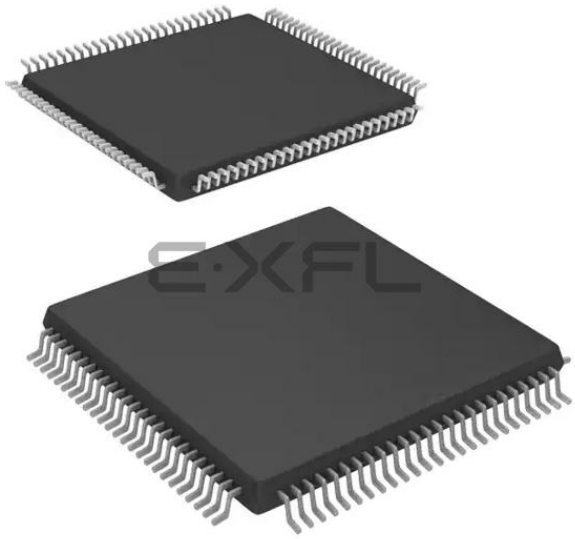

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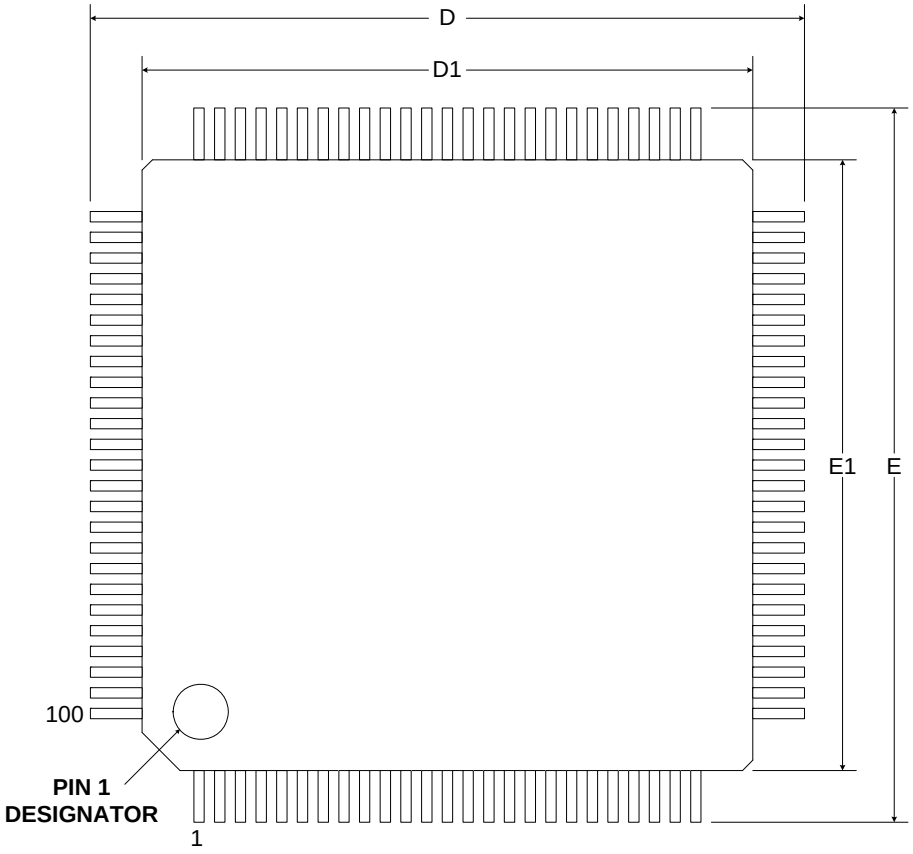
Applications of "Embedded - Microcontrollers"

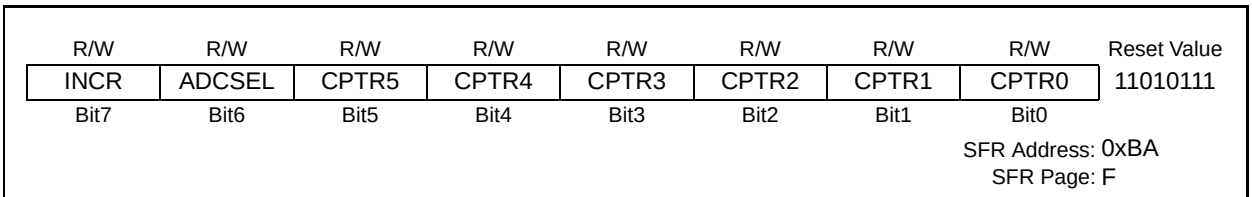
Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	59
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f066-gq



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
D	-	16.00	-
D1	-	14.00	-
e	-	0.50	-
E	-	16.00	-
E1	-	14.00	-
L	0.45	0.60	0.75

Figure 4.3. TQFP-100 Package Drawing

Figure 5.22. ADC0CPT: ADC Calibration Pointer Register



R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
INCR	ADCSEL	CPTR5	CPTR4	CPTR3	CPTR2	CPTR1	CPTR0	11010111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

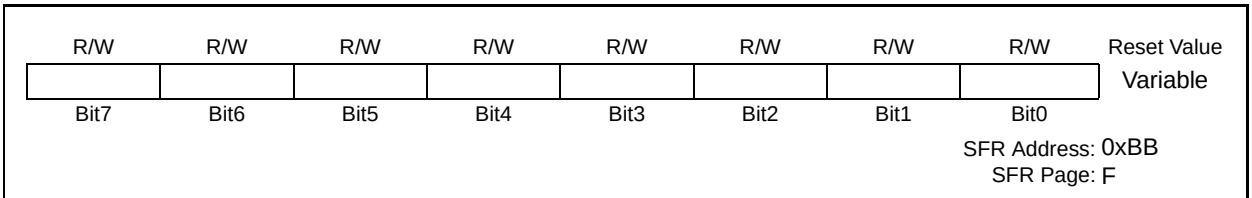
SFR Address: 0xBA
SFR Page: F

Bit 7: INCR: Pointer Address Automatic Increment.
0: Disable Auto-Increment.
1: Enable Auto-Increment. CPTR5-0 will automatically be incremented after each read or write to ADC0CCF.

Bit 6: ADCSEL: ADC Calibration Coefficient Select.
0: Reads and Writes of ADC0CCF will access ADC0 Calibration Coefficients.
1: Reads and Writes of ADC0CCF will access ADC1 Calibration Coefficients.

Bits 5-0: CPTR5-0: Calibration Coefficent Pointer.
Select which Calibration Coefficient location will be accessed when ADC0CCF is read or written.

Figure 5.23. ADC0CCF: ADC Calibration Coefficient Register

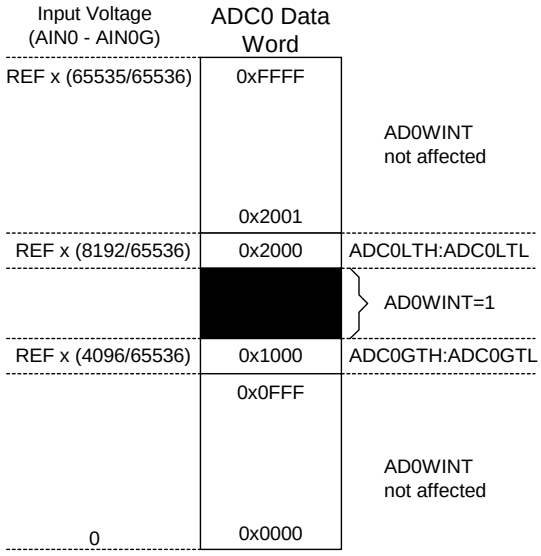


R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

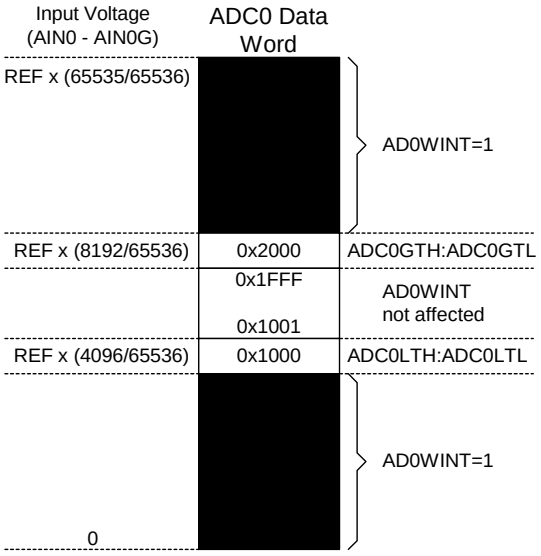
SFR Address: 0xBB
SFR Page: F

Bits 7-0: Calibration Coefficients at the location specified in ADC0CPT. See Table 5.19.

Figure 5.28. 16-Bit ADC0 Window Interrupt Example: Single-Ended Data



Given:
AMX0SL = 0x00,
ADC0LTH:ADC0LTL = 0x2000,
ADC0GTH:ADC0GTL = 0x1000.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = ‘1’) if the resulting ADC0 Data Word is < 0x2000 and > 0x1000.



Given:
AMX0SL = 0x00,
ADC0LTH:ADC0LTL = 0x1000,
ADC0GTH:ADC0GTL = 0x2000.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = ‘1’) if the resulting ADC0 Data Word is > 0x2000 or < 0x1000.

Table 5.2. 16-Bit ADC0 and ADC1 Electrical Characteristics

VDD = 3.0 V, AV+ = 3.0 V, AVDD = 3.0 V, VREF = 2.50 V (REFBE=0), -40 to +85 °C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			16		bits
Integral Nonlinearity (C8051F060/1/4/5/6/7)	Single-Ended Differential		±0.75 ±0.5	±2 ±1	LSB
Integral Nonlinearity (C8051F062/3)	Single-Ended Differential		±1.5 ±1	±4 ±2	LSB
Differential Nonlinearity	Guaranteed Monotonic		±0.5		LSB
Offset Error			0.1		mV
Full Scale Error			0.008		%F.S.
Gain Temperature Coefficient			0.5		ppm/°C
Dynamic Performance (Sampling Rate = 1 Msps, AVDD, AV+ = 3.3V)					
Signal-to-Noise Plus Distortion	Fin = 10 kHz, Single-Ended Fin = 100 kHz, Single-Ended Fin = 10 kHz, Differential Fin = 100 kHz, Differential		86 84 89 88		dB dB dB dB
Total Harmonic Distortion	Fin = 10 kHz, Single-Ended Fin = 100 kHz, Single-Ended Fin = 10 kHz, Differential Fin = 100 kHz, Differential		96 84 103 93		dB dB dB dB
Spurious-Free Dynamic Range	Fin = 10 kHz, Single-Ended Fin = 100 kHz, Single-Ended Fin = 10 kHz, Differential Fin = 100 kHz, Differential		97 88 104 99		dB dB dB dB
CMRR	Fin = 10 kHz		86		dB
Channel Isolation			100		dB
Timing					
SAR Clock Frequency				25	MHz
Conversion Time in SAR Clocks		18			clocks
Track/Hold Acquisition Time		280			ns
Throughput Rate				1	Msps
Aperture Delay	External CNVST Signal		1.5		ns
RMS Aperture Jitter	External CNVST Signal		5		ps
Analog Inputs					
Input Voltage Range	Single-Ended (AINn - AINnG) Differential (AIN0 - AIN1)	0 -VREF		VREF VREF	V V
Input Capacitance			80		pF

6.5. Instruction Execution in Mode 1

When the DMA interface begins an operation cycle, the DMA Instruction Status Register (DMA0ISW, Figure 6.9) is loaded with the address contained within the DMA Instruction Boundary Register (DMA0BND, Figure 6.8). The instruction is fetched from the Instruction Buffer, and the DMA Control Logic waits for data from the appropriate ADC(s). At the end of an instruction, the Repeat Counter (Registers DMA0CSH and DMA0CSL) is decremented, and the instruction will be repeated until the Repeat Counter reaches 0x0000. The Repeat Counter is then reset to the Repeat Counter Limit value (Registers DMA0CTH and DMA0CTL), and the DMA will increment DMA0ISW to the next instruction address. When the current DMA instruction is an End of Operation instruction, the Instruction Status Register is reset to the Instruction Boundary Register. If the Continuous Conversion bit (bit 7, CCNV) in the End of Operation instruction word is set to '1', the DMA will continue to execute instructions. When CCNV is set to '0', the DMA will stop executing instructions at this point. An example of Mode 1 operation is shown in Figure 6.3.

Figure 6.3. DMA Mode 1 Operation

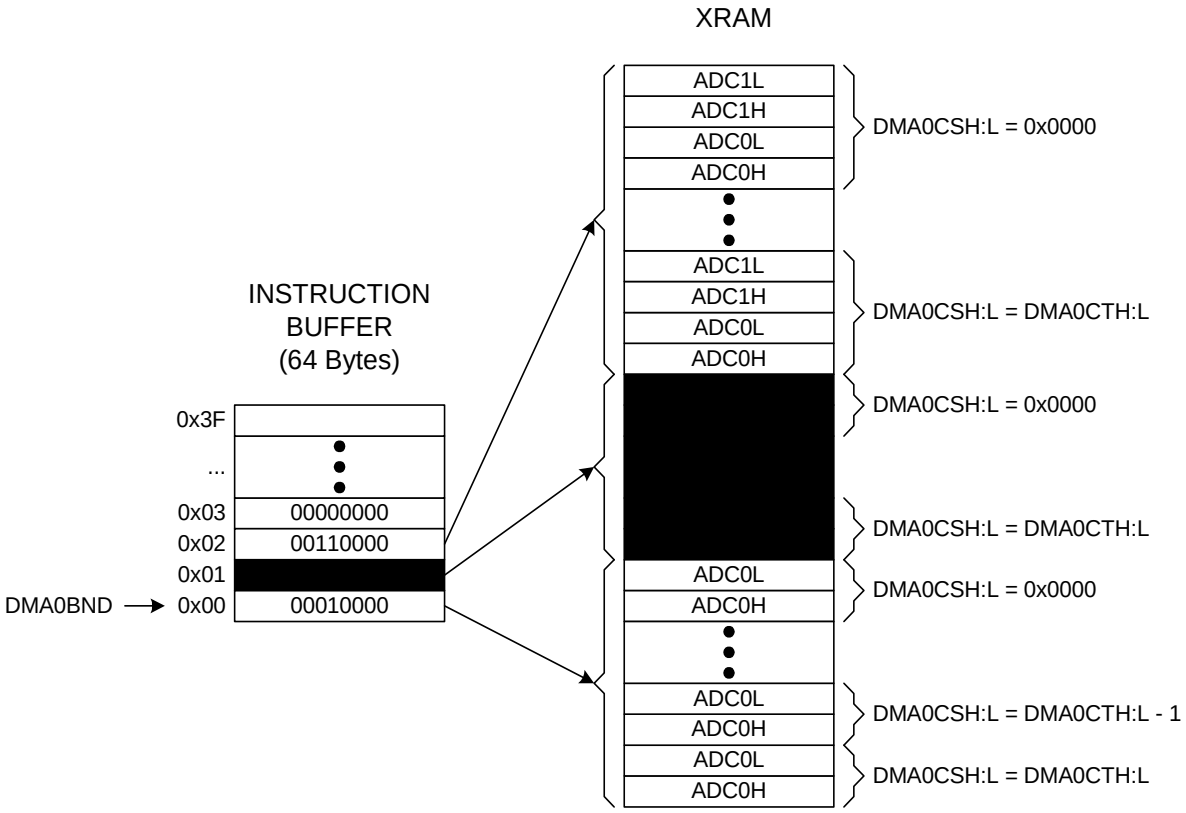


Figure 6.8. DMA0BND: DMA0 Instruction Boundary Register

SFR Page: 3
SFR Address: 0xFD

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-							00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7-6: Unused.
Bits 5-0: DMA0 instruction address to begin with when executing DMA instructions.

Figure 6.9. DMA0ISW: DMA0 Instruction Status Register

SFR Page: 3
SFR Address: 0xFE

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-							00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7-6: Unused.
Bits 5-0: Contains the address of the current DMA0 Instruction to be executed.

Figure 7.6. AMX2SL: AMUX2 Channel Select Register

SFR Page: 2
SFR Address: 0xBB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AMX2AD3	AMX2AD2	AMX2AD1	AMX2AD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7-4: UNUSED. Read = 0000b; Write = don't care.
Bits 3-0: AMX2AD3-0: AMX2 Address Bits.
0000-1111b: ADC input multiplexer channel selected per chart below.

AMX2AD3-0	Single-Ended Measurement		AMX2AD3-0	Differential Measurement	
0000	AIN2.0	AIN01IC = 0	0000	+(AIN2.0) -(AIN2.1)	AIN01IC = 1
0001	AIN2.1		0001	+(AIN2.1) -(AIN2.0)	
0010	AIN2.2	AIN23IC = 0	0010	+(AIN2.2) -(AIN2.3)	AIN23IC = 1
0011	AIN2.3		0011	+(AIN2.3) -(AIN2.2)	
0100	AIN2.4	AIN45IC = 0	0100	+(AIN2.4) -(AIN2.5)	AIN45IC = 1
0101	AIN2.5		0101	+(AIN2.5) -(AIN2.4)	
0110	AIN2.6	AIN67IC = 0	0110	+(AIN2.6) -(AIN2.7)	AIN67IC = 1
0111	AIN2.7		0111	+(AIN2.7) -(AIN2.6)	
1xxx	Temperature Sensor		1xxx	-	

8.1. DAC Output Scheduling

Each DAC features a flexible output update mechanism which allows for seamless full-scale changes and supports jitter-free updates for waveform generation. The following examples are written in terms of DAC0, but DAC1 operation is identical.

8.1.1. Update Output On-Demand

In its default mode (DAC0CN.[4:3] = ‘00’) the DAC0 output is updated “on-demand” on a write to the high-byte of the DAC0 data register (DAC0H). It is important to note that writes to DAC0L are held, and have no effect on the DAC0 output until a write to DAC0H takes place. If writing a full 12-bit word to the DAC data registers, the 12-bit data word is written to the low byte (DAC0L) and high byte (DAC0H) data registers. Data is latched into DAC0 after a write to the corresponding DAC0H register, **so the write sequence should be DAC0L followed by DAC0H** if the full 12-bit resolution is required. The DAC can be used in 8-bit mode by initializing DAC0L to the desired value (typically 0x00), and writing data to only DAC0H (also see Section 8.2 for information on formatting the 12-bit DAC data word within the 16-bit SFR space).

8.1.2. Update Output Based on Timer Overflow

Similar to the ADC operation, in which an ADC conversion can be initiated by a timer overflow independently of the processor, the DAC outputs can use a Timer overflow to schedule an output update event. This feature is useful in systems where the DAC is used to generate a waveform of a defined sampling rate by eliminating the effects of variable interrupt latency and instruction execution on the timing of the DAC output. When the DAC0MD bits (DAC0CN.[4:3]) are set to ‘01’, ‘10’, or ‘11’, writes to both DAC data registers (DAC0L and DAC0H) are held until an associated Timer overflow event (Timer 3, Timer 4, or Timer 2, respectively) occurs, at which time the DAC0H:DAC0L contents are copied to the DAC input latches allowing the DAC output to change to the new value.

8.2. DAC Output Scaling/Justification

In some instances, input data should be shifted prior to a DAC0 write operation to properly justify data within the DAC input registers. This action would typically require one or more load and shift operations, adding software overhead and slowing DAC throughput. To alleviate this problem, the data-formatting feature provides a means for the user to program the orientation of the DAC0 data word within data registers DAC0H and DAC0L. The three DAC0DF bits (DAC0CN.[2:0]) allow the user to specify one of five data word orientations as shown in the DAC0CN register definition.

DAC1 is functionally the same as DAC0 described above. The electrical specifications for both DAC0 and DAC1 are given in Table 8.1.

Figure 13.21. EIE1: Extended Interrupt Enable 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
EADC0	CP2IE	CP1IE	CP0IE	EPCA0	EWADC0	ESMB0	ESPI0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE6
SFR Page: All Pages

Bit7: EADC0: Enable ADC0 End of Conversion Interrupt.
This bit sets the masking of the ADC0 End of Conversion Interrupt.
0: Disable ADC0 Conversion Interrupt.
1: Enable interrupt requests generated by the ADC1 Conversion Interrupt.

Bit6: CP2IE: Enable Comparator (CP2) Interrupt.
This bit sets the masking of the CP2 interrupt.
0: Disable CP2 interrupts.
1: Enable interrupt requests generated by the CP2IF flag.

Bit6: CP1IE: Enable Comparator (CP1) Interrupt.
This bit sets the masking of the CP1 interrupt.
0: Disable CP1 interrupts.
1: Enable interrupt requests generated by the CP1IF flag.

Bit6: CP0IE: Enable Comparator (CP0) Interrupt.
This bit sets the masking of the CP0 interrupt.
0: Disable CP0 interrupts.
1: Enable interrupt requests generated by the CP0IF flag.

Bit3: EPCA0: Enable Programmable Counter Array (PCA0) Interrupt.
This bit sets the masking of the PCA0 interrupts.
0: Disable all PCA0 interrupts.
1: Enable interrupt requests generated by PCA0.

Bit2: EWADC0: Enable Window Comparison ADC0 Interrupt.
This bit sets the masking of ADC0 Window Comparison interrupt.
0: Disable ADC0 Window Comparison Interrupt.
1: Enable Interrupt requests generated by ADC0 Window Comparisons.

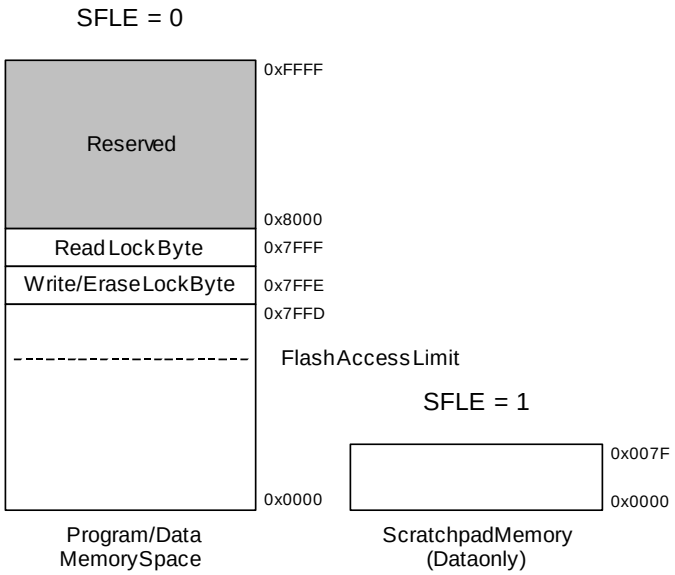
Bit1: ESMB0: Enable System Management Bus (SMBus0) Interrupt.
This bit sets the masking of the SMBus interrupt.
0: Disable all SMBus interrupts.
1: Enable interrupt requests generated by the SI flag.

Bit0: ESPI0: Enable Serial Peripheral Interface (SPI0) Interrupt.
This bit sets the masking of SPI0 interrupt.
0: Disable all SPI0 interrupts.
1: Enable Interrupt requests generated by the SPI0 flag.

Figure 16.2. C8051F066/7 Flash Program Memory Map and Security Bytes

Read and Write/Erase Security Bits
(Bit 7 is MSB)

Bit	Memory Block
7	N/A
6	N/A
5	N/A
4	N/A
3	0x6000-0x7FFD
2	0x4000-0x5FFF
1	0x2000-0x3FFF
0	0x0000-0x1FFF



Flash Read Lock Byte

Bits7-0: Each bit locks a corresponding block of memory.

0: Read operations are locked (disabled) for corresponding block across the JTAG interface.

1: Read operations are unlocked (enabled) for corresponding block across the JTAG interface.

Flash Write/Erase Lock Byte

Bits7-0: Each bit locks a corresponding block of memory.

0: Write/Erase operations are locked (disabled) for corresponding block across the JTAG interface.

1: Write/Erase operations are unlocked (enabled) for corresponding block across the JTAG interface.

NOTE: When the block containing the security bytes is locked, the security bytes may be written but not erased.

Flash Access Limit Register (FLACL)

The Flash Access Limit is defined by the setting of the FLACL register, as described in Figure 16.3. Firmware running at or above this address is prohibited from using the MOVX and MOVC instructions to read, write, or erase Flash locations below this address.

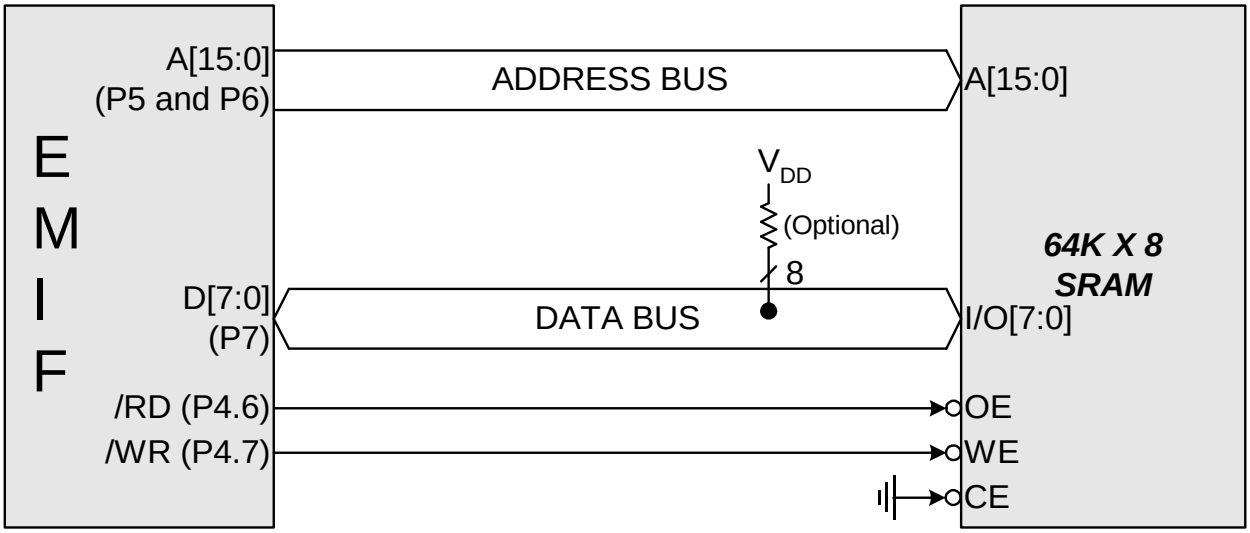
The Flash Access Limit security feature (see Figure 16.3) protects proprietary program code and data from being read by software running on the C8051F060/1/2/3/4/5/6/7. This feature provides support for OEMs that wish to program the MCU with proprietary value-added firmware before distribution. The value-added firmware can be protected while allowing additional code to be programmed in remaining program memory space later.

The Flash Access Limit (FAL) is a 16-bit address that establishes two logical partitions in the program memory space. The first is an upper partition consisting of all the program memory locations at or above the FAL address, and the second is a lower partition consisting of all the program memory locations start-

17.4.2. Non-multiplexed Configuration

In Non-multiplexed mode, the Data Bus and the Address Bus pins are not shared. An example of a Non-multiplexed Configuration is shown in Figure 17.4. See Section “17.6.1. Non-multiplexed Mode” on page 196 for more information about Non-multiplexed operation.

Figure 17.4. Non-multiplexed Configuration Example



ing a logic 1 to the Weak Pull-up Disable bit, (WEAKPUD, XBR2.7). The weak pull-up is automatically deactivated on any pin that is driving a logic 0; that is, an output pin will not contend with its own pull-up device.

18.2.5. External Memory Interface

If the External Memory Interface is enabled on the High ports and an off-chip MOVX operation occurs, the External Memory Interface will control the output states of the affected Port pins during the execution phase of the MOVX instruction, regardless of the settings of the Port Data registers. The output configuration of the Port pins is not affected by the EMIF operation, except that Read operations will explicitly disable the output drivers on the Data Bus during the MOVX execution. See Section “17. External Data Memory Interface and On-Chip XRAM” on page 187 for more information about the External Memory Interface.

Figure 18.21. P5: Port5 Data Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xD8
SFR Page: F

Bits7-0: P5.[7:0]: Port5 Output Latch Bits.
Write - Output appears on I/O pins.
0: Logic Low Output.
1: Logic High Output (open, if corresponding P5MDOUT bit = 0). See Figure 18.22.
Read - Returns states of I/O pins.
0: P5.n pin is logic low.
1: P5.n pin is logic high.

Note: P5.[7:0] can be driven by the External Data Memory Interface (as Address[15:8] in Non-multiplexed mode). See Section “17. External Data Memory Interface and On-Chip XRAM” on page 187 for more information about the External Memory Interface.

Figure 18.22. P5MDOUT: Port5 Output Mode Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x9D
SFR Page: F

Bits7-0: P5MDOUT.[7:0]: Port5 Output Mode Bits.
0: Port Pin output mode is configured as Open-Drain.
1: Port Pin output mode is configured as Push-Pull.

28 SMBus0 states, along with their corresponding status codes, are given in Table 1.1.

Figure 20.12. SMB0STA: SMBus0 Status Register

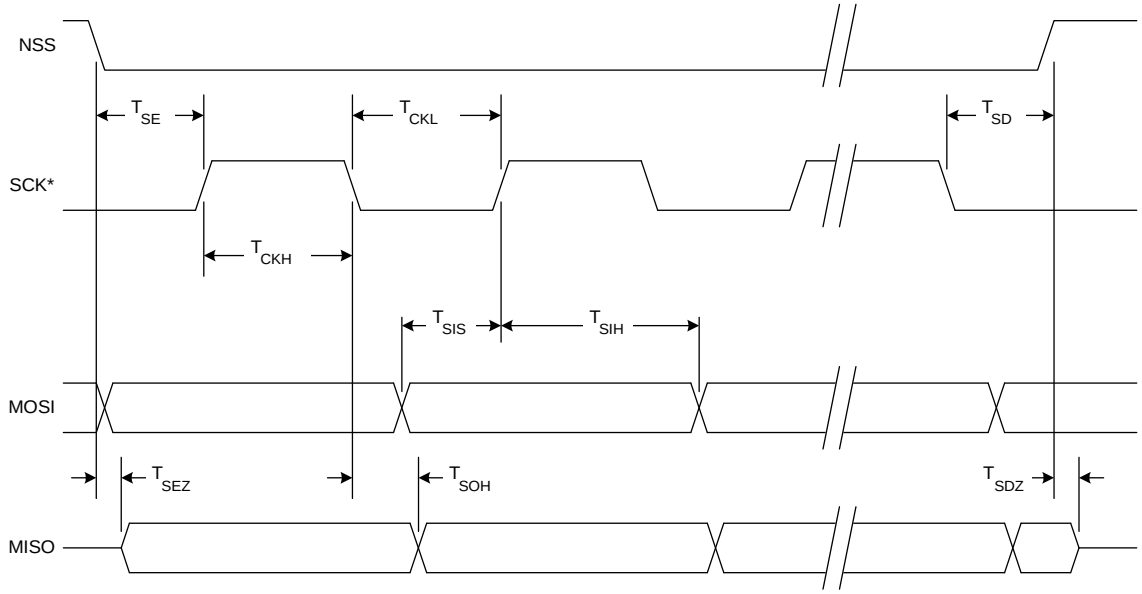
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0	11111000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC1
SFR Page: 0

Bits7-3: STA7-STA3: SMBus0 Status Code.
These bits contain the SMBus0 Status Code. There are 28 possible status codes; each status code corresponds to a single SMBus state. A valid status code is present in SMB0STA when the SI flag (SMB0CN.3) is set to logic 1. The content of SMB0STA is not defined when the SI flag is logic 0. Writing to the SMB0STA register at any time will yield indeterminate results.

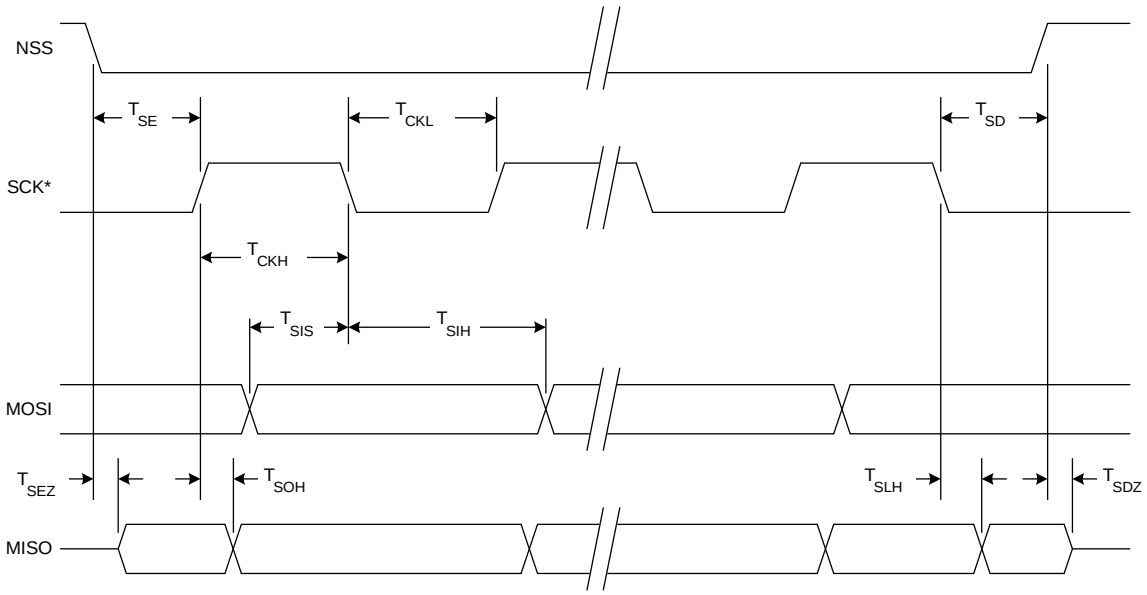
Bits2-0: STA2-STA0: The three least significant bits of SMB0STA are always read as logic 0 when the SI flag is logic 1.

Figure 21.14. SPI Slave Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 21.15. SPI Slave Timing (CKPHA = 1)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 25.11. PCA0MD: PCA0 Mode Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CIDL	-	-	-	CPS2	CPS1	CPS0	ECF	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD9
SFR Page: 0

Bit7: CIDL: PCA0 Counter/Timer Idle Control.
Specifies PCA0 behavior when CPU is in Idle Mode.
0: PCA0 continues to function normally while the system controller is in Idle Mode.
1: PCA0 operation is suspended while the system controller is in Idle Mode.

Bits6-4: UNUSED. Read = 000b, Write = don't care.

Bits3-1: CPS2-CPS0: PCA0 Counter/Timer Pulse Select.
These bits select the timebase source for the PCA0 counter

CPS2	CPS1	CPS0	Timebase
0	0	0	System clock divided by 12
0	0	1	System clock divided by 4
0	1	0	Timer 0 overflow
0	1	1	High-to-low transitions on ECI (max rate = system clock divided by 4)
1	0	0	System clock
1	0	1	External clock divided by 8†
1	1	0	Reserved
1	1	1	Reserved

Bit0: ECF: PCA Counter/Timer Overflow Interrupt Enable.
This bit sets the masking of the PCA0 Counter/Timer Overflow (CF) interrupt.
0: Disable the CF interrupt.
1: Enable a PCA0 Counter/Timer Overflow interrupt request when CF (PCA0CN.7) is set.

†Note: External clock divided by 8 is synchronized with the system clock, and external clock must be less than or equal to the system clock frequency to operate in this mode.