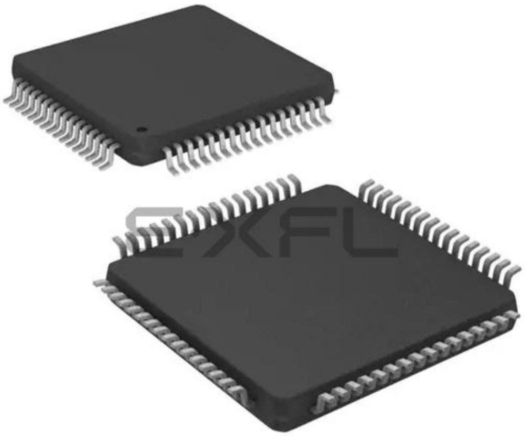
Silicon Labs - C8051F067-GQ Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f067-gq

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F06x family of devices utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The core has all the peripherals included with a standard 8052, including five 16-bit counter/timers, two full-duplex UARTs, 256 bytes of internal RAM, 128 byte Special Function Register (SFR) address space, and bit-addressable I/O Ports.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.5 shows a comparison of peak throughputs of various 8-bit microcontroller cores with their maximum system clocks.

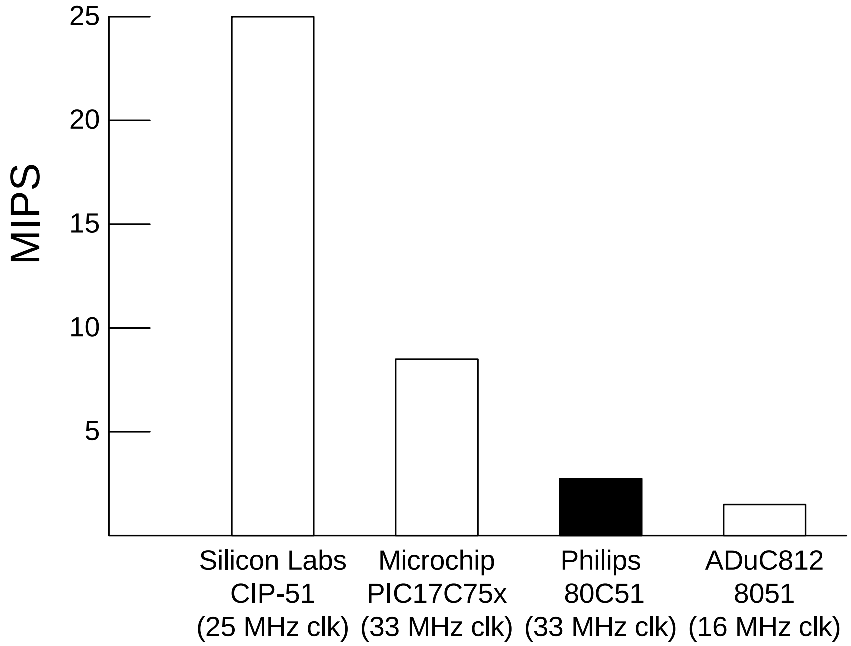


Figure 1.5. Comparison of Peak MCU Execution Speeds

1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The CIP-51 SFR address space contains up to 256 *SFR Pages*. In this way, the CIP-51 MCU can accommodate the many SFRs required to control and configure the various peripherals featured on the device. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

The CIP-51 in the C8051F060/1/2/3/4/5/6/7 MCUs additionally has an on-chip 4 kB RAM block. The on-chip 4 kB block can be addressed over the entire 64 k external data memory address range (overlapping 4 k boundaries). The C8051F060/2/4/6 also have an external memory interface (EMIF) for accessing off-chip data memory or memory-mapped peripherals. External data memory address space can be mapped to on-chip memory only, off-chip memory only, or a combination of the two (addresses up to 4 k directed to on-chip, above 4 k directed to EMIF). The EMIF is also configurable for multiplexed or non-multiplexed address/data lines.

The MCU's program memory consists of 64 k (C8051F060/1/2/3/4/5) or 32 k (C8051F066/7) of Flash. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. On the C8051F060/1/2/3/4/5, the 1024 bytes from addresses 0xFC00 to 0xFFFF are reserved. There is also a single 128 byte Scratchpad Memory sector on all devices which may be used by firmware for non-volatile data storage. See Figure 1.7 for the MCU system memory map.

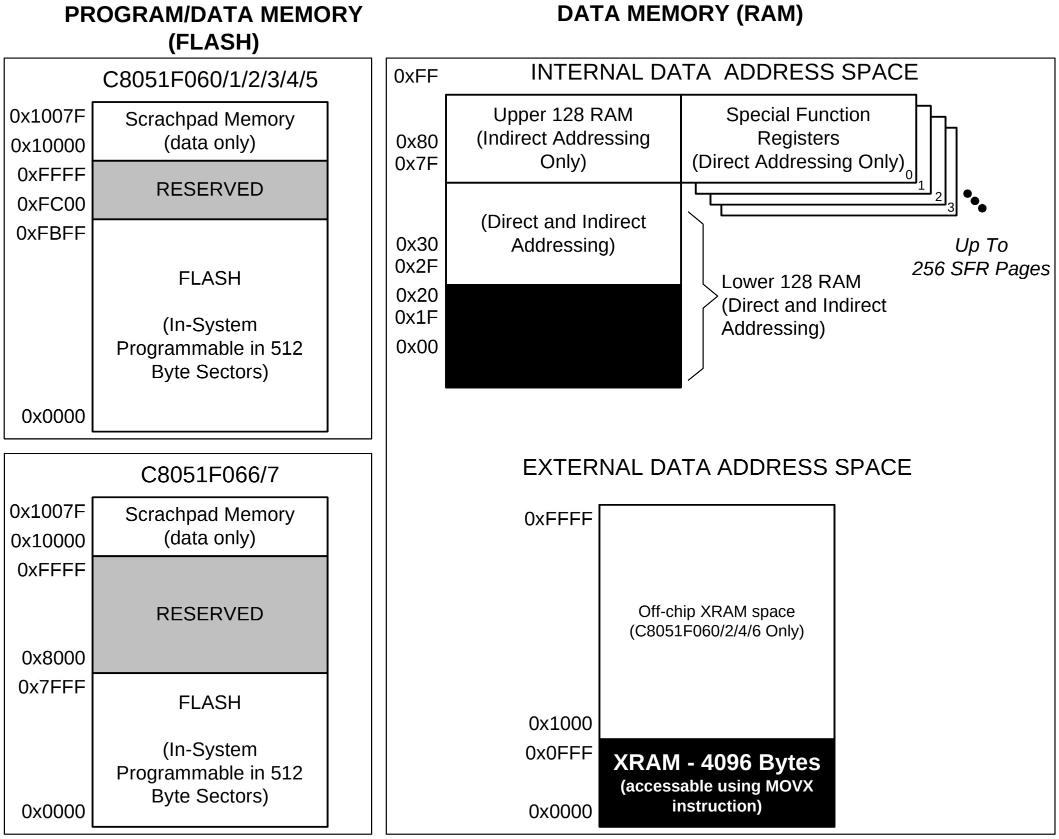

PROGRAM/DATA MEMORY (FLASH)
C8051F060/1/2/3/4/5
0x1007F
0x10000
Scrachpad Memory (data only)
0xFFFF
0xFC00
RESERVED
0xFBFF
FLASH
(In-System Programmable in 512 Byte Sectors)
0x0000
C8051F066/7
0x1007F
0x10000
Scrachpad Memory (data only)
0xFFFF
RESERVED
0x8000
0x7FFF
FLASH
(In-System Programmable in 512 Byte Sectors)
0x0000
DATA MEMORY (RAM)
INTERNAL DATA ADDRESS SPACE
0xFF
0x80
0x7F
Upper 128 RAM (Indirect Addressing Only)
Special Function Registers (Direct Addressing Only)
0
1
2
3
Up To 256 SFR Pages
0x30
0x2F
0x20
0x1F
0x00
(Direct and Indirect Addressing)
Lower 128 RAM (Direct and Indirect Addressing)
EXTERNAL DATA ADDRESS SPACE
0xFFFF
Off-chip XRAM space (C8051F060/2/4/6 Only)
0x1000
0x0FFF
XRAM - 4096 Bytes (accessable using MOVX instruction)
0x0000

Figure 1.7. On-Chip Memory Map

1.9. 10-Bit Analog to Digital Converter

The C8051F060/1/2/3 devices have an on-board 10-bit SAR ADC (ADC2) with a 9-channel input multiplexer and programmable gain amplifier. This ADC features a 200 ksps maximum throughput and true 10-bit performance with an INL of ±1LSB. Eight input pins are available for measurement and can be programmed as single-ended or differential inputs. Additionally, the on-chip temperature sensor can be used as an input to the ADC. The ADC is under full control of the CIP-51 microcontroller via the Special Function Registers. The ADC2 voltage reference is selected between the analog power supply (AV+) and the external VREF2 pin. User software may put ADC2 into shutdown mode to save power.

A flexible conversion scheduling system allows ADC2 conversions to be initiated by software commands, timer overflows, or an external input signal. Conversion completions are indicated by a status bit and an interrupt (if enabled), and the resulting 10-bit data word is latched into two SFR locations upon completion.

ADC2 also contains Window Compare registers, which can be configured to interrupt the controller when ADC2 data is within or outside of a specified range. ADC2 can monitor a key voltage continuously in background mode, and not interrupt the controller unless the converted data is within the specified window.

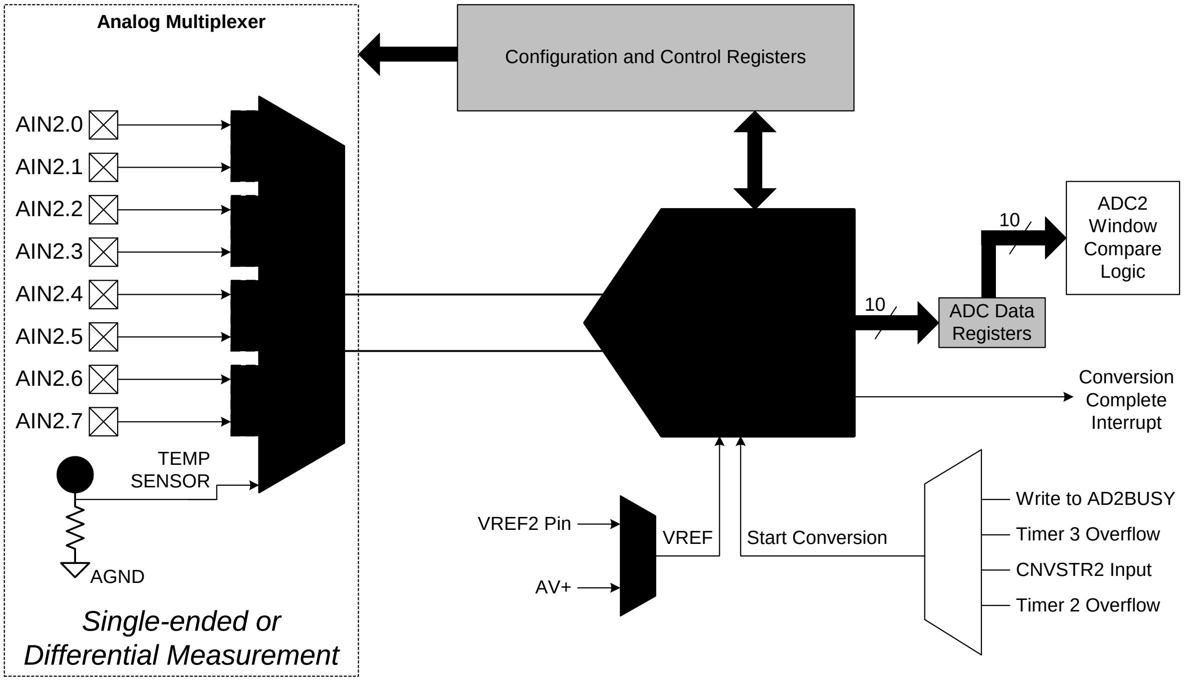


Figure 1.13. 10-Bit ADC Diagram

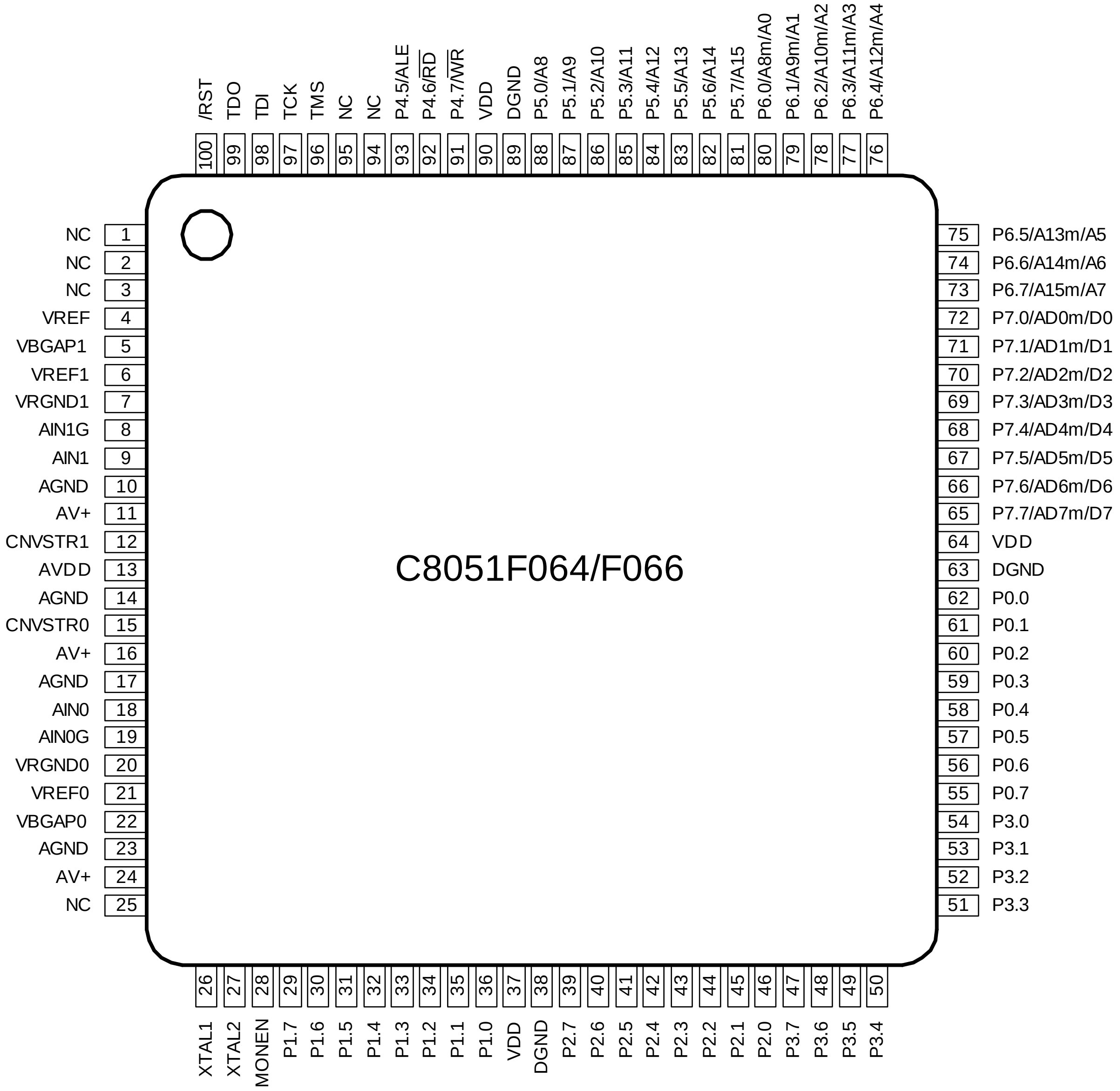


Figure 4.2. C8051F064 / C8051F066 Pinout Diagram (TQFP-100)

Figure 5.16. ADC1H: ADC1 Data Word MSB Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBF
SFR Page: 1

Bits 7-0: ADC1 Data Word High-Order Bits.

Figure 5.17. ADC1L: ADC1 Data Word LSB Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBE
SFR Page: 1

Bits 7-0: ADC1 Data Word Low-Order Bits.

Figure 5.18. ADC1 Data Word Example

16-bit ADC1 Data Word appears in the ADC1 Data Word Registers as follows:

Example: ADC1 Data Word Conversion Map, AIN1 Input in Single-Ended Mode (AMX1SL = 0x00)

AIN1-AIN1G (Volts)	**ADC1H:ADC1L**
VREF * (65535/65536)	0xFFFF
VREF / 2	0x8000
VREF * (32767/65536)	0x7FFF
0	0x0000

$$Code = Vin \times \frac{Gain}{VREF} \times 2^{n} \qquad \text{; ‘n’ = 16}$$

For differential mode, the differential data word appears in ADC0H and ADC0L. The single-ended ADC1 results are always present in ADC1H and ADC1L, regardless of the operating mode.

5.5. ADC0 Programmable Window Detector

The ADC0 Programmable Window Detector continuously compares the ADC0 output to user-programmed limits, and notifies the system when an out-of-bound condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD0WINT in ADC0CN) can also be used in polled mode. The high and low bytes of the reference words are loaded into the ADC0 Greater-Than and ADC0 Less-Than registers (ADC0GTH, ADC0GTL, ADC0LTH, and ADC0LTL). The Window Detector can be used in single-ended or differential mode. In signle-ended mode, the Window Detector compares the ADC0GTx and ADC0LTx registers to the output of ADC0. In differential mode, the combined output of ADC0 and ADC1 (contained in the ADC0 data registers) is used for the comparison. Reference comparisons are shown starting on page 71. Notice that the window detector flag can be asserted when the measured data is inside or outside the user-programmed limits, depending on the programming of the ADC0GTx and ADC0LTx registers.

Figure 5.24. ADC0GTH: ADC0 Greater-Than Data High Byte Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC5
SFR Page: 0

Bits 7-0: High byte of ADC0 Greater-Than Data Word.

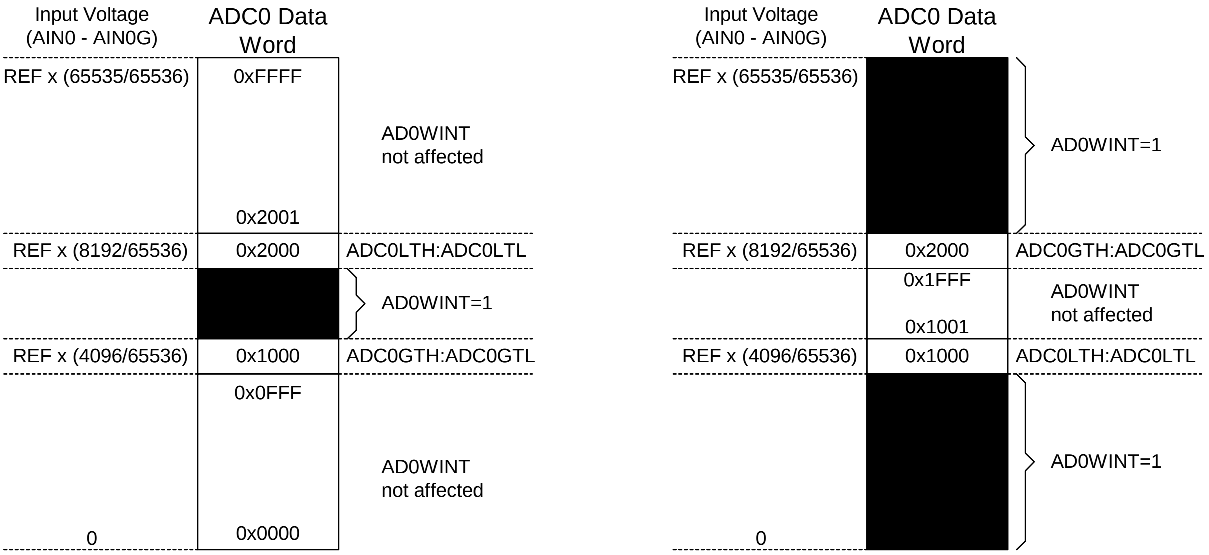
Figure 5.25. ADC0GTL: ADC0 Greater-Than Data Low Byte Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC4
SFR Page: 0

Bits 7-0: Low byte of ADC0 Greater-Than Data Word.

Figure 5.28. 16-Bit ADC0 Window Interrupt Example: Single-Ended Data



Given:
AMX0SL = 0x00,
ADC0LTH:ADC0LTL = 0x2000,
ADC0GTH:ADC0GTL = 0x1000.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = ‘1’) if the resulting ADC0 Data Word is < 0x2000 and > 0x1000.

Given:
AMX0SL = 0x00,
ADC0LTH:ADC0LTL = 0x1000,
ADC0GTH:ADC0GTL = 0x2000.
An ADC0 End of Conversion will cause an ADC0 Window Compare Interrupt (AD0WINT = ‘1’) if the resulting ADC0 Data Word is > 0x2000 or < 0x1000.

Figure 7.6. AMX2SL: AMUX2 Channel Select Register

SFR Page: 2
SFR Address: 0xBB

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AMX2AD3	AMX2AD2	AMX2AD1	AMX2AD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7-4: UNUSED. Read = 0000b; Write = don’t care.
Bits 3-0: AMX2AD3-0: AMX2 Address Bits.
0000-1111b: ADC input multiplexer channel selected per chart below.

AMX2AD3-0	Single-Ended Measurement		AMX2AD3-0	Differential Measurement	
0000	AIN2.0	AIN01IC = 0	0000	+(AIN2.0) -(AIN2.1)	AIN01IC = 1
0001	AIN2.1		0001	+(AIN2.1) -(AIN2.0)	
0010	AIN2.2	AIN23IC = 0	0010	+(AIN2.2) -(AIN2.3)	AIN23IC = 1
0011	AIN2.3		0011	+(AIN2.3) -(AIN2.2)	
0100	AIN2.4	AIN45IC = 0	0100	+(AIN2.4) -(AIN2.5)	AIN45IC = 1
0101	AIN2.5		0101	+(AIN2.5) -(AIN2.4)	
0110	AIN2.6	AIN67IC = 0	0110	+(AIN2.6) -(AIN2.7)	AIN67IC = 1
0111	AIN2.7		0111	+(AIN2.7) -(AIN2.6)	
1xxx	Temperature Sensor		1xxx	-	

Comparator interrupts can be generated on either rising-edge and falling-edge output transitions. (For Interrupt enable and priority control, see Section “13.3. Interrupt Handler” on page 151). The rising and/or falling -edge interrupts are enabled using the comparator’s Rising/Falling Edge Interrupt Enable Bits (CPnRIE and CPnFIE) in their respective Comparator Mode Selection Register (CPTnMD), shown in Figure 12.4. These bits allow the user to control which edge (or both) will cause a comparator interrupt. However, the comparator interrupt must also be enabled in the Extended Interrupt Enable Register (EIE1). The CPnFIF flag is set to logic 1 upon a Comparator falling-edge interrupt, and the CPnRIF flag is set to logic 1 upon the Comparator rising-edge interrupt. Once set, these bits remain set until cleared by software. The output state of a Comparator can be obtained at any time by reading the CPnOUT bit. A Comparator is enabled by setting its respective CPnEN bit to logic 1, and is disabled by clearing this bit to logic 0.Upon enabling a comparator, the output of the comparator is not immediately valid. Before using a comparator as an interrupt or reset source, software should wait for a minimum of the specified “Power-up time” as specified in Table 12.1, “Comparator Electrical Characteristics,” on page 122.

12.1. Comparator Inputs

The Port pins selected as comparator inputs should be configured as analog inputs in the Port 2 Input Configuration Register (for details on Port configuration, see Section “18.1.3. Configuring Port Pins as Digital Inputs” on page 207). The inputs for Comparator are on Port 2 as follows:

Comparator Input	Port PIN
CP0 +	P2.6
CP0 -	P2.7
CP1 +	P2.2
CP1 -	P2.3
CP2 +	P2.4
CP2 -	P2.5

Figure 12.3. CPTnCN: Comparator 0, 1, and 2 Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CPnEN	CPnOUT	CPnRIF	CPnFIF	CPnHYP1	CPnHYP0	CPnHYN1	CPnHYN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: CPT0CN: 0x88; CPT1CN: 0x88; CPT2CN: 0x88
SFR Pages: CPT0CN: page 1; CPT1CN: page 2; CPT2CN: page 3

Bit7: CPnEN: Comparator Enable Bit. **(Please see note below.)**
0: Comparator Disabled.
1: Comparator Enabled.

Bit6: CPnOUT: Comparator Output State Flag.
0: Voltage on CPn+ < CPn-.
1: Voltage on CPn+ > CPn-.

Bit5: CPnRIF: Comparator Rising-Edge Interrupt Flag.
0: No Comparator Rising Edge Interrupt has occurred since this flag was last cleared.
1: Comparator Rising Edge Interrupt has occurred. Must be cleared by software.

Bit4: CPnFIF: Comparator Falling-Edge Interrupt Flag.
0: No Comparator Falling-Edge Interrupt has occurred since this flag was last cleared.
1: Comparator Falling-Edge Interrupt has occurred. Must be cleared by software.

Bits3-2: CPnHYP1-0: Comparator Positive Hysteresis Control Bits.
00: Positive Hysteresis Disabled.
01: Positive Hysteresis = 5 mV.
10: Positive Hysteresis = 10 mV.
11: Positive Hysteresis = 20 mV.

Bits1-0: CPnHYN1-0: Comparator Negative Hysteresis Control Bits.
00: Negative Hysteresis Disabled.
01: Negative Hysteresis = 5 mV.
10: Negative Hysteresis = 10 mV.
11: Negative Hysteresis = 20 mV.

NOTE: Upon enabling a comparator, the output of the comparator is not immediately valid. Before using a comparator as an interrupt or reset source, software should wait for a minimum of the specified “Power-up time” as specified in Table 12.1, “Comparator Electrical Characteristics,” on page 122.

Figure 12.4. CPTnMD: Comparator Mode Selection Register

R/W	R/W	R/W	R/W	R	R	R/W	R/W	Reset Value
-	-	CPnRIE	CPnFIE	-	-	CPnMD1	CPnMD0	00000010
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: CPT0MD: 0x89; CPT1MD: 0x89; CPT2MD: 0x89
SFR Page: CPT0MD: page 1; CPT1MD: page 2; CPT2MD: page 3

Bits7-6: UNUSED. Read = 00b, Write = don’t care.
Bit 5: CPnRIE: Comparator Rising-Edge Interrupt Enable Bit.
0: Comparator rising-edge interrupt disabled.
1: Comparator rising-edge interrupt enabled.
Bit 4: CPnFIE: Comparator Falling-Edge Interrupt Enable Bit.
0: Comparator falling-edge interrupt disabled.
1: Comparator falling-edge interrupt enabled.
Bits3-2: UNUSED. Read = 00b, Write = don’t care.
Bits1-0: CPnMD1-CPnMD0: Comparator Mode Select
These bits select the response time for the Comparator.

Mode	CPnMD1	CPnMD0	Notes
0	0	0	Fastest Response Time
1	0	1	-
2	1	0	-
3	1	1	Lowest Power Consumption

14. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External port pins are forced to a known configuration
- Interrupts and timers are disabled.

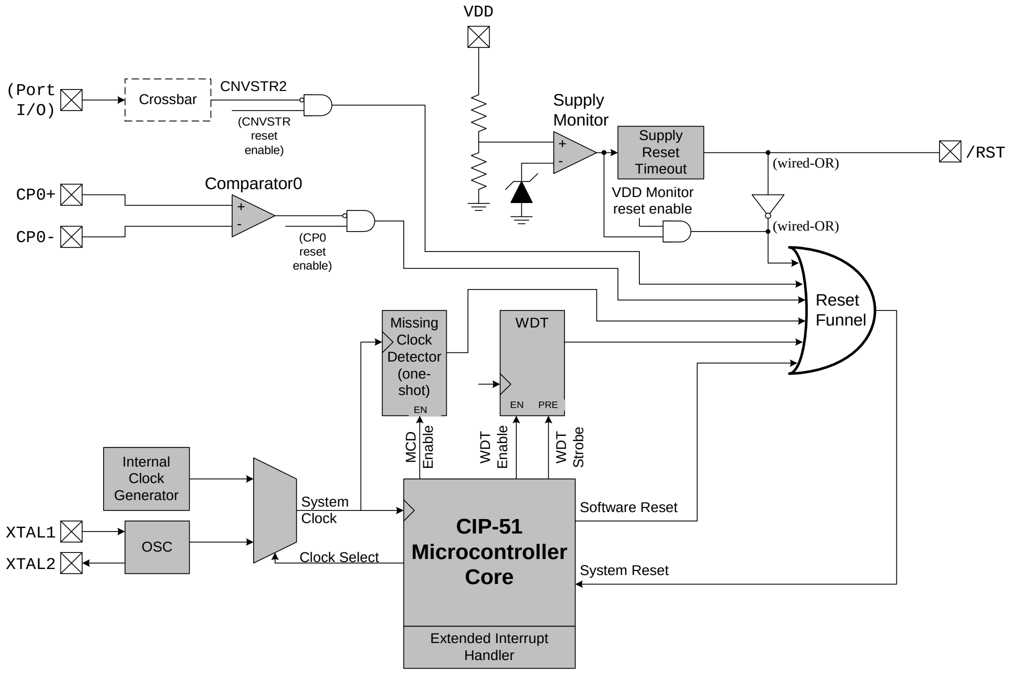
All SFRs are reset to the predefined values noted in the SFR detailed descriptions. The contents of internal data memory are unaffected during a reset; any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost even though the data on the stack are not altered.

The I/O port latches are reset to 0xFF (all logic 1's), activating internal weak pull-ups which take the external I/O pins to a high state. The external I/O pins do not go high immediately, but will go high within four system clock cycles after entering the reset state. This allows power to be conserved while the part is held in reset. For VDD Monitor resets, the /RST pin is driven low until the end of the VDD reset timeout.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal oscillator running at its lowest frequency. Refer to Section “15. Oscillators” on page 171 for information on selecting and configuring the system clock source. The Watchdog Timer is enabled using its longest timeout interval (see Section “14.7. Watchdog Timer Reset” on page 165). Once the system clock source is stable, program execution begins at location 0x0000.

There are seven sources for putting the MCU into the reset state: power-on, power-fail, external /RST pin, external CNVSTR2 signal, software command, Comparator0, Missing Clock Detector, and Watchdog Timer. Each reset source is described in the following sections.

Figure 14.1. Reset Sources



The Mode 0 baud rate is SYSCLK / 12. RX0 is forced to open-drain in Mode 0, and an external pull-up will typically be required.

Figure 22.2. UART0 Mode 0 Timing Diagram

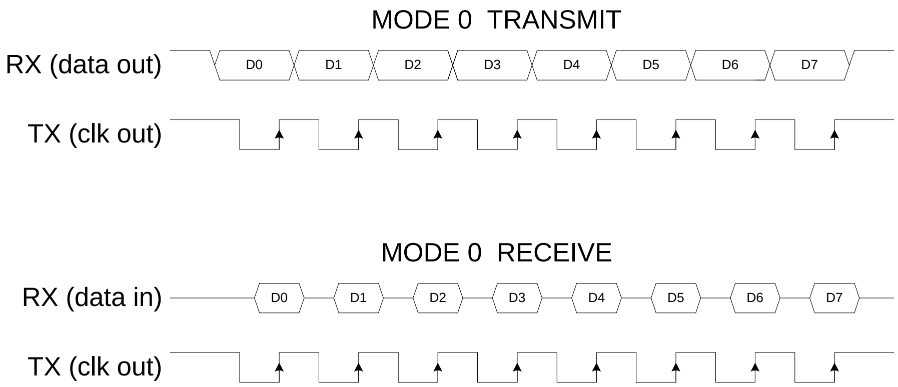
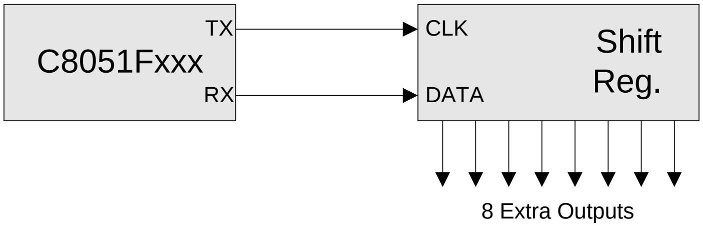


Figure 22.3. UART0 Mode 0 Interconnect



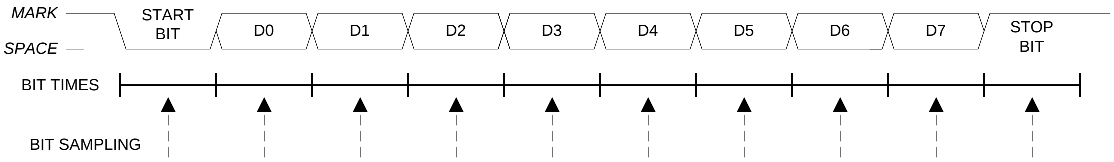
22.1.2. Mode 1: 8-Bit UART, Variable Baud Rate

Mode 1 provides standard asynchronous, full duplex communication using a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted from the TX0 pin and received at the RX0 pin. On receive, the eight data bits are stored in SBUF0 and the stop bit goes into RB80 (SCON0.2).

Data transmission begins when an instruction writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: RI0 must be logic 0, and if SM20 is logic 1, the stop bit must be logic 1.

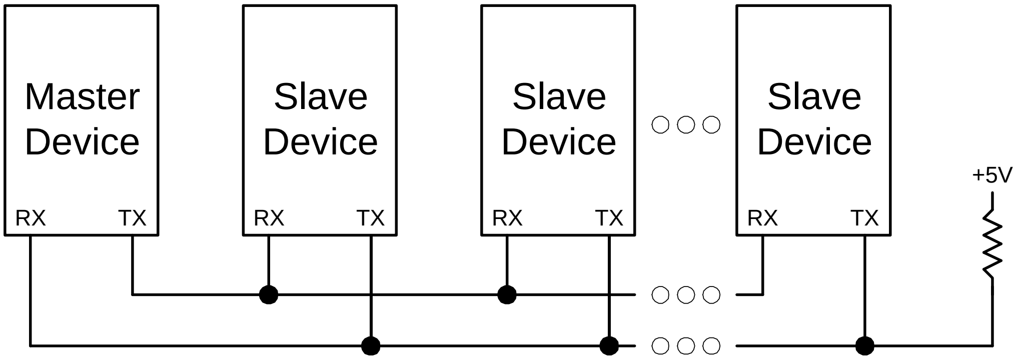
If these conditions are met, the eight bits of data is stored in SBUF0, the stop bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either TI0 or RI0 are set.

Figure 22.4. UART0 Mode 1 Timing Diagram



address as valid. If a master were to then send an address of "11111111", all three slave devices would recognize the address as a valid broadcast address.

Figure 22.7. UART Multi-Processor Mode Interconnect Diagram



22.3. Frame and Transmission Error Detection

All Modes:
The Transmit Collision bit (TXCOL0 bit in register SCON0) reads '1' if user software writes data to the SBUF0 register while a transmit is in progress. Note that the TXCOL0 bit is also used as the SM20 bit when written by user software. This bit does not generate an interrupt.

Modes 1, 2, and 3:

The Receive Overrun bit (RXOV0 in register SCON0) reads '1' if a new data byte is latched into the receive buffer before software has read the previous byte. Note that the RXOV0 bit is also used as the SM10 bit when written by user software. The Frame Error bit (FE0 in register SSTA0) reads '1' if an invalid (low) STOP bit is detected. Note that the FE0 bit is also used as the SM00 bit when written by user software. The RXOV0 and FE0 bits do not generate interrupts.

Figure 23.7. SCON1: Serial Port 1 Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
S1MODE	-	MCE1	REN1	TB81	RB81	TI1	RI1	01000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x98
SFR Page: 1

Bit7: S1MODE: Serial Port 1 Operation Mode.
This bit selects the UART1 Operation Mode.
0: 8-bit UART with Variable Baud Rate.
1: 9-bit UART with Variable Baud Rate.

Bit6: UNUSED. Read = 1b. Write = don’t care.

Bit5: MCE1: Multiprocessor Communication Enable.
The function of this bit is dependent on the Serial Port 0 Operation Mode.
S1MODE = 0: Checks for valid stop bit.
0: Logic level of stop bit is ignored.
1: RI1 will only be activated if stop bit is logic level 1.
S1MODE = 1: Multiprocessor Communications Enable.
0: Logic level of ninth bit is ignored.
1: RI1 is set and an interrupt is generated only when the ninth bit is logic 1.

Bit4: REN1: Receive Enable.
This bit enables/disables the UART receiver.
0: UART1 reception disabled.
1: UART1 reception enabled.

Bit3: TB81: Ninth Transmission Bit.
The logic level of this bit will be assigned to the ninth transmission bit in 9-bit UART Mode. It is not used in 8-bit UART Mode. Set or cleared by software as required.

Bit2: RB81: Ninth Receive Bit.
RB81 is assigned the value of the STOP bit in Mode 0; it is assigned the value of the 9th data bit in Mode 1.

Bit1: TI1: Transmit Interrupt Flag.
Set by hardware when a byte of data has been transmitted by UART1 (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART1 interrupt is enabled, setting this bit causes the CPU to vector to the UART1 interrupt service routine. This bit must be cleared manually by software.

Bit0: RI1: Receive Interrupt Flag.
Set to ‘1’ by hardware when a byte of data has been received by UART1 (set at the STOP bit sampling time). When the UART1 interrupt is enabled, setting this bit to ‘1’ causes the CPU to vector to the UART1 interrupt service routine. This bit must be cleared manually by software.