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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15344-e-ss

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Name	Function	Input Type	Output Type	Description
RA0/ANA0/C1IN0+/DAC1OUT/	RA0	TTL/ST	CMOS/OD	General purpose I/O.
ICSPDAT/IOCAU	ANA0	AN	_	ADC Channel A0 input.
	C1IN0+	AN	_	Comparator 1 positive input.
	DAC1OUT	_	AN	Digital-to-Analog Converter output.
	ICSPDAT	ST	CMOS	In-Circuit Serial Programming [™] and debugging data input/ output.
	IOCA0	TTL/ST	—	Interrupt-on-change input.
RA1/ANA1/VREF+/C1IN0-/C2IN0-/	RA1	TTL/ST	CMOS/OD	General purpose I/O.
DAG IREFTITUCKI, TICSF CENTOCAT	ANA1	AN	—	ADC Channel A1 input.
	VREF+	AN	_	External ADC and/or DAC positive reference input.
	C1IN0-	AN	_	Comparator 1 negative input.
	C2IN0-	AN	—	Comparator 2 negative input.
	DAC1REF+	TTL/ST	AN	DAC positive reference.
	T0CKI ⁽¹⁾	TTL/ST	_	Timer0 clock input.
	ICSPCLK	ST	_	In-Circuit Serial Programming™ and debugging clock input.
	IOCA1	TTL/ST	_	Interrupt-on-change input.
RA2/ANA2/CWG1IN ⁽¹⁾ /ZCD1/INT ⁽¹⁾ /	RA2	TTL/ST	CMOS/OD	General purpose I/O.
IUGAZ	ANA2	AN	_	ADC Channel A2 input.
	CWG1IN ⁽¹⁾	TTL/ST	_	Complementary Waveform Generator 1 input.
	ZCD1	AN	AN	Zero-cross detect input pin (with constant current sink/ source).
	INT ⁽¹⁾	TTL/ST	_	External interrupt request input.
	IOCA2	TTL/ST	_	Interrupt-on-change input.
RA3/MCLR/Vpp/IOCA3	RA3	TTL/ST	CMOS/OD	General purpose I/O.
	MCLR	ST	_	Master clear input with internal weak pull up resistor.
	Vpp	HV	_	ICSP™ High-Voltage Programming mode entry input.
	IOCA3	TTL/ST	—	Interrupt-on-change input.
RA4/ANA4/C1IN1-/T1G ⁽¹⁾ /CLKOUT/	RA4	TTL/ST	CMOS/OD	General purpose I/O.
0502/10044	ANA4	AN	_	ADC Channel A4 input.
	C1IN1-	AN	_	Comparator 1 negative input.
	T1G ⁽¹⁾	ST	_	Timer1 Gate input.
	CLKOUT	_	CMOS/OD	Fosc/4 digital output (in non-crystal/resonator modes).
	OSC2	—	XTAL	External Crystal/Resonator (LP, XT, HS modes) driver output.
	IOCA4	TTL/ST	_	Interrupt-on-change input.
Legend: AN = Analog input or outp TTL = TTL compatible input	out CMOS = ut ST =	CMOS cor Schmitt Tr	npatible input or ou igger input with CM	utput OD = Open-Drain /OS levels I ² C = Schmitt Trigger input with I ² C

TABLE 1-2: PIC16(L)F15324 PINOUT DESCRIPTION

 HV = High Voltage
 XTAL = Crystal levels

 This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to Table 15-3 for details on which PORT pins may be used for this signal.

 1:

All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin 2:

options as described in Table 15-3. This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and 3: PPS output registers.

These pins are configured for l^2C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, but input logic levels will be standard TTL/ST, as selected by the INLVL register, 4: instead of the I²C specific or SMBus input buffer thresholds.

Note

TABLE 4-7: PIC16(L)F15324/44 MEMORY MAP, BANKS 56-63

	BANK 56		BANK 57		BANK 58		BANK 59		BANK 60		BANK 61		BANK 62		BANK 63	
1C00h	Core Register (Table 4-3)	1C80h	Core Register (Table 4-3)	1D00h	Core Register (Table 4-3)	1D80h	Core Register (Table 4-3)	1E00h	Core Register (Table 4-3)	1E80h	Core Register (Table 4-3)	1F00h	Core Register (Table 4-3)	1F80h	Core Register (Table 4-3)	
1C0BH		1C8Ch		1D0BH 1D0Ch		1Dobii 1D8Ch		1E0Bh		1E0DII 1E8Ch		1F0DII 1F0Ch		1F8Ch		
1C0Dh		1C8Dh		1D00h		D8Dh1		1E00h		1E8Dh		1F0Dh		1F8Dh		
1C0Eh	_	1C8Eh	_	1D0Eh	_	1D8Eh		1E0Eh		1E8Eh		1F0Eh		1F8Eh		
1C0Fh	_	1C8Fh	_	1D0Fh	_	1D8Fh		1E0Fh		1E8Fh		1F0Fh		1F8Fh		
1C10h	—	1C90h	_	1D10h	_	1D90h	—	1E10h		1E90h		1F10h		1F90h		
1C11h	_	1C91h	_	1D11h	_	1D91h	_	1E11h		1E91h		1F11h		1F91h		
1C12h	_	1C92h		1D12h	_	1D92h	_	1E12h		1E92h		1F12h		1F92h		
1C13h	_	1C93h	—	1D13h	—	1D93h	—	1E13h		1E93h		1F13h		1F93h		
1C14h	—	1C94h	—	1D14h	—	1D94h	_	1E14h		1E94h		1F14h		1F94h		
1C15h	—	1C95h	—	1D15h	—	1D95h	_	1E15h		1E95h		1F15h		1F95h		
1C16h	—	1C96h	—	1D16h	—	1D96h	—	1E16h		1E96h		1F16h	5 550 0 / I	1F96h		
1C17h	—	1C97h	—	1D17h	—	1D97h	—	1E17h	CLC Controls	1E97h	nnnPPS Controls	1F17h	RxyPPS Controls	1F97h	(See Table 4-8 for	
1C18h	—	1C98h	_	1D18h	_	1D98h	—	1E18h	(See Table 4-8 for	1E98h	(See Table 4-8 for	1F18h	(See Table 4-8 for	1F98h	register mapping	
1C19h	_	1C99h	_	1D19h	_	1D99h		1E19h	register mapping	1E99h	register mapping	1F19h	register mapping	1F99h	details)	
1C1Ah	—	1C9Ah	_	1D1Ah	—	1D9Ah		1E1Ah	details)	1E9Ah	details)	1F1Ah	details)	1F9Ah		
1C1Bh	_	1C9Bh	_	1D1Bh	_	1D9Bh		1E1Bh		1E9Bh		1F1Bh		1F9Bh		
1C1Ch	—	1C9Ch	—	1D1Ch	_	1D9Ch		1E1Ch		1E9Ch		1F1Ch		1F9Ch		
1C1Dh	—	1C9Dh	—	1D1Dh	_	1D9Dh		1E1Dh		1E9Dh		1F1Dh		1F9Dh		
1C1Eh	_	1C9Eh	_	1D1Eh	_	1D9Eh		1E1Eh		1E9Eh		1F1Eh		1F9Eh		
1C1Fh	—	1C9Fh	—	1D1Fh	—	1D9Fh	—	1E1Fh		1E9Fh		1F1Fh		1F9Fh		
1C20h		1CA0h		1D20h		1DA0h		1E20h		1EA0h		1F20h		1FA0h		
	Unimplemented Read as '0'		Unimplemented Read as '0'		Unimplemented Read as '0'		Unimplemented Read as '0'									
1C6Fh		1CEFh		1D6Fh		1DEFh		1E6Fh		1EEFh		1F6Fh		1FEFh		
1C70h	Common RAM	1CF0h	Common RAM	1D70h	Common RAM	1DF0h	Common RAM	1E70h	Common RAM	1EF0h	Common RAM	1F70h	Common RAM	1FF0h	Common RAM	
	Accesses		Accesses		Accesses		Accesses		Accesses		Accesses		Accesses		Accesses	
1C7Fh	70h-7Fh	1CFFh	70h-7Fh	1D7Fh	70h-7Fh	1DFFh	70h-7Fh	1E7Fh	70h-7Fh	1EFFh	70h-7Fh	1F7Fh	70h-7Fh	1FFFh	70h-7Fh	

Note 1: Unimplemented locations read as '0'.

2: The banks 24-55 have been omitted from the tables in the data sheet since the banks have unimplemented registers.

TABLE 4-10:	SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-63 (CONTINUED)	

						•	,					
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	V <u>alue o</u> n: MCLR	
Bank 12	.k 12											
	CPU CORE REGISTERS; see Table 4-3 for specifics											
60Ch	CWG1CLKCON	_	—	—	_	—	_	—	CS	0	0	
60Dh	CWG1DAT	—	—	— — DAT<3:0>						0000	0000	
60Eh	CWG1DBR	—	—		DBR<5:0>						00 0000	
60Fh	CWG1DBF	—	—		DBF<5:0>						00 0000	
610h	CWG1CON0	EN	LD	_	—	—		MODE<2:0>		00000	00000	
611h	CWG1CON1	—	—	IN	—	POLD	POLC	POLB	POLA	x- 0000	u- 0000	
612h	CWG1AS0	SHUTDOWN	REN	LSBD	<2:0>	LSAC	<2:0>	—	_	0001 01	0001 01	
613h	CWG1AS1	—	—	_	AS4E	AS3E	AS2E	AS1E	AS0E	0 0000	u 0000	
614h	CWG1STR	OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA	0000 0000	0000 0000	
315hUnimplemented							_	_				

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

4.5 Stack

All devices have a 16-level x 15-bit wide hardware stack (refer to Figure 4-4 through Figure 4-7). The stack space is not part of either program or data space. The PC is PUSHed onto the stack when CALL or CALLW instructions are executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer if the STVREN bit is programmed to '0' (Configuration Words). This means that after the stack has been PUSHed sixteen times, the seventeenth PUSH overwrites the value that was stored from the first PUSH. The eighteenth PUSH overwrites the second PUSH (and so on). The STKOVF and STKUNF flag bits will be set on an Overflow/Underflow, regardless of whether the Reset is enabled.

Note 1: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, CALLW, RETURN, RETLW and RETFIE instructions or the vectoring to an interrupt address.

4.5.1 ACCESSING THE STACK

The stack is accessible through the TOSH, TOSL and STKPTR registers. STKPTR is the current value of the Stack Pointer. TOSH:TOSL register pair points to the TOP of the stack. Both registers are read/writable. TOS is split into TOSH and TOSL due to the 15-bit size of the PC. To access the stack, adjust the value of STKPTR, which will position TOSH:TOSL, then read/write to TOSH:TOSL. STKPTR is five bits to allow detection of overflow and underflow.

Note:	Care should be taken when modifying the
	STKPTR while interrupts are enabled.

During normal program operation, CALL, CALLW and interrupts will increment STKPTR while RETLW, RETURN, and RETFIE will decrement STKPTR. STKPTR can be monitored to obtain to value of stack memory left at any given time. The STKPTR always points at the currently used place on the stack. Therefore, a CALL or CALLW will increment the STKPTR and then write the PC, and a return will unload the PC value from the stack and then decrement the STKPTR.

Reference Figure 4-4 through Figure 4-7 for examples of accessing the stack.



6.1 Microchip Unique identifier (MUI)

The PIC16(L)F15324/44 devices are individually encoded during final manufacturing with a Microchip Unique Identifier, or MUI. The MUI cannot be erased by a Bulk Erase command or any other user-accessible means. This feature allows for manufacturing traceability of Microchip Technology devices in applications where this is a required. It may also be used by the application manufacturer for a number of functions that require unverified unique identification, such as:

- Tracking the device
- Unique serial number

The MUI consists of nine program words. When taken together, these fields form a unique identifier. The MUI is stored in nine read-only locations, located between 8100h to 8109h in the DIA space. Table 6-1 lists the addresses of the identifier words.

Note:	For applications that require verified unique				
	identification, contact your Microchip Tech-				
	nology sales office to create a Serialized				
	Quick Turn Programming option.				

6.2 External Unique Identifier (EUI)

The EUI data is stored at locations 810Ah to 8111h in the program memory region. This region is an optional space for placing application specific information. The data is coded per customer requirements during manufacturing. The EUI cannot be erased by a Bulk Erase command.

Note: Data is stored in this address range on receiving a request from the customer. The customer may contact the local sales representative or Field Applications Engineer, and provide them the unique identifier information that is required to be stored in this region.

6.3 Analog-to-Digital Conversion Data of the Temperature Sensor

The purpose of the temperature indicator module is to provide a temperature-dependent voltage that can be measured by an analog module. Section 19.0 "Temperature Indicator Module" explains the operation of the Temperature Indicator module and defines terms such as the low range and high range settings of the sensor.

The DIA table contains the internal ADC measurement values of the temperature sensor for low and high range at fixed points of reference. The values are measured during test and are unique to each device. The right-justified ADC readings are stored in the DIA memory region. The calibration data can be used to plot the approximate sensor output voltage, VTSENSE vs. Temperature curve.

- **TSLR<3:1>**: Address 8112h to 8114h store the measurements for the low range setting of the temperature sensor at VDD = 3V.
- TSHR<3:1>: Address 8115h to 8117h store the measurements for the high range setting of the temperature sensor at VDD = 3V.

The stored measurements are made by the device ADC using the internal VREF = 2.048V.

6.4 Fixed Voltage Reference Data

The Fixed Voltage Reference, or FVR, is a stable voltage reference, independent of VDD, with 1.024V, 2.048V or 4.096V selectable output levels. The output of the FVR can be configured to supply a reference voltage to the following:

- ADC input channel
- ADC positive reference
- Comparator positive input
- Digital-to-Analog Converter

For more information on the FVR, refer to Section 18.0 "Fixed Voltage Reference (FVR)".

The DIA stores measured FVR voltages for this device in mV for the different buffer settings of 1x, 2x or 4x at program memory locations 8118h to 811Dh.

- FVRA1X stores the value of ADC FVR1 Output voltage for 1x setting (in mV)
- FVRA2X stores the value of ADC FVR1 Output Voltage for 2x setting (in mV)
- FVRA4X stores the value of ADC FVR1 Output Voltage for 4x setting (in mV)
- FVRC1X stores the value of Comparator FVR2 output voltage for 1x setting (in mV)
- FVRC2X stores the value of Comparator FVR2 output voltage for 2x setting (in mV)
- FVRC4X stores the value of Comparator FVR2 output voltage for 4x setting (in mV)

9.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a precision digitally-controlled internal clock source that produces a stable clock up to 32 MHz. The HFINTOSC can be enabled through one of the following methods:

- Programming the RSTOSC<2:0> bits in Configuration Word 1 to '110' (1 MHz) or '001' (32 MHz) to set the oscillator upon device Power-up or Reset.
- Write to the NOSC<2:0> bits of the OSCCON1 register during run-time.

The HFINTOSC frequency can be selected by setting the HFFRQ<2:0> bits of the OSCFRQ register. The MFINTOSC is an internal clock source within the HFINTOSC that provides two (500 kHz, 32 kHz) constant clock outputs. These constant clock outputs are available for selection to various peripherals, internally.

The NDIV<3:0> bits of the OSCCON1 register allow for division of the HFINTOSC output from a range between 1:1 and 1:512.

9.2.2.2 Internal Oscillator Frequency Adjustment

The internal oscillator is factory-calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 9-7).

The default value of the OSCTUNE register is 00h. The value is a 6-bit two's complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

9.2.2.3 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is a factory-calibrated 31 kHz internal clock source. The LFINTOSC is the clock source for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM). The LFINTOSC can also be used as the system clock, or as a clock or input source to certain peripherals.

The LFINTOSC is selected as the clock source through one of the following methods:

- Programming the RSTOSC<2:0> bits of Configuration Word 1 to enable LFINTOSC.
- Write to the NOSC<2:0> bits of the OSCCON1 register.

9.2.2.4 Oscillator Status and Manual Enable

The 'ready' status of each oscillator is displayed in the OSCSTAT register (Register 9-4). The oscillators can also be manually enabled through the OSCEN register (Register 9-7). Manual enabling makes it possible to verify the operation of the EXTOSC oscillator. This can be achieved by enabling the selected oscillator, then watching the corresponding 'ready' state of the oscillator in the OSCSTAT register.

PIC16(L)F15324/44

REGISTER 9-7: OSCTUNE: HFINTOSC TUNING REGISTER

U-0	U-0	R/W-1/1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0			
—	—		HFTUN<5:0>							
bit 7							bit 0			

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	Unimplemented: Read as '0'.
bit 5-0	HFTUN<5:0>: HFINTOSC Frequency Tuning bits 01 1111 = Maximum frequency 01 1110 =
	•••
	 00 0001 = 00 0000 = Center frequency. Oscillator module is running at the calibrated frequency (default value). 11 1111 =
	•••
	10 0001 = 10 0000 = Minimum frequency.

11.2.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source, with the exception of the clock switch interrupt, has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the execution of a SLEEP instruction
 - SLEEP instruction will execute as a NOP
 - WDT and WDT prescaler will not be cleared
 - TO bit of the STATUS register will not be set
 - PD bit of the STATUS register will not be cleared

- If the interrupt occurs **during or after** the execution of a **SLEEP** instruction
 - SLEEP instruction will be completely executed
 - Device will immediately wake-up from Sleep
 - WDT and WDT prescaler will be cleared
 - TO bit of the STATUS register will be set
 - PD bit of the STATUS register will be cleared

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.



FIGURE 11-2: WAKE-UP FROM SLEEP THROUGH INTERRUPT

11.2.3 LOW-POWER SLEEP MODE

The PIC16F15324/44 device contains an internal Low Dropout (LDO) voltage regulator, which allows the device I/O pins to operate at voltages up to 5.5V while the internal device logic operates at a lower voltage. The LDO and its associated reference circuitry must remain active when the device is in Sleep mode.

The PIC16F15324/44 allows the user to optimize the operating current in Sleep, depending on the application requirements.

Low-Power Sleep mode can be selected by setting the VREGPM bit of the VREGCON register. Depending on the configuration of these bits, the LDO and reference circuitry are placed in a low-power state when the device is in Sleep.

11.2.3.1 Sleep Current vs. Wake-up Time

In the default operating mode, the LDO and reference circuitry remain in the normal configuration while in Sleep. The device is able to exit Sleep mode quickly since all circuits remain active. In Low-Power Sleep mode, when waking-up from Sleep, an extra delay time is required for these circuits to return to the normal configuration and stabilize.

The Low-Power Sleep mode is beneficial for applications that stay in Sleep mode for long periods of time. The Normal mode is beneficial for applications that need to wake from Sleep quickly and frequently.

REGISTER 12-2:	WDTCON1: WATCHDOG TIMER CONTROL REGISTER 1	

U-0	R/W ⁽³⁾ -q/q ⁽¹⁾	R/W ⁽³⁾ -q/q ⁽¹⁾ R/W ⁽³⁾ -q/q ⁽¹⁾	U-0	R/W ⁽⁴⁾ -q/q ⁽²⁾	R/W ⁽⁴⁾ -q/q ⁽²⁾	R/W ⁽⁴⁾ -q/q ⁽²⁾
-		WDTCS<2:0>	-		WINDOW<2:0>	
bit 7						bit 0
Legend:						
R = Readable bit		W = Writable bit	U = Unimple	mented bit, read	as '0'	
u = Bit is unchanged		x = Bit is unknown	-n/n = Value	er Resets		
'1' = Bit is se	et	'0' = Bit is cleared	q = Value de	pends on conditi	ion	

bit 7 Unimplemented: Read as '0'

bit 6-4 WDTCS<2:0>: Watchdog Timer Clock Select bits

111 = Reserved

•

•

•

010 = Reserved

001 = MFINTOSC 31.25 kHz 000 = LFINTOSC 31 kHz

bit 3 Unimplemented: Read as '0'

bit 2-0 WINDOW<2:0>: Watchdog Timer Window Select bits

WINDOW<2:0>	Window delay Percent of time	Window opening Percent of time
111	N/A	100
110	12.5	87.5
101	25	75
100	37.5	62.5
011	50	50
010	62.5	37.5
001	75	25
000	87.5	12.5

Note 1: If WDTCCS <2:0> in CONFIG3 = 111, the Reset value of WDTCS<2:0> is 000.

2: The Reset value of WINDOW<2:0> is determined by the value of WDTCWS<2:0> in the CONFIG3 register.

3: If WDTCCS<2:0> in CONFIG3 \neq 111, these bits are read-only.

4: If WDTCWS<2:0> in CONFIG3 \neq 111, these bits are read-only.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page	
OSCCON1	—		NOSC<2:0>				114			
OSCCON2	—		COSC<2:0>			114				
OSCCON3	CSWHOLD	—	—	- ORDY NOSCR -		—	—	—	115	
PCON0	STKOVF	STKUNF	WDTWV RWDT RMCLR RI POR BOR		BOR	103				
STATUS	—	_	— <u>TO</u>		PD	Z	DC	С	36	
WDTCON0	—	—			WDTPS<4:0	0>		SWDTEN	154	
WDTCON1	—	V	VDTCS<2:0>		—	WI	>	155		
WDTPSL				PSCN	T<7:0>				156	
WDTPSH		PSCNT<15:8>								
WDTTMR	_		WDTTM	R<4:0>		STATE	PSCNT	<17:16>	156	

TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Legend: – = unimplemented locations read as '0'. Shaded cells are not used by Watchdog Timer.

TABLE 12-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
	13:8	—		FCMEN	_	CSWEN	_	_	CLKOUTEN	00
CONFIG1	7:0	_	F	RSTOSC<2:0	>	—	I	80		

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Watchdog Timer.

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0			
WPUB7	WPUB6	WPUB5	WPUB4	_	_	_	_			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'						
u = Bit is uncha	anged	x = Bit is unkn	nown	-n/n = Value at POR and BOR/Value at all other Resets						
'1' = Bit is set		'0' = Bit is clea	ared							
bit 7-4 WPUB<7:4>: Weak Pull-up Register bits										

REGISTER 14-13: WPUB: WEAK PULL-UP PORTB REGISTER

bit 7-4	WPUB<7:4>: Weak Pull-up Register bits
	1 = Pull-up enabled
	0 = Pull-up disabled
bit 3-0	Unimplemented: Read as '0'

REGISTER 14-14: ODCONB: PORTB OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0				
ODCB7	ODCB6	ODCB5	ODCB4	—	—	—	—				
bit 7 bit 0											

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4	ODCB<7:4>: PORTB Open-Drain Enable bits For RB<7:4> pins, respectively 1 = Port pin operates as open-drain drive (sink current only) 0 = Port pin operates as standard push-pull drive (source and sink current)
bit 3-0	Unimplemented: Read as '0'







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24.7 Operation During Sleep

The ZCD current sources and interrupts are unaffected by Sleep.

24.8 Effects of a Reset

The ZCD circuit can be configured to default to the active or inactive state on Power-on-Reset (POR). When the ZCDDIS Configuration bit is cleared, the ZCD circuit will be active at POR. When the ZCD Configuration bit is set, the EN bit of the ZCDxCON register must be set to enable the ZCD module.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page			
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	125			
PIR5	CLC4IF	CLC3IF	CLC2IF	CLC1IF	—	_	_	TMR1GIF	139			
PIE5	CLC4IE	CLC4IE	CLC2IE CLC1IE — — — TMR1GIE		TMR1GIE	131						
CLC1CON	LC1EN	_	LC10UT LC1INTP LC1INTN LC1MODE<2:0>				366					
CLC1POL	LC1POL	_	_	_	LC1G4POL	LC1G3POL	LC1G2POL	LC1G1POL	367			
CLC1SEL0	_	_			LC1D	1S<5:0>			368			
CLC1SEL1	_	_		LC1D2S<5:0>								
CLC1SEL2	_	_		LC1D3S<5:0>								
CLC1SEL3	_	_		LC1D4S<5:0>								
CLC1GLS0	_	_	LC1G1D3T	LC1G1D3N	LC1G1D2T	LC1G1D2N	LC1G1D1T	LC1G1D1N	369			
CLC1GLS1	_	_	LC1G2D3T	LC1G2D3N	LC1G2D2T	LC1G2D2N	LC1G2D1T	LC1G2D1N	370			
CLC1GLS2	_	_	LC1G3D3T	LC1G3D3N	LC1G3D2T	LC1G3D2N	LC1G3D1T	LC1G3D1N	371			
CLC1GLS3	_	_	LC1G4D3T	LC1G4D3N	LC1G4D2T	LC1G4D2N	LC1G4D1T	LC1G4D1N	372			
CLC2CON	LC2EN	_	LC2OUT LC2INTP LC2INTN LC2MODE<2:0>									
CLC2POL	LC2POL	_	LC2G4POL LC2G3POL LC2G2POL LC2G1POL						367			
CLC2SEL0	_	_		LC2D1S<5:0>								
CLC2SEL1	_	_			LC2D	2S<5:0>			368			
CLC2SEL2	_	_			LC2D	3S<5:0>			368			
CLC2SEL3	_	_			LC2D	4S<5:0>			368			
CLC2GLS0	_	_	LC2G1D3T	LC2G1D3N	LC2G1D2T	LC2G1D2N	LC2G1D1T	LC2G1D1N	369			
CLC2GLS1	_	_	LC2G2D3T	LC2G2D3N	LC2G2D2T	LC2G2D2N	LC2G2D1T	LC2G2D1N	370			
CLC2GLS2	_	_	LC2G3D3T	LC2G3D3N	LC2G3D2T	LC2G3D2N	LC2G3D1T	LC2G3D1N	371			
CLC2GLS3	_	_	LC2G4D3T	LC2G4D3N	LC2G4D2T	LC2G4D2N	LC2G4D1T	LC2G4D1N	372			
CLC3CON	LC3EN	_	LC3OUT	LC3INTP	LC3INTN		LC3MODE<2:0>	>	366			
CLC3POL	LC3POL	_	—	—	LC3G4POL	LC3G3POL	LC3G2POL	LC3G1POL	367			
CLC3SEL0	_	_			LC3D	1S<5:0>			368			
CLC3SEL1	_	_			LC3D	2S<5:0>			368			
CLC3SEL2	_	_			LC3D	3S<5:0>			368			
CLC3SEL3	_	_			LC3D	4S<5:0>			368			
CLC3GLS0	_	_	LC3G1D3T	LC3G1D3N	LC3G1D2T	LC3G1D2N	LC3G1D1T	LC3G1D1N	369			
CLC3GLS1	_	_	LC3G2D3T	LC3G2D3N	LC3G2D2T	LC3G2D2N	LC3G2D1T	LC3G2D1N	370			
CLC3GLS2	_	_	LC3G3D3T	LC3G3D3N	LC3G3D2T	LC3G3D2N	LC3G3D1T	LC3G3D1N	371			
CLC3GLS3	_	_	LC3G4D3T	LC3G4D3N	LC3G4D2T	LC3G4D2N	LC3G4D1T	LC3G4D1N	372			
CLC4CON	LC4EN	_	LC4OUT	LC4INTP	LC4INTN		LC4MODE<2:0>	>	366			
CLC4POL	LC4POL	—	—	—	LC4G4POL	LC4G3POL	LC4G2POL	LC4G1POL	367			
CLC4SEL0	—	—			LC4D	1S<5:0>			368			
CLC4SEL1	—	—			LC4D	2S<5:0>			368			
CLC4SEL2	—	—			LC4D	3S<5:0>			368			
CLC4SEL3	—	—			LC4D	4S<5:0>			368			
CLC4GLS0	—	—	LC4G1D3T	LC4G1D3N	LC4G1D2T	LC4G1D2N	LC4G1D1T	LC4G1D1N	369			

TABLE 31-4: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the CLCx modules.

32.5.3.3 7-bit Transmission with Address Hold Enabled

Setting the AHEN bit of the SSP1CON3 register enables additional clock stretching and interrupt generation after the eighth falling edge of a received matching address. Once a matching address has been clocked in, CKP is cleared and the SSP1IF interrupt is set.

Figure 32-19 displays a standard waveform of a 7-bit address slave transmission with AHEN enabled.

- 1. Bus starts Idle.
- Master sends Start condition; the S bit of SSP1STAT is set; SSP1IF is set if interrupt on Start detect is enabled.
- Master sends matching address with R/W bit set. After the eighth falling edge of the SCL line the CKP bit is cleared and SSP1IF interrupt is generated.
- 4. Slave software clears SSP1IF.
- Slave software reads ACKTIM bit of SSP1CON3 register, and R/W and D/A of the SSP1STAT register to determine the source of the interrupt.
- 6. Slave reads the address value from the SSP1BUF register clearing the BF bit.
- Slave software decides from this information if it wishes to ACK or not ACK and sets the ACKDT bit of the SSP1CON2 register accordingly.
- 8. Slave sets the CKP bit releasing SCL.
- 9. Master clocks in the \overline{ACK} value from the slave.
- 10. Slave hardware automatically clears the CKP bit and sets SSP1IF after the ACK if the R/W bit is set.
- 11. Slave software clears SSP1IF.
- 12. Slave loads value to transmit to the master into SSP1BUF setting the BF bit.

Note: SSP1BUF cannot be loaded until after the ACK.

13. Slave sets the CKP bit releasing the clock.

- 14. Master clocks out the data from the slave and sends an ACK value on the ninth SCL pulse.
- 15. Slave hardware copies the ACK value into the ACKSTAT bit of the SSP1CON2 register.
- 16. Steps 10-15 are repeated for each byte transmitted to the master from the slave.
- 17. If the master sends a not ACK the slave releases the bus allowing the master to send a Stop and end the communication.

Note: Master must send a not ACK on the last byte to ensure that the slave releases the SCL line to receive a Stop.

32.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition (Figure 32-27) occurs when the RSEN bit of the SSP1CON2 register is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSP1CON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSP1STAT register will be set. The SSP1IF bit will not be set until the Baud Rate Generator has timed out.

- Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.
 - **2:** A bus collision during the Repeated Start condition occurs if:
 - SDA is sampled low when SCL goes from low-to-high.
 - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

FIGURE 32-27: REPEATED START CONDITION WAVEFORM



32.6.7 I²C MASTER MODE RECEPTION

Master mode reception (Figure 32-29) is enabled by programming the Receive Enable bit, RCEN bit of the SSP1CON2 register.

Note:	The MSSP module must be in an Idle
	state before the RCEN bit is set or the
	RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSP1SR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSP1SR are loaded into the SSP1BUF, the BF flag bit is set, the SSP1IF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSP1CON2 register.

32.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSP1BUF from SSP1SR. It is cleared when the SSP1BUF register is read.

32.6.7.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when eight bits are received into the SSP1SR and the BF flag bit is already set from a previous reception.

32.6.7.3 WCOL Status Flag

If the user writes the SSP1BUF when a receive is already in progress (i.e., SSP1SR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

- 32.6.7.4 Typical Receive Sequence:
- 1. The user generates a Start condition by setting the SEN bit of the SSP1CON2 register.
- 2. SSP1IF is set by hardware on completion of the Start.
- 3. SSP1IF is cleared by software.
- 4. User writes SSP1BUF with the slave address to transmit and the R/W bit set.
- 5. Address is shifted out the SDA pin until all eight bits are transmitted. Transmission begins as soon as SSP1BUF is written to.
- 6. The MSSP module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSP1CON2 register.
- 7. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSP1IF bit.
- User sets the RCEN bit of the SSP1CON2 register and the master clocks in a byte from the slave.
- 9. After the eighth falling edge of SCL, SSP1IF and BF are set.
- 10. Master clears SSP1IF and reads the received byte from SSP1BUF, clears BF.
- 11. Master sets ACK value sent to slave in ACKDT bit of the SSP1CON2 register and initiates the ACK by setting the ACKEN bit.
- 12. Master's ACK is clocked out to the slave and SSP1IF is set.
- 13. User clears SSP1IF.
- 14. Steps 8-13 are repeated for each received byte from the slave.
- 15. Master sends a not ACK or Stop to end communication.

32.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSP1CON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into IDLE mode (Figure 32-30).

32.6.8.1 WCOL Status Flag

If the user writes the SSP1BUF when an Acknowledge sequence is in progress, then WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

32.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSP1CON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSP1STAT register is set. A TBRG later, the PEN bit is cleared and the SSP1IF bit is set (Figure 32-31).

32.6.9.1 WCOL Status Flag

If the user writes the SSP1BUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 32-30: ACKNOWLEDGE SEQUENCE WAVEFORM



FIGURE 32-31: STOP CONDITION RECEIVE OR TRANSMIT MODE



	SYNC = 0, BRGH = 0, BRG16 = 1											
BAUD	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fos	c = 1.000) MHz
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	299.9	-0.02	1666	300.1	0.04	832	300.0	0.00	767	300.5	0.16	207
1200	1199	-0.08	416	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	_	_
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19.23k	0.16	25	19.23k	0.16	12	19.20k	0.00	11	—	_	_
57.6k	55556	-3.55	8	_	_	_	57.60k	0.00	3	—	_	_
115.2k	—	—	—	—	_	—	115.2k	0.00	1	—	_	_

TABLE 33-4: BAUD RATE FOR ASYNCHRONOUS MODES (CONTINUED)

	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1												
BAUD	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc	= 11.059	92 MHz	
RATE	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	
300	300.0	0.00	26666	300.0	0.00	16665	300.0	0.00	15359	300.0	0.00	9215	
1200	1200	0.00	6666	1200	-0.01	4166	1200	0.00	3839	1200	0.00	2303	
2400	2400	0.01	3332	2400	0.02	2082	2400	0.00	1919	2400	0.00	1151	
9600	9604	0.04	832	9597	-0.03	520	9600	0.00	479	9600	0.00	287	
10417	10417	0.00	767	10417	0.00	479	10425	0.08	441	10433	0.16	264	
19.2k	19.18k	-0.08	416	19.23k	0.16	259	19.20k	0.00	239	19.20k	0.00	143	
57.6k	57.55k	-0.08	138	57.47k	-0.22	86	57.60k	0.00	79	57.60k	0.00	47	
115.2k	115.9k	0.64	68	116.3k	0.94	42	115.2k	0.00	39	115.2k	0.00	23	

	SYNC = 0, BRGH = 1, BRG16 = 1 or SYNC = 1, BRG16 = 1											
BAUD RATE	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	6666	300.0	0.01	3332	300.0	0.00	3071	300.1	0.04	832
1200	1200	-0.02	1666	1200	0.04	832	1200	0.00	767	1202	0.16	207
2400	2401	0.04	832	2398	0.08	416	2400	0.00	383	2404	0.16	103
9600	9615	0.16	207	9615	0.16	103	9600	0.00	95	9615	0.16	25
10417	10417	0	191	10417	0.00	95	10473	0.53	87	10417	0.00	23
19.2k	19.23k	0.16	103	19.23k	0.16	51	19.20k	0.00	47	19.23k	0.16	12
57.6k	57.14k	-0.79	34	58.82k	2.12	16	57.60k	0.00	15	—	_	_
115.2k	117.6k	2.12	16	111.1k	-3.55	8	115.2k	0.00	7	—	_	_

R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0		
CLKREN —		_	CLKRE	C<1:0>		CLKRDIV<2:0>			
bit 7							bit 0		
Legend:									
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'					
u = Bit is uncha	anged	x = Bit is unkr	iown	-n/n = Value at POR and BOR/Value at all other Resets					
'1' = Bit is set		'0' = Bit is clea	ared						
bit 7 bit 6-5 bit 4-3	CLKREN: Reference Clock Module Enable bit 1 = Reference clock module enabled 0 = Reference clock module is disabled Unimplemented: Read as '0' CLKRDC<1:0>: Reference Clock Duty Cycle bits ⁽¹⁾ 11 = Clock outputs duty cycle of 75% 10 = Clock outputs duty cycle of 50% 01 = Clock outputs duty cycle of 25% 00 = Clock outputs duty cycle of 0%								
bit 2-0	CLKRDIV<2:(111 = Base cl 110 = Base cl 101 = Base cl 100 = Base cl 011 = Base cl 010 = Base cl 001 = Base cl 000 = Base cl	D>: Reference lock value divid lock value	Clock Divider led by 128 led by 64 led by 32 led by 16 led by 8 led by 4 led by 2	bits					

REGISTER 34-1: CLKRCON: REFERENCE CLOCK CONTROL REGISTER

Note 1: Bits are valid for reference clock divider values of two or larger, the base clock cannot be further divided.