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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	224 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf15344-i-ss

PIC16(L)F15324/44

TABLE 1: PIC16(L)F153XX FAMILY TYPES

Device	Data Sheet Index	Program Flash Memory (KW)	Program Flash Memory (KB)	Storage Area Flash (B)	Data SRAM (bytes)	I/O Pins	10-bit ADC	5-bit DAC	Comparator	8-bit/ (with HLT) Timer	16-bit Timer	Window Watchdog Timer	CCP/10-bit PWM	CWG	NCO	CLC	Zero-Cross Detect	Temperature Indicator	Memory Access Partition	Device Information Area	EUSART/ I ² C-SPI	Peripheral Pin Select	Peripheral Module Disable	Debug (1)
PIC16(L)F15313	(C)	2	3.5	224	256	6	5	1	1	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	1/1	Y	Y	I
PIC16(L)F15323	(C)	2	3.5	224	256	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	1/1	Y	Y	I
PIC16(L)F15324	(D)	4	7	224	512	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15325	(B)	8	14	224	1024	12	11	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15344	(D)	4	7	224	512	18	17	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15345	(B)	8	14	224	1024	18	17	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/1	Y	Y	I
PIC16(L)F15354	(A)	4	7	224	512	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15355	(A)	8	14	224	1024	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15356	(E)	16	28	224	2048	25	24	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15375	(E)	8	14	224	1024	36	35	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15376	(E)	16	28	224	2048	36	35	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15385	(E)	8	14	224	1024	44	43	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I
PIC16(L)F15386	(E)	16	28	224	2048	44	43	1	2	1	2	Y	2/4	1	1	4	Y	Y	Y	Y	2/2	Y	Y	I

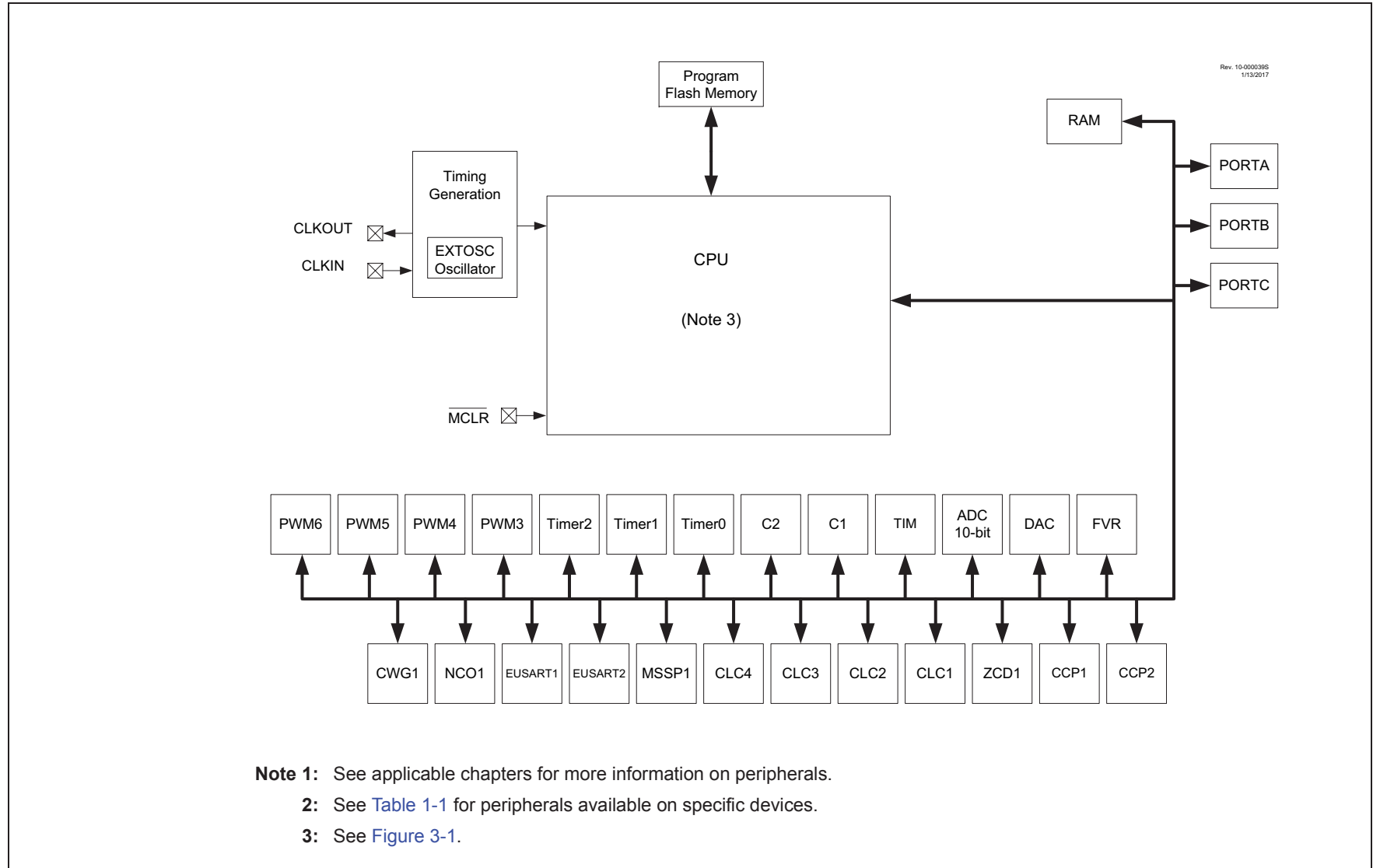
Note 1: I - Debugging integrated on chip.

Data Sheet Index:

- A: DS40001853 PIC16(L)F15354/5 Data Sheet, 28-Pin
- B: DS40001865 PIC16(L)F15325/45 Data Sheet, 14/20-Pin
- C: Future Release PIC16(L)F15313/23 Data Sheet, 8/14-Pin
- D: DS40001889 PIC16(L)F15324/44 Data Sheet, 14/20-Pin
- E: DS40001866 PIC16(L)F15356/75/76/85/86 Data Sheet, 28/40/48-Pin

Note: For other small form-factor package availability and marking information, visit www.microchip.com/packaging or contact your local sales office.

FIGURE 1-2: PIC16(L)F15344 BLOCK DIAGRAM



- Note 1:** See applicable chapters for more information on peripherals.
2: See [Table 1-1](#) for peripherals available on specific devices.
3: See [Figure 3-1](#).

TABLE 1-3: PIC16(L)F15344 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
OUT ⁽²⁾	C1OUT	—	CMOS/OD	Comparator 1 output.
	C2OUT	—	CMOS/OD	Comparator 2 output.
	SDO1	—	CMOS/OD	MSSP1 SPI serial data output.
	SCK1	—	CMOS/OD	MSSP1 SPI serial clock output.
	DT1 ⁽³⁾	—	CMOS/OD	EUSART Synchronous mode data output.
	TX1	—	CMOS/OD	EUSART1 Asynchronous mode transmitter data output.
	CK1	—	CMOS/OD	EUSART1 Synchronous mode clock output.
	DT2 ⁽³⁾	—	CMOS/OD	EUSART Synchronous mode data output.
	TX2	—	CMOS/OD	EUSART2 Asynchronous mode transmitter data output.
	CK2	—	CMOS/OD	EUSART2 Synchronous mode clock output.
	SCL1 ^(3,4)	—	CMOS/OD	MSSP1 I ² C output.
	SDA1 ^(3,4)	—	CMOS/OD	MSSP1 I ² C output.
	TMR0	—	CMOS/OD	Timer0 output.
	CCP1	—	CMOS/OD	CCP1 output (compare/PWM functions).
	CCP2	—	CMOS/OD	CCP2 output (compare/PWM functions).
	PWM3OUT	—	CMOS/OD	PWM3 output.
	PWM4OUT	—	CMOS/OD	PWM4 output.
	PWM5OUT	—	CMOS/OD	PWM5 output.
	PWM6OUT	—	CMOS/OD	PWM6 output.
	CWG1A	—	CMOS/OD	Complementary Waveform Generator 1 output A.
	CWG1B	—	CMOS/OD	Complementary Waveform Generator 1 output B.
	CWG1C	—	CMOS/OD	Complementary Waveform Generator 1 output C.
	CWG1D	—	CMOS/OD	Complementary Waveform Generator 1 output D.
	CLC1OUT	—	CMOS/OD	Configurable Logic Cell 1 output.
	CLC2OUT	—	CMOS/OD	Configurable Logic Cell 2 output.
	CLC3OUT	—	CMOS/OD	Configurable Logic Cell 3 output.
	CLC4OUT	—	CMOS/OD	Configurable Logic Cell 4 output.
NCO1OUT	—	CMOS/OD	Numerically Controller Oscillator output.	
CLKR	—	CMOS/OD	Clock Reference module output.	

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note**
- 1: This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins. Refer to [Table 15-3](#) for details on which PORT pins may be used for this signal.
 - 2: All output signals shown in this row are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options as described in [Table 15-3](#).
 - 3: This is a bidirectional signal. For normal module operation, the firmware should map this signal to the same pin in both the PPS input and PPS output registers.
 - 4: These pins are configured for I²C logic levels. The SCLx/SDAx signals may be assigned to any of the RB1/RB2/RC3/RC4 pins. PPS assignments to the other pins (e.g., RA5) will operate, but input logic levels will be standard TTL/ST, as selected by the INLVL register, instead of the I²C specific or SMBus input buffer thresholds.
 - 5: For 14/16-pin package only.
 - 6: For 20-pin package only.

REGISTER 5-2:
CONFIGURATION WORD 2: SUPERVISORS

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
$\overline{\text{DEBUG}}$	STVREN	PPS1WAY	ZCDDIS	BORV	—
bit 13					bit 8

R/P-1	R/P-1	R/P-1	U-1	U-1	U-1	R/P-1	R/P-1
BOREN1	BOREN0	$\overline{\text{LPBOREN}}$	—	—	—	$\overline{\text{PWRTE}}$	MCLRE
bit 7							bit 0

Legend:

R = Readable bit	P = Programmable bit	x = Bit is unknown	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	W = Writable bit	n = Value when blank or after Bulk Erase

- bit 13 **DEBUG**: Debugger Enable bit
 1 = Background debugger disabled
 0 = Background debugger enabled
- bit 12 **STVREN**: Stack Overflow/Underflow Reset Enable bit
 1 = Stack Overflow or Underflow will cause a Reset
 0 = Stack Overflow or Underflow will not cause a Reset
- bit 11 **PPS1WAY**: PPSLOCK One-Way Set Enable bit
 1 = The PPSLOCK bit can be cleared and set only once; PPS registers remain locked after one clear/set cycle
 0 = The PPSLOCK bit can be set and cleared repeatedly (subject to the unlock sequence)
- bit 10 **ZCDDIS**: Zero-Cross Detect Disable bit
 1 = ZCD disabled. ZCD can be enabled by setting the ZCDSEN bit of the ZCDCON register
 0 = ZCD always enabled (ZCDSEN bit is ignored)
- bit 9 **BORV**: Brown-out Reset Voltage Selection bit⁽¹⁾
 1 = Brown-out Reset voltage (VBOR) set to lower trip point level
 0 = Brown-out Reset voltage (VBOR) set to higher trip point level
- bit 8 **Unimplemented**: Read as '1'
- bit 7-6 **BOREN<1:0>**: Brown-out Reset Enable bits
 When enabled, Brown-out Reset Voltage (VBOR) is set by the BORV bit
 11 = Brown-out Reset is enabled; SBOREN bit is ignored
 10 = Brown-out Reset is enabled while running, disabled in Sleep; SBOREN bit is ignored
 01 = Brown-out Reset is enabled according to SBOREN
 00 = Brown-out Reset is disabled
- bit 5 **LPBOREN**: Low-Power BOR Enable bit
 1 = ULPBOR is disabled
 0 = ULPBOR is enabled
- bit 4-2 **Unimplemented**: Read as '1'
- bit 1 **PWRTE**: Power-up Timer Enable bit
 1 = PWRT is disabled
 0 = PWRT is enabled
- bit 0 **MCLRE**: Master Clear ($\overline{\text{MCLR}}$) Enable bit
 If LVP = 1:
 RE3 pin function is $\overline{\text{MCLR}}$ (it will reset the device when driven low)
 If LVP = 0:
 1 = $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$ (it will reset the device when driven low)
 0 = $\overline{\text{MCLR}}$ pin may be used as general purpose RE3 input

- Note 1:** See [Vbor](#) parameter for specific trip point voltages.
- Note 2:** The **DEBUG** bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.

5.6 Device ID and Revision ID

The 14-bit Device ID word is located at 8006h and the 14-bit Revision ID is located at 8005h. These locations are read-only and cannot be erased or modified.

Development tools, such as device programmers and debuggers, may be used to read the Device ID, Revision ID and Configuration Words. These locations can also be read from the NVMCON register.

5.7 Register Definitions: Device and Revision

REGISTER 5-6: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R
DEV<13:8>					
bit 13			bit 8		

R	R	R	R	R	R	R	R
DEV<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

'1' = Bit is set

'0' = Bit is cleared

bit 13-0 **DEV<13:0>**: Device ID bits

Device	DEVID<13:0> Values
PIC16F15324	11 0000 1100 0010 (30C2h)
PIC16LF15324	11 0000 1100 0011 (30C3h)
PIC16F15344	11 0000 1100 0100 (30C4h)
PIC16LF15344	11 0000 1100 0101 (30C5h)

8.14 Power Control (PCONx) Registers

The Power Control (PCONx) registers contain flag bits to differentiate between a:

- Power-on Reset ($\overline{\text{POR}}$)
- Brown-out Reset ($\overline{\text{BOR}}$)
- Reset Instruction Reset ($\overline{\text{RI}}$)
- MCLR Reset ($\overline{\text{RMCLR}}$)
- Watchdog Timer Reset ($\overline{\text{RWDT}}$)
- Watchdog Timer Window Violation Reset (WDTWV)
- Stack Underflow Reset (STKUNF)
- Stack Overflow Reset (STKOVF)
- Memory Violation Reset ($\overline{\text{MEMV}}$)

The PCON0 register bits are shown in [Register 8-3](#).
The PCON1 register bits are shown in [Register 8-3](#).

Hardware will change the corresponding register bit during the Reset process; if the Reset was not caused by the condition, the bit remains unchanged ([Table 8-4](#)).

Software should reset the bit to the inactive state after the restart (hardware will not reset the bit).

Software may also set any PCON bit to the active state, so that user code may be tested, but no reset action will be generated.

13.3.6 NVMREG ACCESS TO DEVICE INFORMATION AREA, DEVICE CONFIGURATION AREA, USER ID, DEVICE ID AND CONFIGURATION WORDS

NVMREGS can be used to access the following memory regions:

- Device Information Area (DIA)
- Device Configuration Information (DCI)
- User ID region
- Device ID and Revision ID
- Configuration Words

The value of NVMREGS is set to '1' in the NVMCON1 register to access these regions. The memory regions listed above would be pointed to by PC<15> = 1, but not all addresses reference valid data. Different access may exist for reads and writes. Refer to [Table 13-3](#).

When read access is initiated on an address outside the parameters listed in [Table 13-3](#), the NVMDATH: NVMDATL register pair is cleared, reading back '0's.

TABLE 13-3: NVMREGS ACCESS TO DEVICE INFORMATION AREA, DEVICE CONFIGURATION AREA, USER ID, DEVICE ID AND CONFIGURATION WORDS (NVMREGS = 1)

Address	Function	Read Access	Write Access
8000h-8003h	User IDs	Yes	Yes
8005h-8006h	Device ID/Revision ID	Yes	No
8007h-800Bh	Configuration Words 1-5	Yes	No
8100h-82FFh	DIA and DCI	Yes	No

REGISTER 13-5: NVMCON1: NONVOLATILE MEMORY CONTROL 1 REGISTER

U-0	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W/HC-x/q	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
—	NVMREGS	LWLO	FREE	WRERR ^(1,2,3)	WREN	WR ^(4,5,6)	RD
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7	Unimplemented: Read as '0'
bit 6	NVMREGS: Configuration Select bit 1 = Access DIA, DCI, Configuration, User ID and Device ID Registers 0 = Access PFM
bit 5	LWLO: Load Write Latches Only bit <u>When FREE = 0:</u> 1 = The next WR command updates the write latch for this word within the row; no memory operation is initiated. 0 = The next WR command writes data or erases Otherwise: The bit is ignored
bit 4	FREE: PFM Erase Enable bit <u>When NVMREGS:NVMADR points to a PFM location:</u> 1 = Performs an erase operation with the next WR command; the 32-word pseudo-row containing the indicated address is erased (to all 1s) to prepare for writing. 0 = All erase operations have completed normally
bit 3	WRERR: Program/Erase Error Flag bit ^(1,2,3) This bit is normally set by hardware. 1 = A write operation was interrupted by a Reset, interrupted unlock sequence, or WR was written to one while NVMADR points to a write-protected address. 0 = The program or erase operation completed normally
bit 2	WREN: Program/Erase Enable bit 1 = Allows program/erase cycles 0 = Inhibits programming/erasing of program Flash
bit 1	WR: Write Control bit ^(4,5,6) <u>When NVMREG:NVMADR points to a PFM location:</u> 1 = Initiates the operation indicated by Table 13-4 0 = NVM program/erase operation is complete and inactive.
bit 0	RD: Read Control bit ⁽⁷⁾ 1 = Initiates a read at address = NVMADR1, and loads data to NVMDAT Read takes one instruction cycle and the bit is cleared when the operation is complete. The bit can only be set (not cleared) in software. 0 = NVM read operation is complete and inactive

- Note**
- 1: Bit is undefined while WR = 1.
 - 2: Bit must be cleared by software; hardware will not clear this bit.
 - 3: Bit may be written to '1' by software in order to implement test sequences.
 - 4: This bit can only be set by following the unlock sequence of [Section 13.3.2 "NVM Unlock Sequence"](#).
 - 5: Operations are self-timed, and the WR bit is cleared by hardware when complete.
 - 6: Once a write operation is initiated, setting this bit to zero will have no effect.

TABLE 16-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE PPS MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
PMD0	SYSCMD	FVRMD	—	—	—	NVMMD	CLKRMD	IOCMD	205
PMD1	NCO1MD	—	—	—	—	TMR2MD	TMR1MD	TMR0MD	206
PMD2	—	DAC1MD	ADCMD	—	—	CMP2MD	CMP1MD	ZCDMD	207
PMD3	—	—	PWM6MD	PWM5MD	PWM4MD	PWM3MD	CCP2MD	CCP1MD	208
PMD4	UART2MD	UART1MD	—	MSSP1MD	—	—	—	CWG1MD	209
PMD5	—	—	—	CLC4MD	CLC3MD	CLC2MD	CLC1MD	—	210

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the PPS module.

20.2 ADC Operation

20.2.1 STARTING A CONVERSION

To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'. Setting the GO/DONE bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.

Note: The GO/DONE bit will not be set in the same instruction that turns on the ADC. Refer to [Section 20.2.5 “ADC Conversion Procedure”](#).

20.2.2 COMPLETION OF A CONVERSION

When the conversion is complete, the ADC module will:

- Clear the GO/DONE bit
- Set the ADIF Interrupt Flag bit
- Update the ADRESH and ADRESL registers with new conversion result

Note: A device Reset forces all registers to their Reset state. Thus, the ADC module is turned off and any pending conversion is terminated.

20.2.3 ADC OPERATION DURING SLEEP

The ADC module can operate during Sleep. This requires the ADC clock source to be set to the ADCRC option. When the ADCRC oscillator source is selected, the ADC waits one additional instruction before starting the conversion. This allows the SLEEP instruction to be executed, which can reduce system noise during the conversion. If the ADC interrupt is enabled, the device will wake-up from Sleep when the conversion completes. If the ADC interrupt is disabled, the ADC module is turned off after the conversion completes, although the ADON bit remains set.

When the ADC clock source is something other than ADCRC, a SLEEP instruction causes the present conversion to be aborted and the ADC module is turned off, although the ADON bit remains set.

20.2.4 AUTO-CONVERSION TRIGGER

The Auto-conversion Trigger allows periodic ADC measurements without software intervention. When a rising edge of the selected source occurs, the GO/DONE bit is set by hardware.

The Auto-conversion Trigger source is selected with the ADACT<3:0> bits of the ADACT register.

Using the Auto-conversion Trigger does not assure proper ADC timing. It is the user's responsibility to ensure that the ADC timing requirements are met.

See [Table 20-2](#) for auto-conversion sources.

TABLE 20-2: ADC AUTO-CONVERSION TABLE

ADACT VALUE	SOURCE/ PERIPHERAL	DESCRIPTION
0x00	Disabled	External Trigger Disabled
0x01	ADACTPPS	Pin Selected by ADACTPPS
0x02	TMR0	Timer0 overflow condition
0x03	TMR1	Timer1 overflow condition
0x04	TMR2	Match between Timer2 postscaled value and PR2
0x05	CCP1	CCP1 output
0x06	CCP2	CCP2 output
0x07	PWM3	PWM3 output
0x08	PWM4	PWM4 output
0x09	PWM5	PWM5 output
0x0A	PWM6	PWM6 output
0x0B	NCO1	NCO1 output
0x0C	C1OUT	Comparator C1 output
0x0D	C2OUT	Comparator C2 output
0x0E	IOCIF	Interrupt-on change flag trigger
0x0F	CLC1	CLC1 output
0x10	CLC2	CLC2 output
0x11	CLC3	CLC3 output
0x12	CLC4	CLC4 output
0x13-0xFF	Reserved	Reserved, do not use

REGISTER 20-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<9:2>							
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ADRES<9:2>**: ADC Result Register bits
Upper eight bits of 10-bit conversion result

REGISTER 20-5: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<1:0>		—	—	—	—	—	—
bit 7							bit 0

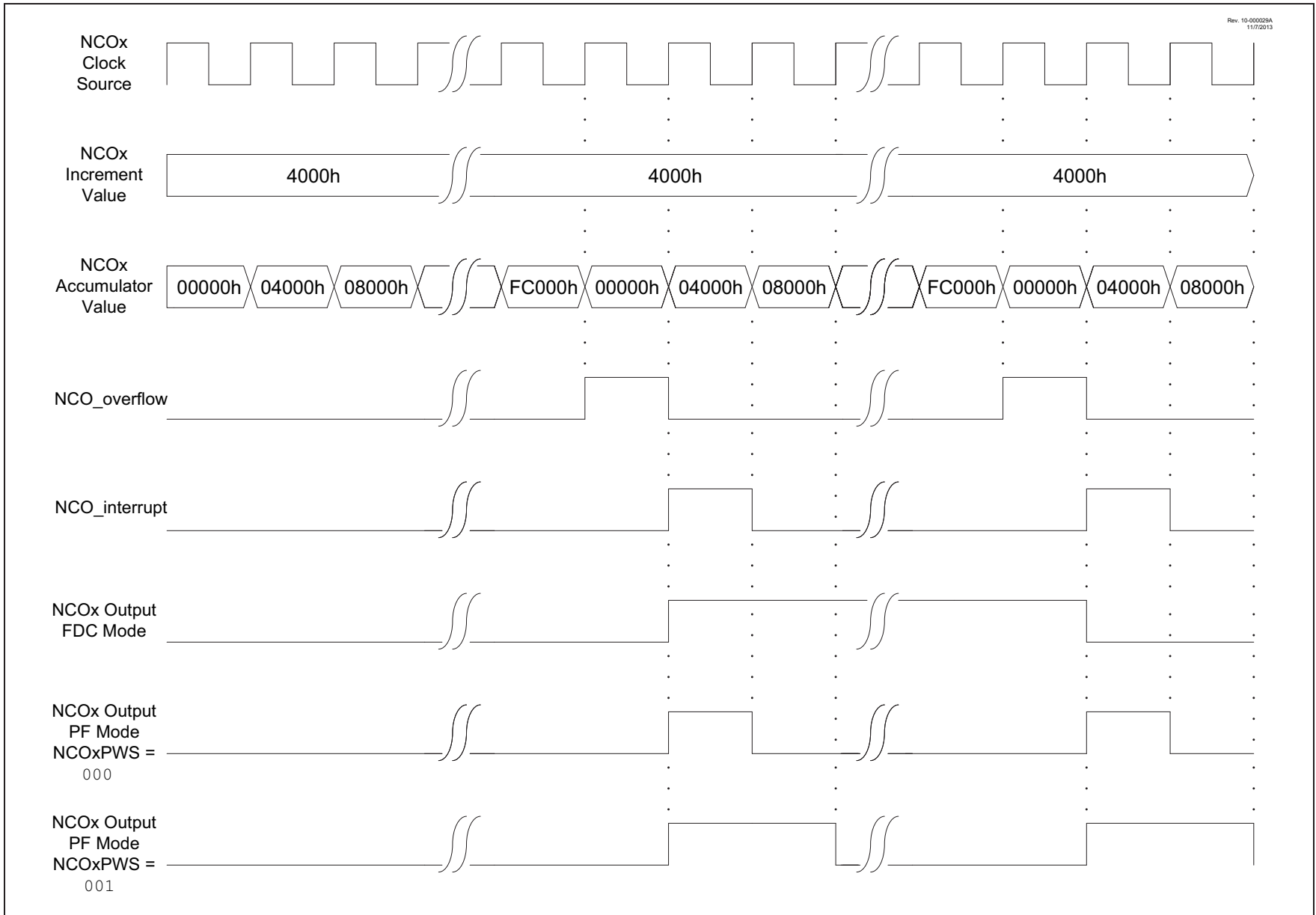
Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **ADRES<1:0>**: ADC Result Register bits
Lower two bits of 10-bit conversion result

bit 5-0 **Reserved**: Do not use.

FIGURE 22-2: FDC OUTPUT MODE OPERATION DIAGRAM



26.10 Register Definitions: Timer1 Control

REGISTER 26-1: T1CON: TIMER1 CONTROL REGISTER

U-0	U-0	R/W-0/u	R/W-0/u	U-0	R/W-0/u	R/W-0/u	R/W-0/u
—	—	CKPS<1:0>		—	SYNC	RD16	ON
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **CKPS<1:0>:** Timer1 Input Clock Prescale Select bits

- 11 = 1:8 Prescale value
- 10 = 1:4 Prescale value
- 01 = 1:2 Prescale value
- 00 = 1:1 Prescale value

bit 3 **Unimplemented:** Read as '0'

bit 2 **SYNC:** Timer1 Synchronization Control bit

When TMR1CLK = Fosc or Fosc/4

This bit is ignored. The timer uses the internal clock and no additional synchronization is performed.

ELSE

- 0 = Synchronize external clock input with system clock
- 1 = Do not synchronize external clock input

bit 1 **RD16:** 16-bit Read/Write Mode Enable bit

- 0 = Enables register read/write of Timer1 in two 8-bit operation
- 1 = Enables register read/write of Timer1 in one 16-bit operation

bit 0 **ON:** Timer1 On bit

- 1 = Enables Timer1
- 0 = Stops Timer1 and clears Timer1 gate flip-flop

27.5.8 LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODES

In Level -Triggered One-Shot mode the timer count is reset on the external signal level and starts counting on the rising/falling edge of the transition from Reset level to the active level while the ON bit is set. Reset levels are selected as follows:

- Low Reset level (MODE<4:0> = 01110)
- High Reset level (MODE<4:0> = 01111)

When the timer count matches the PRx period count, the timer is reset and the ON bit is cleared. When the ON bit is cleared by either a PRx match or by software control a new external signal edge is required after the ON bit is set to start the counter.

When Level-Triggered Reset One-Shot mode is used in conjunction with the CCP PWM operation the PWM drive goes active with the external signal edge that starts the timer. The PWM drive goes inactive when the timer count equals the CCPRx pulse width count. The PWM drive does not go active when the timer count clears at the PRx period count match.

28.1.2 TIMER1 MODE RESOURCE

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

See [Section 26.0 “Timer1 Module with Gate Control”](#) for more information on configuring Timer1.

28.1.3 SOFTWARE INTERRUPT MODE

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit of the PIE6 register clear to avoid false interrupts. Additionally, the user should clear the CCPxIF interrupt flag bit of the PIR6 register following any change in Operating mode.

Note: Clocking Timer1 from the system clock (FOSC) should not be used in Capture mode. In order for Capture mode to recognize the trigger event on the CCPx pin, Timer1 must be clocked from the instruction clock (FOSC/4).

28.1.4 CCP PRESCALER

There are four prescaler settings specified by the CCPxMODE<3:0> bits of the CCPxCON register. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any Reset will clear the prescaler counter.

Switching from one capture prescaler to another does not clear the prescaler and may generate a false interrupt. To avoid this unexpected operation, turn the module off by clearing the CCPxCON register before changing the prescaler. [Example 28-1](#) demonstrates the code to perform this function.

EXAMPLE 28-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
BANKSEL CCPxCON    ;Set Bank bits to point
                   ;to CCPxCON
CLRF    CCPxCON    ;Turn CCP module off
MOVLW  NEW_CAPT_PS;Load the W reg with
                   ;the new prescaler
MOVWF  CCPxCON    ;move value and CCP ON
                   ;Load CCPxCON with this
                   ;value
```

28.1.5 CAPTURE DURING SLEEP

Capture mode depends upon the Timer1 module for proper operation. There are two options for driving the Timer1 module in Capture mode. It can be driven by the instruction clock (FOSC/4), or by an external clock source.

When Timer1 is clocked by FOSC/4, Timer1 will not increment during Sleep. When the device wakes from Sleep, Timer1 will continue from its previous state.

Capture mode will operate during Sleep when Timer1 is clocked by an external clock source.

28.2 Compare Mode

Compare mode makes use of the 16-bit Timer1 resource. The 16-bit value of the CCPRxH:CCPRxL register pair is constantly compared against the 16-bit value of the TMR1H:TMR1L register pair. When a match occurs, one of the following events can occur:

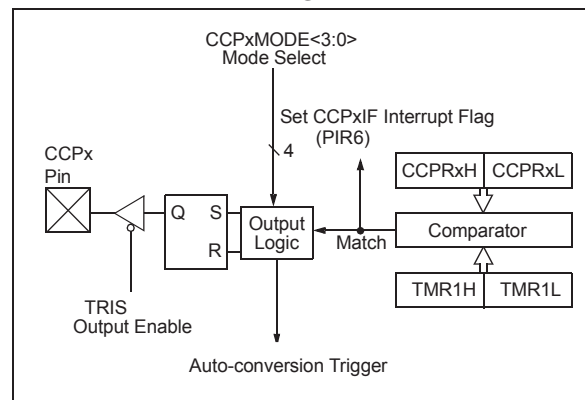
- Toggle the CCPx output
- Set the CCPx output
- Clear the CCPx output
- Generate an Auto-conversion Trigger
- Generate a Software Interrupt

The action on the pin is based on the value of the CCPxMODE<3:0> control bits of the CCPxCON register. At the same time, the interrupt flag CCPxIF bit is set, and an ADC conversion can be triggered, if selected.

All Compare modes can generate an interrupt and trigger and ADC conversion.

[Figure 28-2](#) shows a simplified diagram of the compare operation.

FIGURE 28-2: COMPARE MODE OPERATION BLOCK DIAGRAM



REGISTER 31-10: CLCxGLS3: GATE 3 LOGIC SELECT REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LCxG4D4T	LCxG4D4N	LCxG4D3T	LCxG4D3N	LCxG4D2T	LCxG4D2N	LCxG4D1T	LCxG4D1N
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	LCxG4D4T: Gate 3 Data 4 True (non-inverted) bit 1 = CLCIN3 (true) is gated into CLCx Gate 3 0 = CLCIN3 (true) is not gated into CLCx Gate 3
bit 6	LCxG4D4N: Gate 3 Data 4 Negated (inverted) bit 1 = CLCIN3 (inverted) is gated into CLCx Gate 3 0 = CLCIN3 (inverted) is not gated into CLCx Gate 3
bit 5	LCxG4D3T: Gate 3 Data 3 True (non-inverted) bit 1 = CLCIN2 (true) is gated into CLCx Gate 3 0 = CLCIN2 (true) is not gated into CLCx Gate 3
bit 4	LCxG4D3N: Gate 3 Data 3 Negated (inverted) bit 1 = CLCIN2 (inverted) is gated into CLCx Gate 3 0 = CLCIN2 (inverted) is not gated into CLCx Gate 3
bit 3	LCxG4D2T: Gate 3 Data 2 True (non-inverted) bit 1 = CLCIN1 (true) is gated into CLCx Gate 3 0 = CLCIN1 (true) is not gated into CLCx Gate 3
bit 2	LCxG4D2N: Gate 3 Data 2 Negated (inverted) bit 1 = CLCIN1 (inverted) is gated into CLCx Gate 3 0 = CLCIN1 (inverted) is not gated into CLCx Gate 3
bit 1	LCxG4D1T: Gate 4 Data 1 True (non-inverted) bit 1 = CLCIN0 (true) is gated into CLCx Gate 3 0 = CLCIN0 (true) is not gated into CLCx Gate 3
bit 0	LCxG4D1N: Gate 3 Data 1 Negated (inverted) bit 1 = CLCIN0 (inverted) is gated into CLCx Gate 3 0 = CLCIN0 (inverted) is not gated into CLCx Gate 3

32.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSP1CON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into IDLE mode (Figure 32-30).

32.6.8.1 WCOL Status Flag

If the user writes the SSP1BUF when an Acknowledge sequence is in progress, then WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

32.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSP1CON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSP1STAT register is set. A TBRG later, the PEN bit is cleared and the SSP1IF bit is set (Figure 32-31).

32.6.9.1 WCOL Status Flag

If the user writes the SSP1BUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 32-30: ACKNOWLEDGE SEQUENCE WAVEFORM

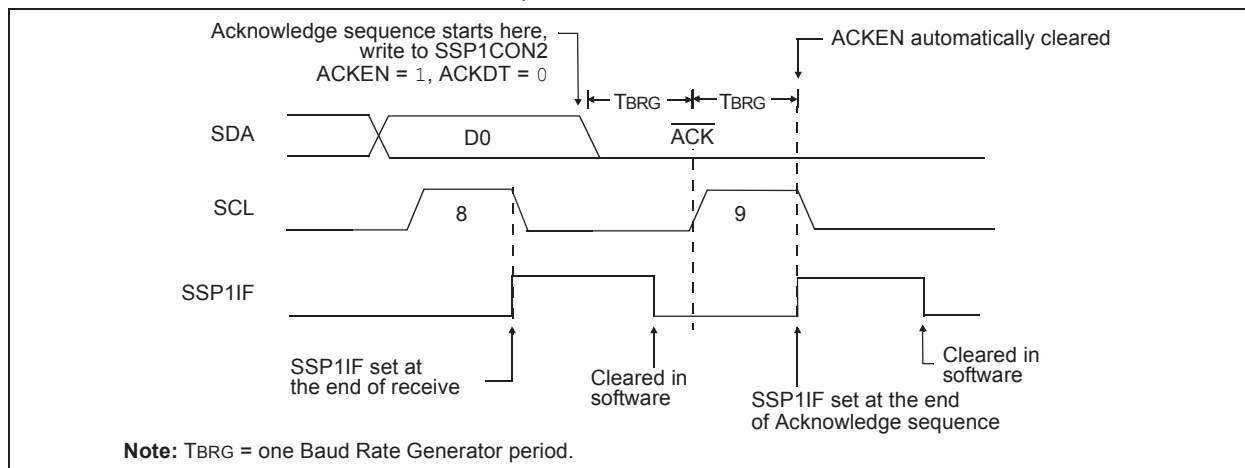
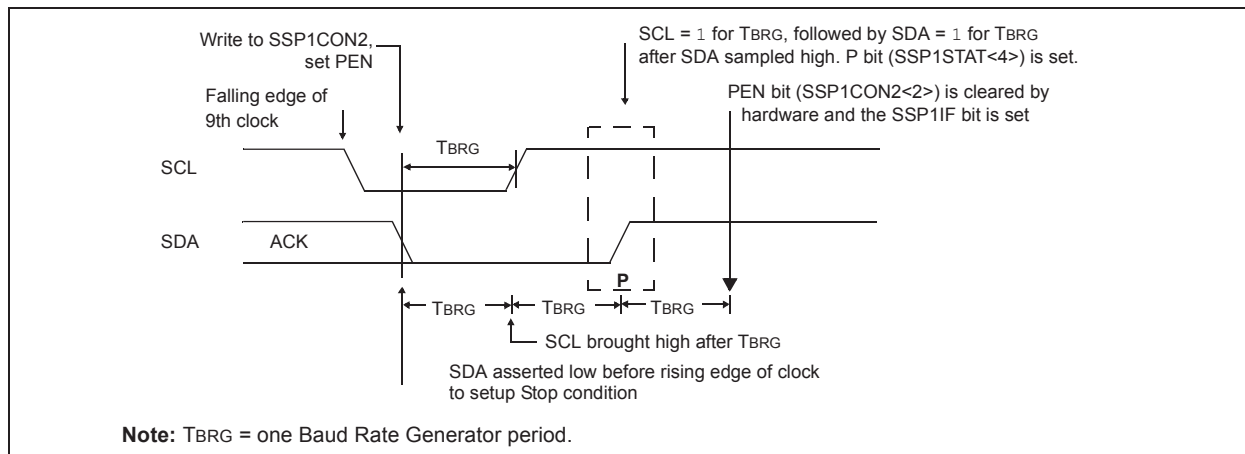


FIGURE 32-31: STOP CONDITION RECEIVE OR TRANSMIT MODE



33.4 EUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The EUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

33.4.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the EUSART for synchronous master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXxSTA register configures the device for synchronous operation. Setting the CSRC bit of the TXxSTA register configures the device as a master. Clearing the SREN and CREN bits of the RCxSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCxSTA register enables the EUSART.

33.4.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the EUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

33.4.1.2 Clock Polarity

A clock polarity option is provided for Microwire compatibility. Clock polarity is selected with the SCKP bit of the BAUDxCON register. Setting the SCKP bit sets the clock Idle state as high. When the SCKP bit is set, the data changes on the falling edge of each clock. Clearing the SCKP bit sets the Idle state as low. When the SCKP bit is cleared, the data changes on the rising edge of each clock.

33.4.1.3 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the EUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXxREG register. If the TSR still contains all or part of a previous character the new character data is held in the TXxREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXxREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXxREG.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

Note: The TSR register is not mapped in data memory, so it is not available to the user.

33.4.1.4 Synchronous Master Transmission Set-up:

1. Initialize the SPxBRGH, SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see [Section 33.3 “EUSART Baud Rate Generator \(BRG\)”](#)).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
3. Disable Receive mode by clearing bits SREN and CREN.
4. Enable Transmit mode by setting the TXEN bit.
5. If 9-bit transmission is desired, set the TX9 bit.
6. If interrupts are desired, set the TXXIE bit of the PIE3 register and the GIE and PEIE bits of the INTCON register.
7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
8. Start transmission by loading data to the TXxREG register.

37.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \leq V_{DD} \leq V_{DDMAX}$

Operating Temperature: $T_{A_MIN} \leq T_A \leq T_{A_MAX}$

V_{DD} — Operating Supply Voltage⁽¹⁾

PIC16LF15324/44

V _{DDMIN} (Fosc ≤ 16 MHz)	+1.8V
V _{DDMIN} (Fosc ≤ 32 MHz)	+2.5V
V _{DDMAX}	+3.6V

PIC16F15324/44

V _{DDMIN} (Fosc ≤ 16 MHz)	+2.3V
V _{DDMIN} (Fosc ≤ 32 MHz)	+2.5V
V _{DDMAX}	+5.5V

T_A — Operating Ambient Temperature Range

Industrial Temperature

T _{A_MIN}	-40°C
T _{A_MAX}	+85°C

Extended Temperature

T _{A_MIN}	-40°C
T _{A_MAX}	+125°C

Note 1: See Parameter [Supply Voltage](#), DS Characteristics: Supply Voltage.