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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	74
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv40f256vll15

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human-body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-up Test*.

1.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	Digital pin input voltage (except open drain pins)	–0.3	VDD + 0.3[1]	V
	Open drain pins (PTC6 and PTC7)	–0.3	5.5	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Maximum value of V_{IO} (except open drain pins) must be 3.8 V.

1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 1 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 1. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Symbol	Description	Notes[1]	Min	Max	Unit
V_{DD}	Supply Voltage Range		-0.3	4.0	V
V_{DDA}	Analog Supply Voltage Range		-0.3	4.0	V
V_{REFHx}	ADC High Voltage Reference		-0.3	4.0	V
V_{REFLx}	ADC Low Voltage Reference		-0.3	0.3	V
ΔV_{DD}	Voltage difference V_{DD} to V_{DDA}		-0.3	0.3	V
ΔV_{SS}	Voltage difference V_{SS} to V_{SSA}		-0.3	0.3	V
V_{IN}	Digital Input Voltage Range	Pin Groups 1, 2	-0.3	4.0	V
V_{OSC}	Oscillator Input Voltage Range	Pin Group 4	- 0.4	4.0	V
V_{INA}	Analog Input Voltage Range	Pin Group 3	-0.3	4.0	V
I_{IC}	Input clamp current, per pin (V_{IN} < 0)		—	-20.0	mA
I_{OC}	Output clamp current, per pin (V_O < 0)[2]		—	-20.0	mA
V_{OUT}	Output Voltage Range (Normal Push-Pull mode)	Pin Group 1	- 0.3	4.0	V
V_{OUTOD}	Output Voltage Range (Open Drain mode)	Pin Group 2	- 0.3	5.5	V
V_{OUT_DAC}	DAC Output Voltage Range	Pin Group 5	- 0.3	4.0	V
T_A	Ambient Temperature Industrial		- 40	105	°C
T_{STG}	Storage Temperature Range (Extended Industrial)		- 55	150	°C

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$, PORTC6, and PORTC7
   - Pin Group 3: ADC and Comparator Analog Inputs

2.4.2 Thermal attributes

Table 13. Thermal attributes

Board type	Symbol	Description	100 LQFP	64 LQFP	48 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	62	64	81	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	49	46	57	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	52	68	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	43	39	51	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	28	35	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	17	15	25	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	2	7	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD Electricals

Table 14. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation			

Table continues on the next page...

3.1.2 Debug trace timing specifications

Table 15. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	1.5	ns
T_h	Data hold	2	1.0	ns

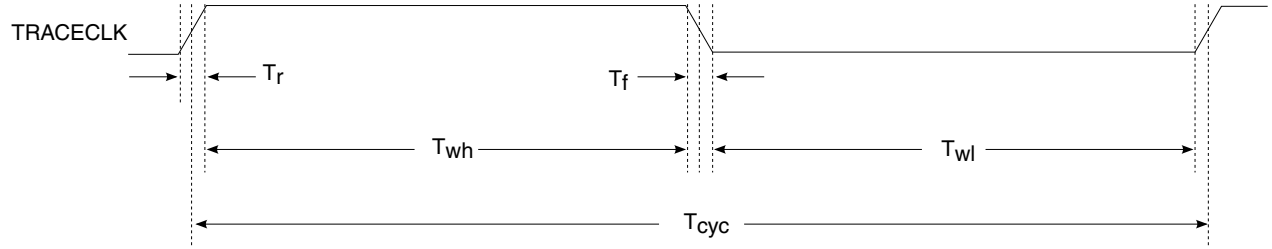

Figure 7. TRACE_CLKOUT specifications

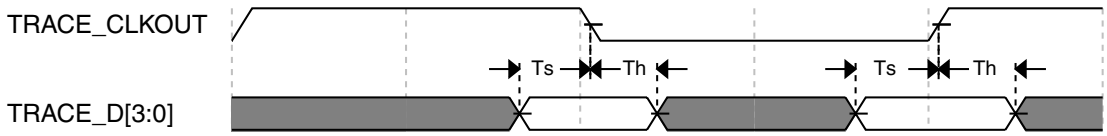

Figure 8. Trace data specifications

3.1.3 JTAG electricals

Table 16. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
		0	25	

Table continues on the next page...

Table 17. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	19.0	ns
J12	TCLK low to TDO high-Z	—	17.0	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

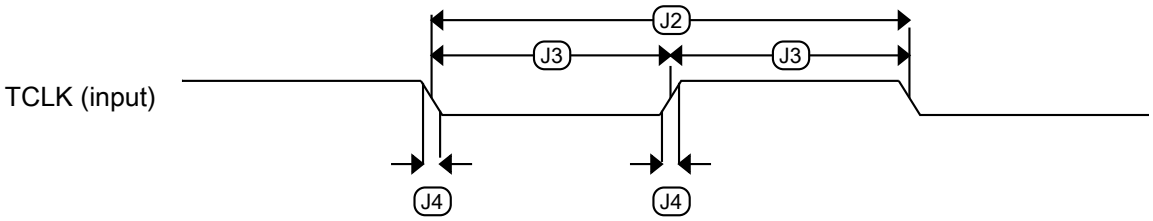

Figure 9. Test clock input timing

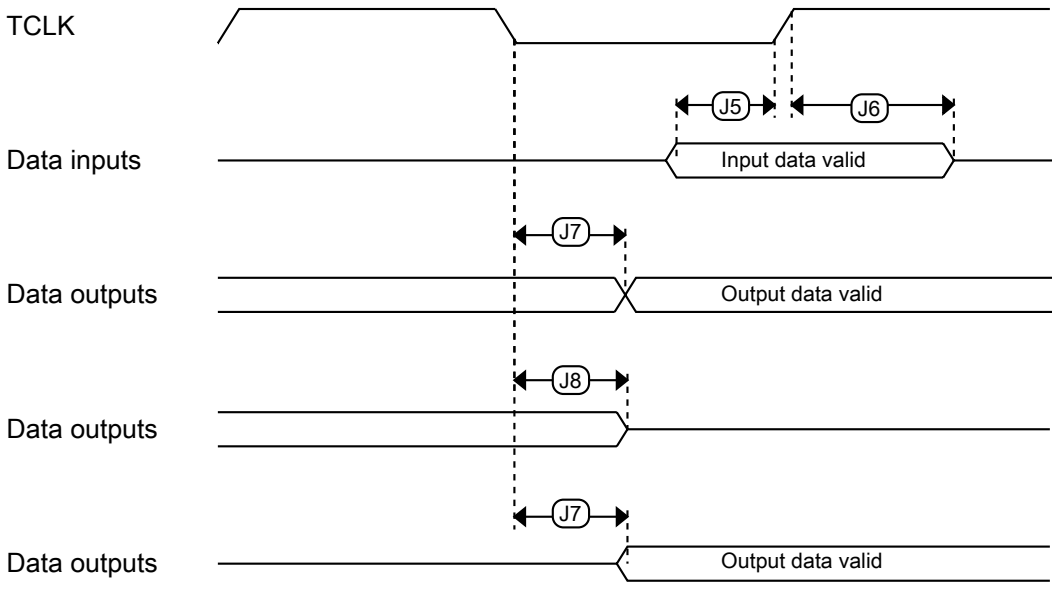

Figure 10. Boundary scan (JTAG) timing

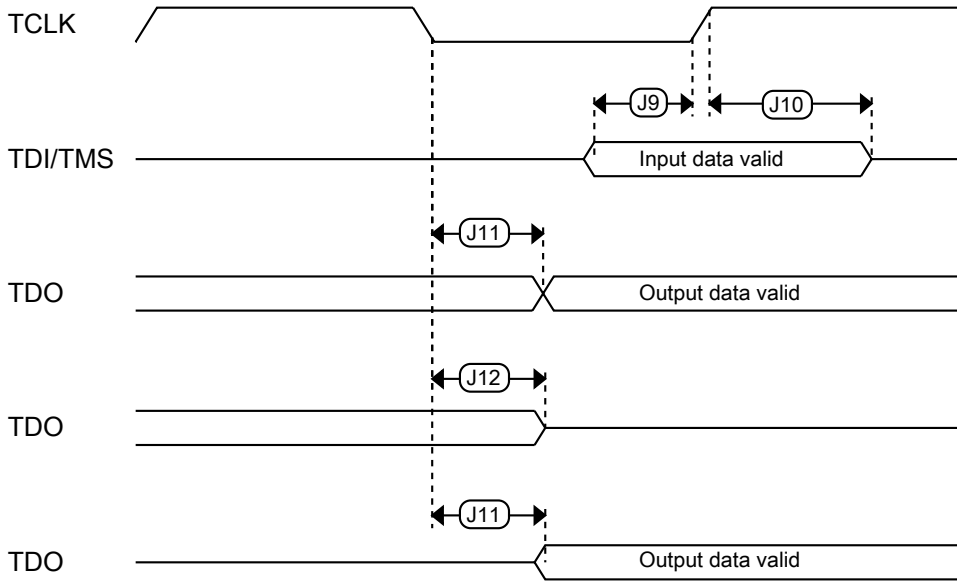

Figure 11. Test Access Port timing

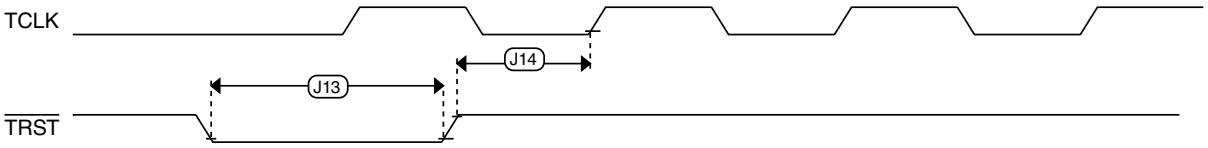

Figure 12. TRST timing

3.2 System modules

There are no specifications necessary for the device's system modules.

3.3 Clock modules

3.3.1 MCG specifications

Table 18. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	± 0.5	± 2	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—		± 1	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11)	—	95.98	—	MHz	

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	2929 × f_{fll_ref}					
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz	— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6
	PLL					
f_{pll_ref}	PLL reference frequency range	8	—	16	MHz	
f_{vcoclk_2x}	VCO output frequency	180	—	360	MHz	
f_{vcoclk}	PLL output frequency	90	—	180	MHz	
f_{vcoclk_90}	PLL quadrature output frequency	90	—	180	MHz	
I_{pll}	PLL operating current • VCO @ 176 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 22)	—	2.8	—	mA	7
I_{pll}	PLL operating current • VCO @ 360 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)	—	4.7	—	mA	7
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz	 — —	 120 75	 — —	 ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz	 — —	 1350 600	 — —	 ps ps	8
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	150 × 10^{-6} + 1075(1/f_{pll_ref})	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 20. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	3, 4

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec4k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	—
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	500	3000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

Table 25. 12-bit ADC electrical specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage Range External Reference Internal Reference	V_{ADIN}	V_{REFL} V_{SSA}		V_{REFH} V_{DDA}	V
Timing and Power					
Conversion Time	t_{ADC}		6		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		13		ADC Clock Cycles
ADC RUN Current (per ADC block) • at 600 kHz ADC Clock, LP mode • ≤ 8.33 MHz ADC Clock, 00 mode • ≤ 12.5 MHz ADC Clock, 01 mode • ≤ 16.67 MHz ADC Clock, 10 mode • ≤ 20 MHz ADC Clock, 11 mode • ≤ 25 MHz ADC Clock	I_{ADRUN}		 1 5.7 10.5 17.7 22.6 TBD		mA
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.02		µA
V_{REFH} Current	I_{VREFH}		0.001		µA
Accuracy (DC or Absolute)					
Integral non-Linearity	I_{NL}		+/- 3	+/- 5	LSB
Differential non-Linearity[1]	DNL		+/- 0.6	+/- 0.9	LSB[2]
Monotonicity					
Offset • 1x gain mode • 2x gain mode • 4x gain mode	V_{OFFSET}			 +/- 17 +/- 20 +/- 25	mV
Gain Error	E_{GAIN}		0.801 to 0.809	0.798 to 0.814	
AC Specifications					
Signal to Noise Ratio	SNR		59		dB
Total Harmonic Distortion	THD		64		dB
Spurious Free Dynamic Range	SFDR		65		dB
Signal to Noise plus Distortion	SINAD		59		dB
Effective Number of Bits	ENOB		9.5		bits
ADC Inputs					
Input Leakage Current	I_{IN}		0	+/-2	µA
Input Injection Current	I_{INJ}			+/-3	mA
Input Capacitance Sampling Capacitor	C_{ADI}		4.8		pF

1. I_{NL} measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$.
2. LSB = Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 Gain Setting

3.6.2 CMP and 6-bit DAC electrical specifications

Table 26. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	$V_{DD} – 0.5$	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to $V_{DD} – 0.7$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

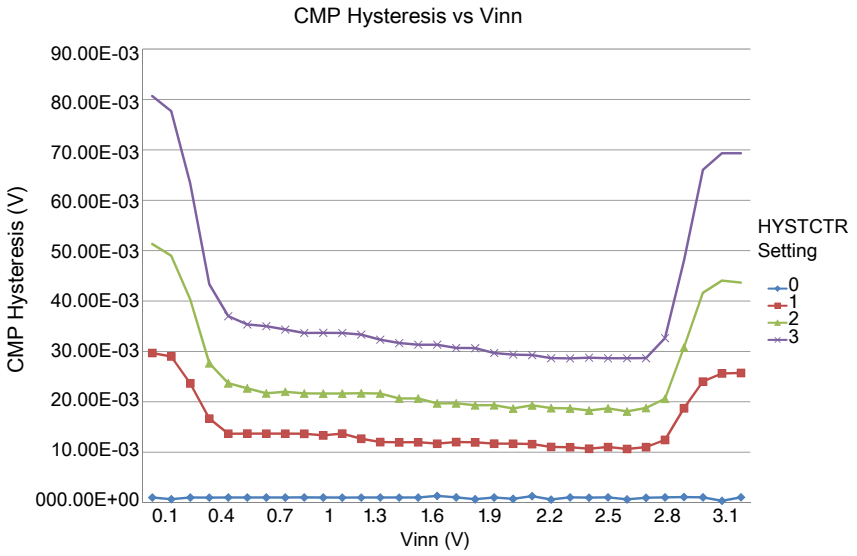

Figure 14. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

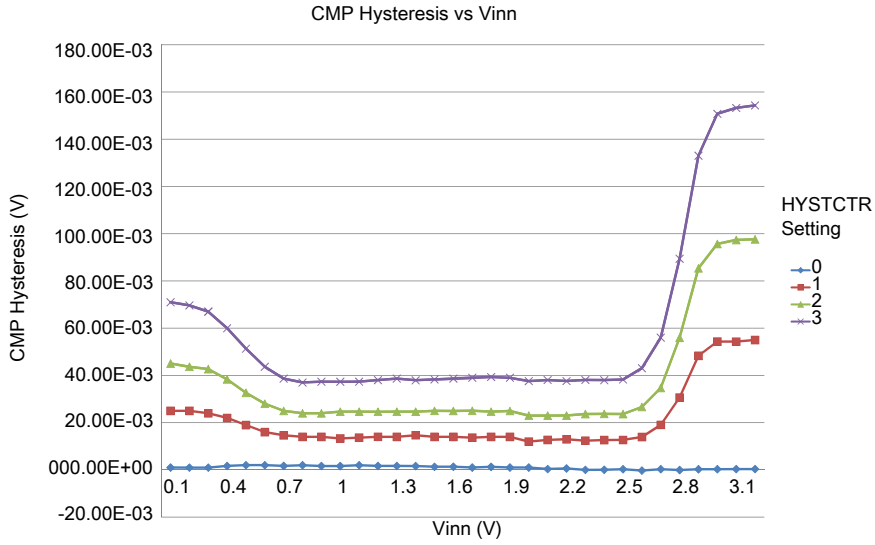

Figure 15. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

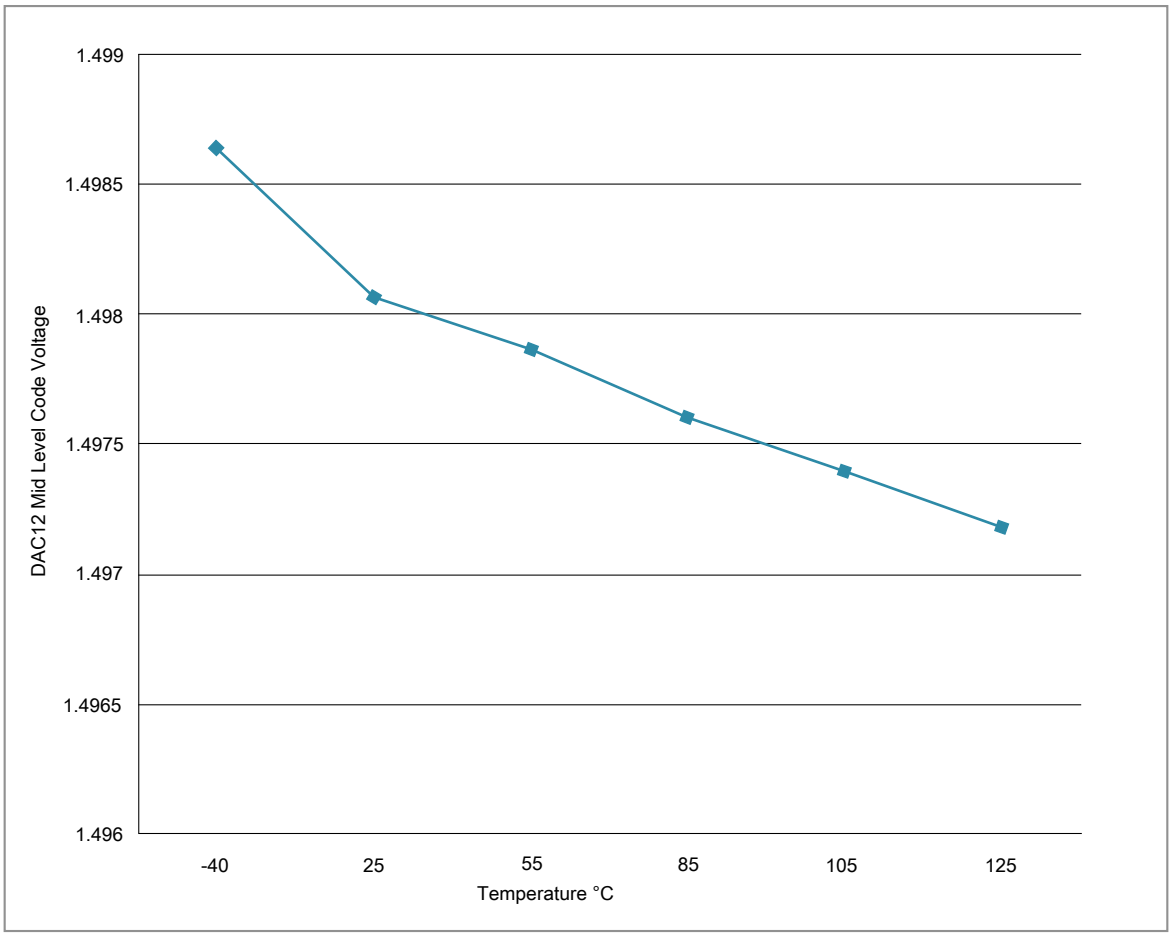

Figure 17. Offset at half scale vs. temperature

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

Table 34. Slave mode DSPI timing for open drain pads (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	28	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	22	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	22	ns

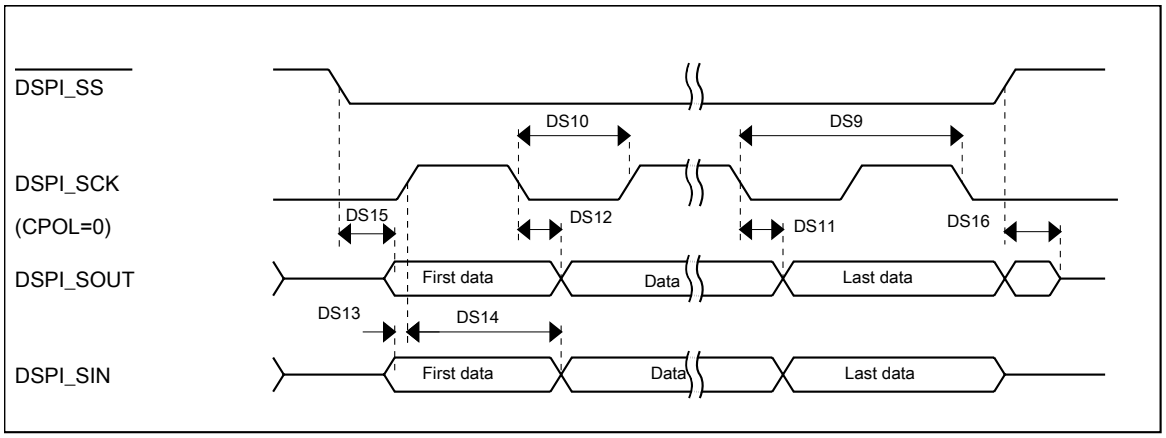

Figure 19. DSPI classic SPI timing — slave mode

3.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

NOTE

Fast pads:

- SIN: PTE19
- SOUT: PTE18

Table 38. Slave mode DSPI timing for normal pads (full voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	22	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	22	ns

Table 39. Slave mode DSPI timing for fast pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	18.75	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	15	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	15	ns

Table 40. Slave mode DSPI timing for open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	9.375	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	43.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	38	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	38	ns

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
77	50	38	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	XBAR0_IN2		CMP0_OUT	FTM0_CH2
77	110	D8	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	XBAR0_IN2		CMP0_OUT	FTM0_CH2
78	51	39	PTC6/ LLWU_P10	CMP2_IN4/ CMP0_IN0	CMP2_IN4/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_ EXTRG	XBAR0_IN3	UART0_RX	XBAR0_ OUT6	I2C0_SCL
78	111	C8	PTC6/ LLWU_P10	CMP2_IN4/ CMP0_IN0	CMP2_IN4/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_ EXTRG	XBAR0_IN3	UART0_RX	XBAR0_ OUT6	I2C0_SCL
79	52	40	PTC7	CMP3_IN4/ CMP0_IN1	CMP3_IN4/ CMP0_IN1	PTC7	SPI0_SIN		XBAR0_IN4	UART0_TX	XBAR0_ OUT7	I2C0_SDA
79	112	B8	PTC7	CMP3_IN4/ CMP0_IN1	CMP3_IN4/ CMP0_IN1	PTC7	SPI0_SIN		XBAR0_IN4	UART0_TX	XBAR0_ OUT7	I2C0_SDA
80	53	—	PTC8	ADCB_CH7c/ CMP0_IN2	ADCB_CH7c/ CMP0_IN2	PTC8		FTM3_CH4				
80	113	A8	PTC8	ADCD_CH7c/ CMP0_IN2	ADCD_CH7c/ CMP0_IN2	PTC8		FTM3_CH4	FLEXPWMB_ A2			
81	54	—	PTC9	ADCB_CH6d/ CMP0_IN3	ADCB_CH6d/ CMP0_IN3	PTC9		FTM3_CH5				
81	114	D7	PTC9	ADCD_CH6d/ CMP0_IN3	ADCD_CH6d/ CMP0_IN3	PTC9		FTM3_CH5	FLEXPWMB_ B2			
82	55	—	PTC10	ADCB_CH7d	ADCB_CH7d	PTC10		FTM3_CH6				
82	115	C7	PTC10	ADCD_CH7d	ADCD_CH7d	PTC10	I2C1_SCL	FTM3_CH6	FLEXPWMB_ A3			
83	56	—	PTC11/ LLWU_P11	ADCB_CH6e	ADCB_CH6e	PTC11/ LLWU_P11		FTM3_CH7				
83	116	B7	PTC11/ LLWU_P11	ADCD_CH6e	ADCD_CH6e	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7	FLEXPWMB_ B3			
84	—	—	PTC12	DISABLED		PTC12			FTM_CLKIN0		FTM3_FLT0	
84	117	A7	PTC12	DISABLED		PTC12	CAN2_TX		FTM_CLKIN0	FLEXPWMB_ A1	FTM3_FLT0	SPI2_PCS1
85	—	—	PTC13	DISABLED		PTC13			FTM_CLKIN1			
85	118	D6	PTC13	DISABLED		PTC13	CAN2_RX		FTM_CLKIN1	FLEXPWMB_ B1		
86	—	—	PTC14	DISABLED		PTC14		I2C0_SCL				
86	119	C6	PTC14	DISABLED		PTC14	I2C1_SCL	I2C0_SCL		FLEXPWMB_ A0		
87	—	—	PTC15	DISABLED		PTC15		I2C0_SDA				
87	120	B6	PTC15	DISABLED		PTC15	I2C1_SDA	I2C0_SDA		FLEXPWMB_ B0		
88	—	—	VSS	VSS	VSS							
88	121	—	VSS	VSS	VSS							
89	—	—	VDD	VDD	VDD							
89	122	—	VDD	VDD	VDD							
90	—	—	PTC16	DISABLED		PTC16	CAN1_RX					

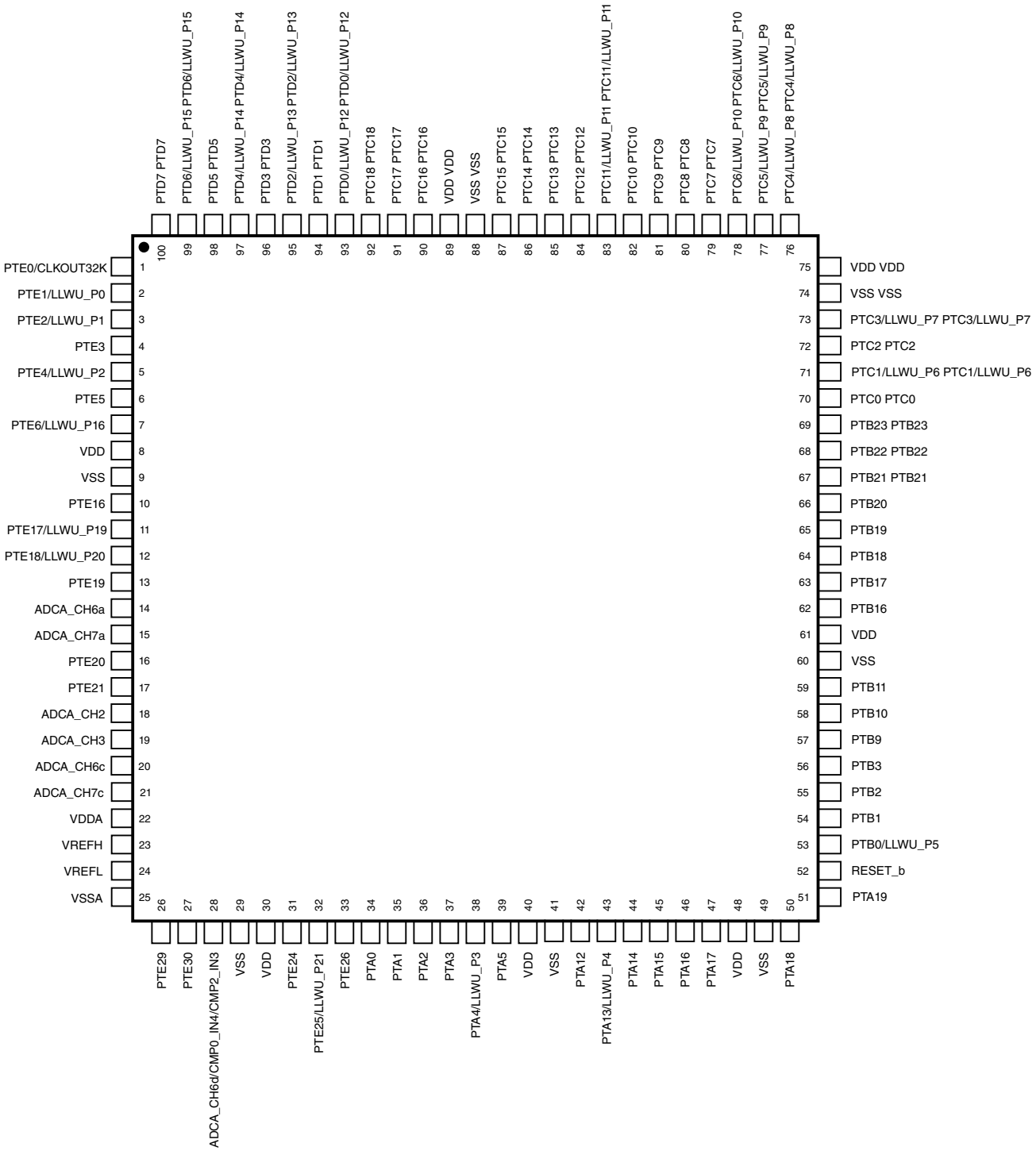

Figure 22. 100-pin LQFP

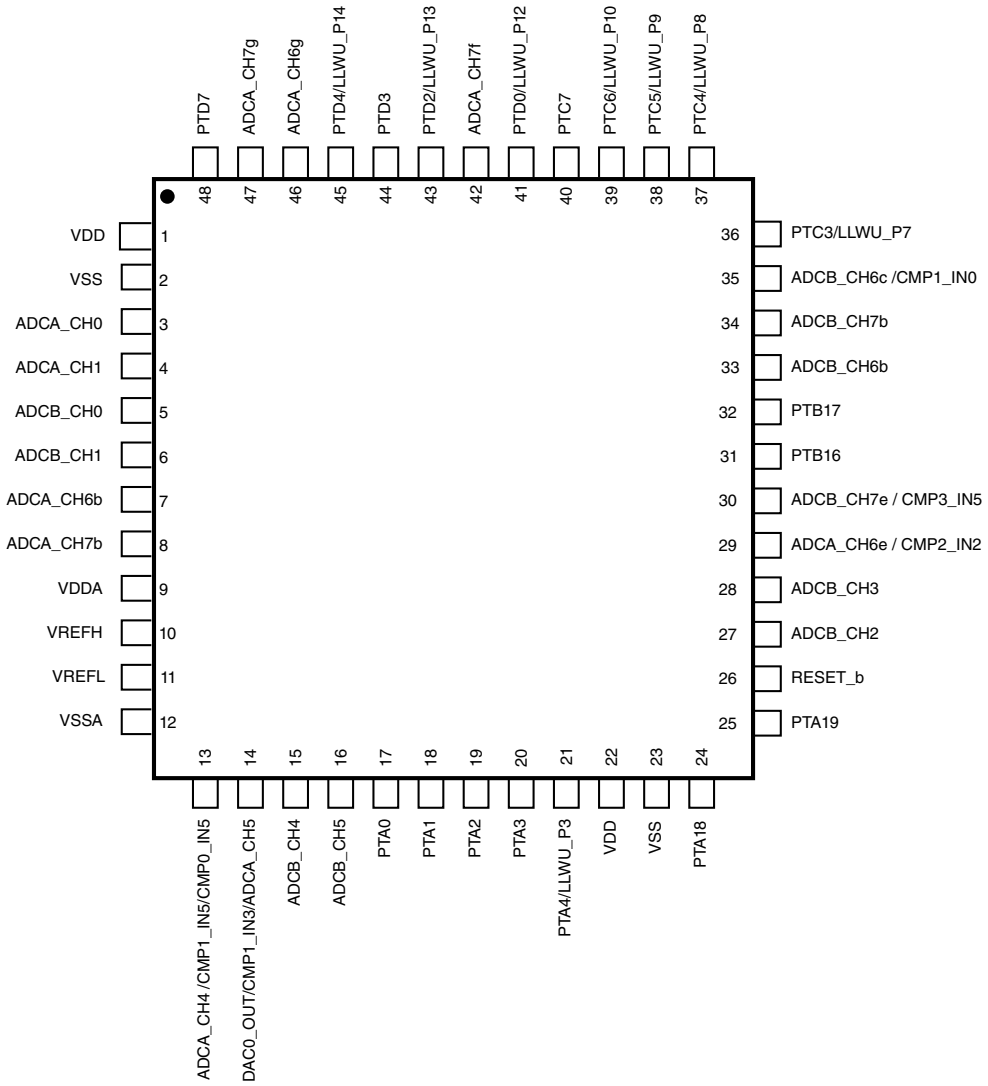

Figure 24. 48-pin LQFP

6 Ordering parts

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