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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	74
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv45f256vll15

Table of Contents

- Pin Group 4: XTAL, EXTAL
- Pin Group 5: DAC analog output

2. Continuous clamp current per pin is -2.0 mA

2 General

Electromagnetic compatibility (EMC) performance depends on the environment in which the MCU resides. Board design and layout, circuit topology choices, location, characteristics of external components, and MCU software operation play a significant role in EMC performance.

See the following applications notes available on freescale.com for guidelines on optimizing EMC performance.

- *AN2321: Designing for Board Level Electromagnetic Compatibility*
- *AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers*
- *AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers*
- *AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications*
- *AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems*

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

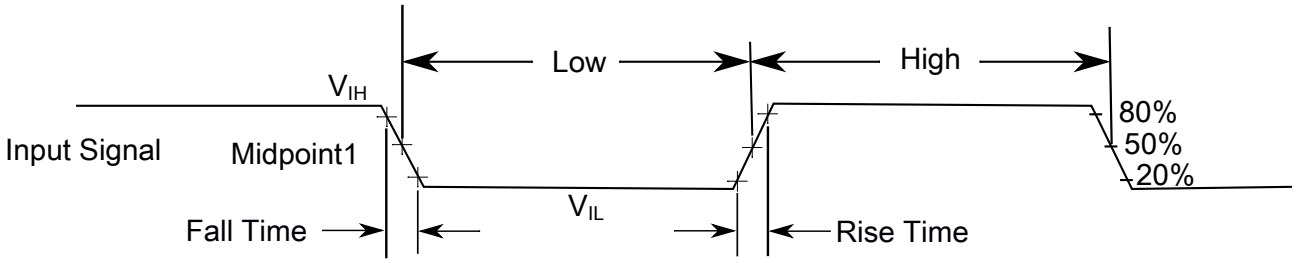


Figure 2. Input signal measurement reference

Table 2. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V) (continued)

Symbol	Description	Notes[1]	Min	Typ	Max	Unit
N_F	Flash Endurance (Program Erase Cycles)	T_A = -40°C to 105°C	10K		—	cycles
T_R	Flash Data Retention	T_J ≤ 85°C avg	15		—	years
t_{FLRET}	Flash Data Retention with < 100 Program/ Erase Cycles	T_J ≤ 85°C avg	25	—	—	years

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
   - Pin Group 6: PTB0, PTB1, PTD4, PTD5, PTD6, PTD7, PTC3, and PTC4. have high output current capability
   - Pin Group 7: PTC6 and PTC7 are true open drain pins and have no P-chanl transistor. A external pull-up resistor is required when these pins are outputs.
2. Total chip source or sink current cannot exceed 75 mA.

2.2.2 LVD and POR operating requirements

Table 3. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	

Table continues on the next page...

Table 3. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 PORT Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Notes[1]	Min	Typ	Max	Unit	Test Conditions
V_{OH}[2]	Output Voltage High	Pin Group 1	V_{DD} - 0.5	—	—	V	$I_{OH} = I_{OHmax}$
V_{OL}	Output Voltage Low	Pin Groups 1, 2	—	—	0.5	V	$I_{OL} = I_{OLmax}$
I_{IH}	Digital Input Current High pull-up enabled or disabled	Pin Groups 1, 2	—	0	+/- 2.5	µA	V_{IN} = 2.4V to 5.5V
I_{IHC}	Comparator Input Current High	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
I_{IHOSC}	Oscillator Input Current High	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
I_{IL}	Digital Input Current Low • pull-up enabled • pull-up disabled	Pin Groups 1, 2	TBD TBD	TBD TBD	TBD TBD	µA	V_{IN} = 0V
$R_{Pull-Up}$	Internal Pull-Up Resistance		20	—	50	kΩ	—
I_{ILC}	Comparator Input Current Low	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
I_{ILOSC}	Oscillator Input Current Low	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
V_{DAC}	DAC Output Voltage Range	Pin Group 5	Typically V_{SSA} + 40mV	—	Typically V_{DDA} - 40mV	V	R_{LD} = 3 kΩ || C_{LD} = 400 pf
I_{OZ}	Output Current[1] High Impedance State	Pin Groups 1, 2	—	0	+/- 2.5	µA	—
V_{HYS}	Schmitt Trigger Input Hysteresis	Pin Groups 1, 2	—	0.06 x V_{DD}	—	V	—
C_{IN}	Input Capacitance		—	10	—	pF	—
C_{OUT}	Output Capacitance		—	10	—	pF	—

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Table 7. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							nA
	VLLS1							
	VLLS3	440	490	540	560	570	580	
	LLS	440	490	540	560	570	580	
	VLPS	490	490	540	560	570	680	
	STOP	510	560	560	560	610	680	
		510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled

3.3.1 MCG specifications

Table 18. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	± 0.5	± 2	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—		± 1	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11)	—	95.98	—	MHz	

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	2929 × f_{fll_ref}					
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz	— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6
	PLL					
f_{pll_ref}	PLL reference frequency range	8	—	16	MHz	
f_{vcoclk_2x}	VCO output frequency	180	—	360	MHz	
f_{vcoclk}	PLL output frequency	90	—	180	MHz	
f_{vcoclk_90}	PLL quadrature output frequency	90	—	180	MHz	
I_{pll}	PLL operating current • VCO @ 176 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 22)	—	2.8	—	mA	7
I_{pll}	PLL operating current • VCO @ 360 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)	—	4.7	—	mA	7
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz	 — —	 120 75	 — —	 ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz	 — —	 1350 600	 — —	 ps ps	8
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	150 × 10^{-6} + 1075(1/f_{pll_ref})	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec4k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	—
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	0.9	ms	—
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	—
t_{ersall}	Erase All Blocks execution time	—	500	3000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

Table 25. 12-bit ADC electrical specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage Range External Reference Internal Reference	V_{ADIN}	V_{REFL} V_{SSA}		V_{REFH} V_{DDA}	V
Timing and Power					
Conversion Time	t_{ADC}		6		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		13		ADC Clock Cycles
ADC RUN Current (per ADC block) • at 600 kHz ADC Clock, LP mode • ≤ 8.33 MHz ADC Clock, 00 mode • ≤ 12.5 MHz ADC Clock, 01 mode • ≤ 16.67 MHz ADC Clock, 10 mode • ≤ 20 MHz ADC Clock, 11 mode • ≤ 25 MHz ADC Clock	I_{ADRUN}		 1 5.7 10.5 17.7 22.6 TBD		mA
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.02		µA
V_{REFH} Current	I_{VREFH}		0.001		µA
Accuracy (DC or Absolute)					
Integral non-Linearity	I_{NL}		+/- 3	+/- 5	LSB
Differential non-Linearity[1]	DNL		+/- 0.6	+/- 0.9	LSB[2]
Monotonicity					
Offset • 1x gain mode • 2x gain mode • 4x gain mode	V_{OFFSET}			 +/- 17 +/- 20 +/- 25	mV
Gain Error	E_{GAIN}		0.801 to 0.809	0.798 to 0.814	
AC Specifications					
Signal to Noise Ratio	SNR		59		dB
Total Harmonic Distortion	THD		64		dB
Spurious Free Dynamic Range	SFDR		65		dB
Signal to Noise plus Distortion	SINAD		59		dB
Effective Number of Bits	ENOB		9.5		bits
ADC Inputs					
Input Leakage Current	I_{IN}		0	+/-2	µA
Input Injection Current	I_{INJ}			+/-3	mA
Input Capacitance Sampling Capacitor	C_{ADI}		4.8		pF

1. I_{NL} measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$.
2. LSB = Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 Gain Setting

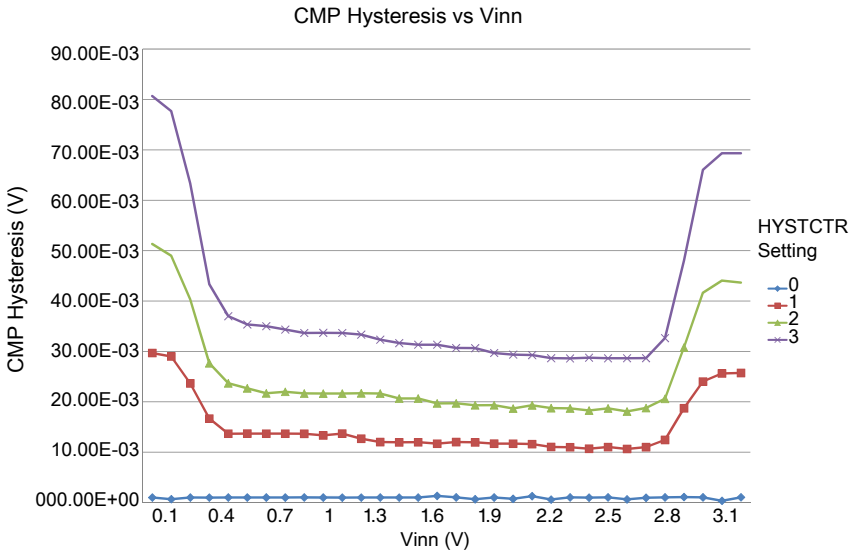


Figure 14. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

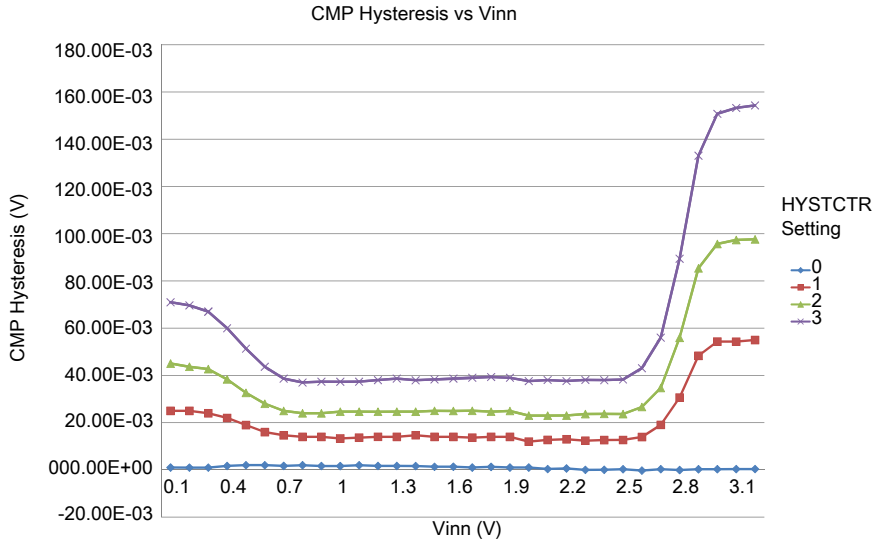


Figure 15. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

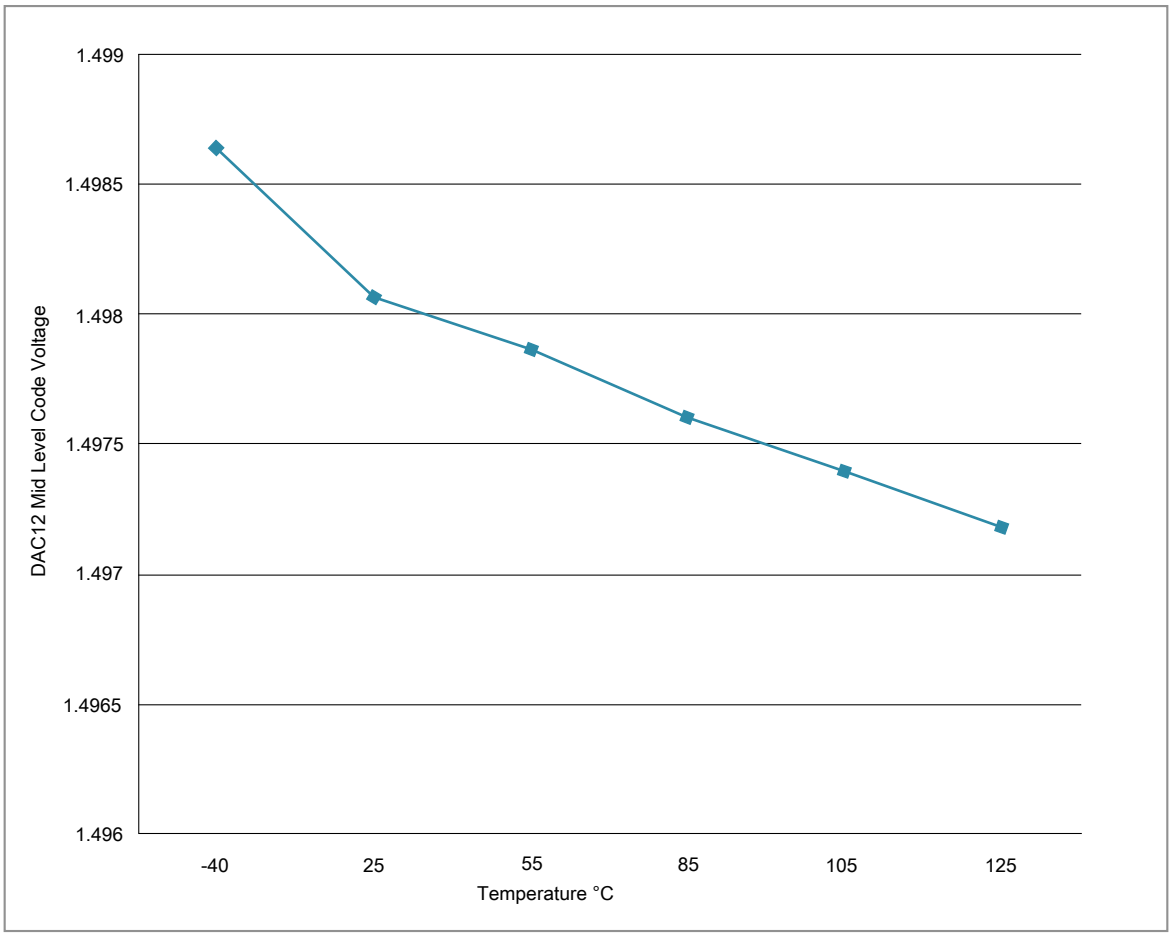


Figure 17. Offset at half scale vs. temperature

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 37. Master mode DSPI timing open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	18.75	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	26	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-7.8	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

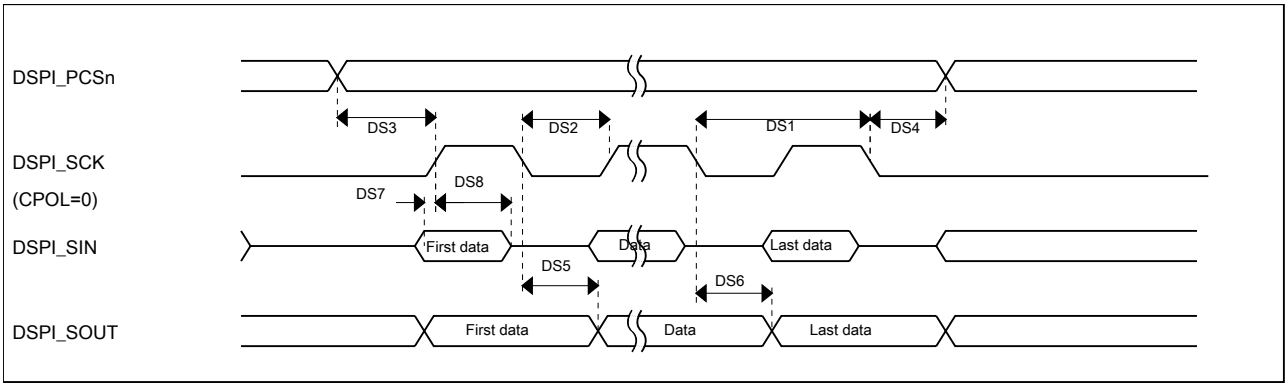


Figure 20. DSPI classic SPI timing — master mode

Table 38. Slave mode DSPI timing for normal pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	12.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	27.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns

Table continues on the next page...

Table 38. Slave mode DSPI timing for normal pads (full voltage range) (continued)

Num	Description	Min.	Max.	Unit
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	22	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	22	ns

Table 39. Slave mode DSPI timing for fast pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	18.75	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	15	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	15	ns

Table 40. Slave mode DSPI timing for open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	9.375	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	43.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	38	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	38	ns

5 Pinout

5.1 KV4x Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

The 48-pin LQFP package for this product is not yet available. However, it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	126	B5	PTC19	DISABLED		PTC19		UART3_CTS_b	ENET0_1588_TMR3	FLEXPWMB_B3		
—	134	M10	VSS	DISABLED	VSS							
—	135	F8	VDD	DISABLED	VDD							
—	137	C9	PTD8/LLWU_P24	DISABLED		PTD8/LLWU_P24	I2C1_SCL	UART5_RX			FLEXPWMA_A3	
—	138	B9	PTD9	DISABLED		PTD9	I2C1_SDA	UART5_TX			FLEXPWMA_B3	
—	139	B3	PTD10	DISABLED		PTD10		UART5_RTS_b			FLEXPWMA_A2	
—	140	B2	PTD11/LLWU_P25	DISABLED		PTD11/LLWU_P25	SPI2_PCS0	UART5_CTS_b			FLEXPWMA_B2	
—	141	B1	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	XBAR0_IN5	XBAR0_OUT5	FLEXPWMA_A1	
—	142	C3	PTD13	DISABLED		PTD13	SPI2_SOUT		XBAR0_IN7	XBAR0_OUT7	FLEXPWMA_B1	
—	143	C2	PTD14	DISABLED		PTD14	SPI2_SIN		XBAR0_IN11	XBAR0_OUT11	FLEXPWMA_A0	
—	144	C1	PTD15	DISABLED		PTD15	SPI2_PCS1				FLEXPWMA_B0	
1	1	—	PTE0/CLKOUT32K	ADCB_CH6f	ADCB_CH6f	PTE0/CLKOUT32K		UART1_TX	XBAR0_OUT10	XBAR0_IN11		
2	2	—	PTE1/LLWU_P0	ADCB_CH7f	ADCB_CH7f	PTE1/LLWU_P0		UART1_RX	XBAR0_OUT11	XBAR0_IN7		
3	—	—	PTE2/LLWU_P1	ADCB_CH6g	ADCB_CH6g	PTE2/LLWU_P1		UART1_CTS_b				

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
4	—	—	PTE3	ADCB_CH7g	ADCB_CH7g	PTE3		UART1_RTS_b				
5	—	—	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2						
6	—	—	PTE5	DISABLED		PTE5					FTM3_CH0	
7	—	—	PTE6/ LLWU_P16	DISABLED		PTE6/ LLWU_P16					FTM3_CH1	
8	3	1	VDD	VDD	VDD							
9	4	2	VSS	VSS	VSS							
10	5	3	PTE16	ADCA_CH0	ADCA_CH0	PTE16	SPI0_PCS0	UART1_TX	FTM_CLKIN0		FTM0_FLT3	
11	6	4	PTE17/ LLWU_P19	ADCA_CH1	ADCA_CH1	PTE17/ LLWU_P19	SPI0_SCK	UART1_RX	FTM_CLKIN1		LPTMR0_ ALT3	
12	7	5	PTE18/ LLWU_P20	ADCB_CH0	ADCB_CH0	PTE18/ LLWU_P20	SPI0_SOUT	UART1_CTS_b	I2C0_SDA			
13	8	6	PTE19	ADCB_CH1	ADCB_CH1	PTE19	SPI0_SIN	UART1_RTS_b	I2C0_SCL		CMP3_OUT	
14	—	—	ADCA_CH6a	ADCA_CH6a	ADCA_CH6a							
15	—	—	ADCA_CH7a	ADCA_CH7a	ADCA_CH7a							
16	—	7	PTE20	ADCA_CH6b	ADCA_CH6b	PTE20		FTM1_CH0	UART0_TX			
17	—	8	PTE21	ADCA_CH7b	ADCA_CH7b	PTE21		FTM1_CH1	UART0_RX			
18	9	—	ADCA_CH2	ADCA_CH2	ADCA_CH2							
19	10	—	ADCA_CH3	ADCA_CH3	ADCA_CH3							
20	11	—	ADCA_CH6c	ADCA_CH6c	ADCA_CH6c							
21	12	—	ADCA_CH7c	ADCA_CH7c	ADCA_CH7c							
22	13	9	VDDA	VDDA	VDDA							
23	14	10	VREFH	VREFH	VREFH							
24	15	11	VREFL	VREFL	VREFL							
25	16	12	VSSA	VSSA	VSSA							
26	17	13	PTE29	ADCA_CH4/ CMP1_IN5/ CMP0_IN5	ADCA_CH4/ CMP1_IN5/ CMP0_IN5	PTE29		FTM0_CH2		FTM_CLKIN0		
27	18	14	PTE30	DAC0_OUT/ CMP1_IN3/ ADCA_CH5	DAC0_OUT/ CMP1_IN3/ ADCA_CH5	PTE30		FTM0_CH3		FTM_CLKIN1		
28	19	—	ADCA_CH6d/ CMP0_IN4/ CMP2_IN3	ADCA_CH6d/ CMP0_IN4/ CMP2_IN3	ADCA_CH6d/ CMP0_IN4/ CMP2_IN3							
29	—	—	VSS	VSS	VSS							
30	—	—	VDD	VDD	VDD							
31	20	15	PTE24	ADCB_CH4	ADCB_CH4	PTE24	CAN1_TX	FTM0_CH0	XBAR0_IN2	I2C0_SCL	EWM_OUT_b	XBAR0_ OUT4
32	21	16	PTE25/ LLWU_P21	ADCB_CH5	ADCB_CH5	PTE25/ LLWU_P21	CAN1_RX	FTM0_CH1	XBAR0_IN3	I2C0_SDA	EWM_IN	XBAR0_ OUT5
33	—	—	PTE26	DISABLED		PTE26						

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
34	22	17	PTA0	JTAG_TCLK/ SWD_CLK		PTA0	UART0_CTS_b/ UART0_COL_b	FTM0_CH5	XBAR0_IN4	EWM_IN		JTAG_TCLK/ SWD_CLK
35	23	18	PTA1	JTAG_TDI		PTA1	UART0_RX	FTM0_CH6	CMP0_OUT		FTM1_CH1	JTAG_TDI
36	24	19	PTA2	JTAG_TDO/ TRACE_SWO		PTA2	UART0_TX	FTM0_CH7	CMP1_OUT		FTM1_CH0	JTAG_TDO/ TRACE_SWO
37	25	20	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_RTS_b	FTM0_CH0	XBAR0_IN9	EWM_OUT_b	FLEXPWMA_A0	JTAG_TMS/ SWD_DIO
38	26	21	PTA4/ LLWU_P3	NMI_b		PTA4/ LLWU_P3		FTM0_CH1	XBAR0_IN10	FTM0_FLT3	FLEXPWMA_B0	NMI_b
39	27	—	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT		JTAG_TRST_b
40	—	22	VDD	VDD	VDD							
41	—	23	VSS	VSS	VSS							
42	28	—	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0				FTM1_QD_PHA
43	29	—	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1				FTM1_QD_PHB
44	—	—	PTA14	CMP3_IN0	CMP3_IN0	PTA14	SPI0_PCS0	UART0_TX				
45	—	—	PTA15	CMP3_IN1	CMP3_IN1	PTA15	SPI0_SCK	UART0_RX				
46	—	—	PTA16	CMP3_IN2	CMP3_IN2	PTA16	SPI0_SOUT	UART0_CTS_b/ UART0_COL_b				
47	—	—	PTA17	ADCA_CH7e	ADCA_CH7e	PTA17	SPI0_SIN	UART0_RTS_b				
48	30	—	VDD	VDD	VDD							
49	31	—	VSS	VSS	VSS							
50	32	24	PTA18	EXTAL0	EXTAL0	PTA18	XBAR0_IN7	FTM0_FLT2	FTM_CLKIN0	XBAR0_OUT8	FTM3_CH2	
51	33	25	PTA19	XTAL0	XTAL0	PTA19	XBAR0_IN8	FTM1_FLT0	FTM_CLKIN1	XBAR0_OUT9	LPTMR0_ALT1	
52	34	26	RESET_b	RESET_b	RESET_b							
53	35	27	PTB0/ LLWU_P5	ADCB_CH2	ADCB_CH2	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA	UART0_RX
54	36	28	PTB1	ADCB_CH3	ADCB_CH3	PTB1	I2C0_SDA	FTM1_CH1	FTM0_FLT2	EWM_IN	FTM1_QD_PHB	UART0_TX
55	37	29	PTB2	ADCA_CH6e/ CMP2_IN2	ADCA_CH6e/ CMP2_IN2	PTB2	I2C0_SCL	UART0_RTS_b	FTM0_FLT1		FTM0_FLT3	
56	38	30	PTB3	ADCB_CH7e/ CMP3_IN5	ADCB_CH7e/ CMP3_IN5	PTB3	I2C0_SDA	UART0_CTS_b/ UART0_COL_b			FTM0_FLT0	
57	—	—	PTB9	DISABLED		PTB9						
58	—	—	PTB10	ADCB_CH6a	ADCB_CH6a	PTB10					FTM0_FLT1	

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
59	—	—	PTB11	ADCB_CH7a	ADCB_CH7a	PTB11					FTM0_FLT2	
60	—	—	VSS	VSS	VSS							
61	—	—	VDD	VDD	VDD							
62	39	31	PTB16	DISABLED		PTB16		UART0_RX	FTM_CLKIN2	CAN0_TX	EWM_IN	XBAR0_IN5
63	40	32	PTB17	DISABLED		PTB17		UART0_TX	FTM_CLKIN1	CAN0_RX	EWM_OUT_b	
64	41	—	PTB18	DISABLED		PTB18	CAN0_TX		FTM3_CH2			
65	42	—	PTB19	DISABLED		PTB19	CAN0_RX		FTM3_CH3			
66	—	—	PTB20	DISABLED		PTB20				FLEXPWMA_X0	CMP0_OUT	
67	—	—	PTB21	DISABLED		PTB21				FLEXPWMA_X1	CMP1_OUT	
67	100	D9	PTB21	DISABLED		PTB21	SPI2_SCK			FLEXPWMA_X1	CMP1_OUT	
68	—	—	PTB22	DISABLED		PTB22				FLEXPWMA_X2	CMP2_OUT	
68	101	C12	PTB22	DISABLED		PTB22	SPI2_SOUT			FLEXPWMA_X2	CMP2_OUT	
69	—	—	PTB23	DISABLED		PTB23		SPI0_PCS5		FLEXPWMA_X3	CMP3_OUT	
69	102	C11	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FLEXPWMA_X3	CMP3_OUT	
70	43	33	PTC0	ADCB_CH6b	ADCB_CH6b	PTC0	SPI0_PCS4	PDB0_EXTRG			FTM0_FLT1	SPI0_PCS0
70	103	B12	PTC0	ADCB_CH6b	ADCB_CH6b	PTC0	SPI0_PCS4	PDB0_EXTRG			FTM0_FLT1	SPI0_PCS0
71	44	34	PTC1/ LLWU_P6	ADCB_CH7b	ADCB_CH7b	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FLEXPWMA_A3	XBAR0_IN11	
71	104	B11	PTC1/ LLWU_P6	ADCB_CH7b	ADCB_CH7b	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FLEXPWMA_A3	XBAR0_IN11	
72	45	35	PTC2	ADCB_CH6c/ CMP1_IN0	ADCB_CH6c/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FLEXPWMA_B3	XBAR0_IN6	
72	105	A12	PTC2	ADCD_CH6c/ CMP1_IN0	ADCD_CH6c/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FLEXPWMA_B3	XBAR0_IN6	
73	46	36	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	FTM3_FLT0	
73	106	A11	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	FTM3_FLT0	
74	47	—	VSS	VSS	VSS							
74	107	H8	VSS	VSS	VSS							
75	48	—	VDD	VDD	VDD							
75	108	—	VDD	VDD	VDD							
76	49	37	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	
76	109	A9	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	

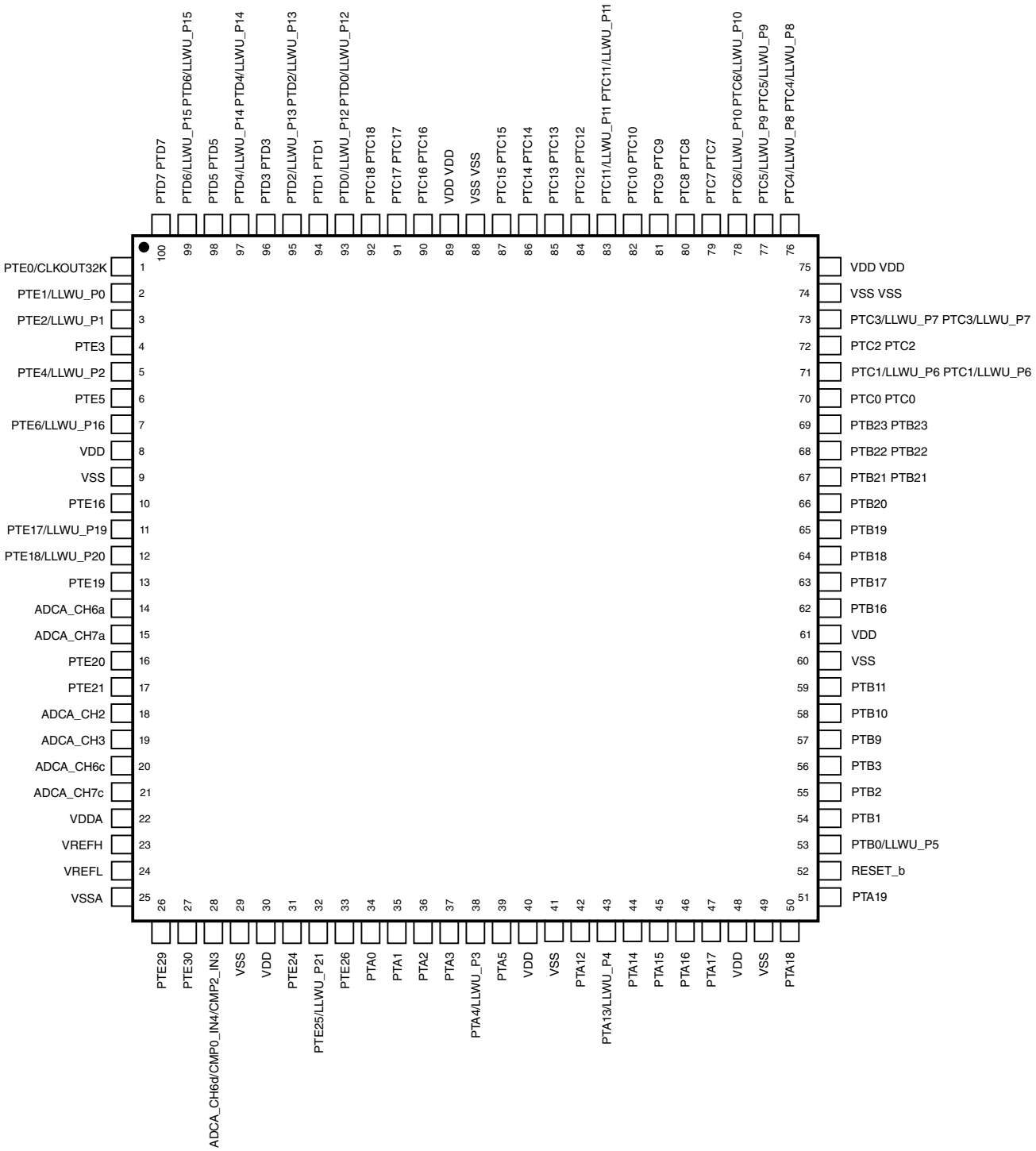
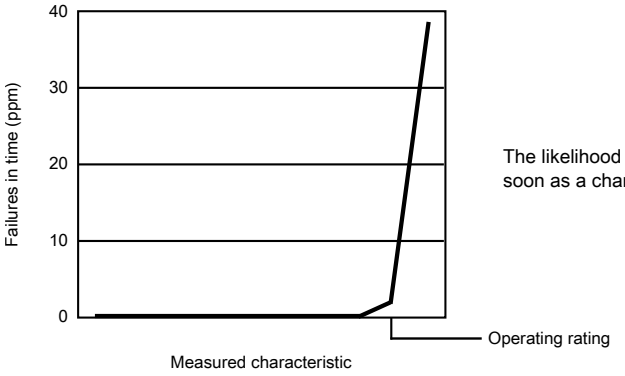


Figure 22. 100-pin LQFP

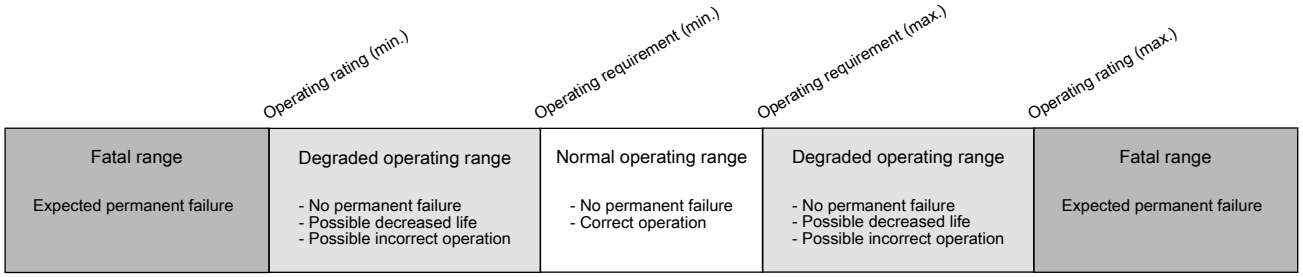
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

8.5 Result of exceeding a rating

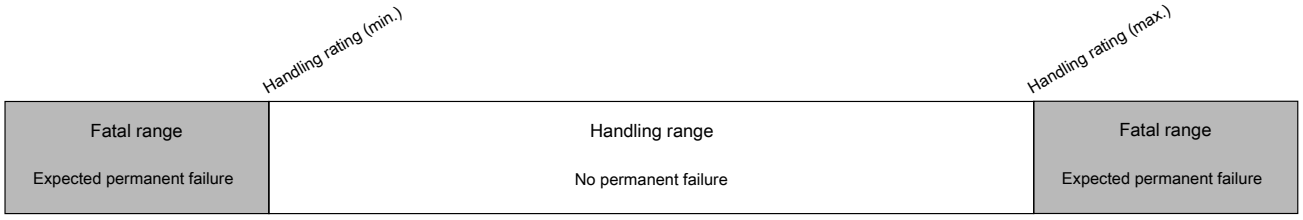


The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

8.6 Relationship between ratings and operating requirements



Operating (power on)



Handling (power off)

8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions: