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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	74
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv46f256vll15

Table 3. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 PORT Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Notes[1]	Min	Typ	Max	Unit	Test Conditions
V_{OH}[2]	Output Voltage High	Pin Group 1	V_{DD} - 0.5	—	—	V	$I_{OH} = I_{OHmax}$
V_{OL}	Output Voltage Low	Pin Groups 1, 2	—	—	0.5	V	$I_{OL} = I_{OLmax}$
I_{IH}	Digital Input Current High pull-up enabled or disabled	Pin Groups 1, 2	—	0	+/- 2.5	µA	V_{IN} = 2.4V to 5.5V
I_{IHC}	Comparator Input Current High	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
I_{IHOSC}	Oscillator Input Current High	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
I_{IL}	Digital Input Current Low • pull-up enabled • pull-up disabled	Pin Groups 1, 2	TBD TBD	TBD TBD	TBD TBD	µA	V_{IN} = 0V
$R_{Pull-Up}$	Internal Pull-Up Resistance		20	—	50	kΩ	—
I_{ILC}	Comparator Input Current Low	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
I_{ILOSC}	Oscillator Input Current Low	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
V_{DAC}	DAC Output Voltage Range	Pin Group 5	Typically V_{SSA} + 40mV	—	Typically V_{DDA} - 40mV	V	R_{LD} = 3 kΩ || C_{LD} = 400 pf
I_{OZ}	Output Current[1] High Impedance State	Pin Groups 1, 2	—	0	+/- 2.5	µA	—
V_{HYS}	Schmitt Trigger Input Hysteresis	Pin Groups 1, 2	—	0.06 x V_{DD}	—	V	—
C_{IN}	Input Capacitance		—	10	—	pF	—
C_{OUT}	Output Capacitance		—	10	—	pF	—

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK

Table 6. Power consumption operating behaviors (All IDDs are Target values) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
						and clocked at 5 MHz.
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes ADC IDDA • @ 1.8V • @ 3.0V	 — —	 6.5 6.6	 14 15	 mA mA	ADC/DAC powered on and clocked at 5 MHz. Core frequency of 25 MHz
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes ADC IDDA • @ 1.8V • @ 3.0V	 — —	 9.6 9.8	 18 20	 mA mA	ADC/DAC powered on and clocked at 5 MHz. Core frequency of 50 MHz
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes ADC IDDA • @ 1.8V • @ 3.0V	 — —	 16.1 16.2	 18 20	 mA mA	ADC/DAC powered on and clocked at 5 MHz. Core frequency of 100 MHz.
I_{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes ADC IDDA • @ 1.8V • @ 3.0V	— — 	 25.3 25.7	 50 60	 mA mA	ADC/DAC powered on and clocked at 5 MHz. Core frequency of 150 MHz.

I_{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code executing from flash,excludes ADC IDDA
	• @ 1.8V @ ambient
	• @ 3.0V
	  • @ 25°C
	  • @ 105°C
		
		—
		
		—
		—
			
			33.7
			
			33.1
			39.6
				
				90
				
				100
				120
					
					mA
					
					mA
					mA
						ADC/DAC powered on and clocked at 5 MHz. Core frequency of 150 MHz. Nanoedge module at 75 MHz.

I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	8.6	—	mA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.574	—	mA	CPU freq 4Mhz
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	0.836	—	mA	CPU freq 4Mhz
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.285	—	mA	2Mhz bus frequency
I_{DD_STOP}	Stop mode current at 3.0 V	—	0.366	2		

Table continues on the next page...

Table 6. Power consumption operating behaviors (All IDDs are Target values) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ –40 to 25°C	—	0.868	TBD	mA	
	• @ 70°C	—	3.5	TBD	mA	
	• @ 105°C				mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.059	TBD	µA	
	• @ 70°C	—	—	TBD	µA	
	• @ 105°C	—	0.717	TBD	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ –40 to 25°C	—	0.124	TBD	mA	
	• @ 70°C	—	3.8	TBD	mA	
	• @ 105°C	—	—	TBD	mA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	0.122	TBD	mA	
	• @ 70°C	—	3.7	TBD	mA	
	• @ 105°C	—	4.1	TBD	mA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	749	TBD	nA	
	• @ 70°C	—	2.2	TBD	µA	
	• @ 105°C	—	9.9	TBD	µA	
I_{DD_VLLS0B}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• @ –40 to 25°C	—	470	TBD	nA	
	• @ 70°C	—	1.9	TBD	µA	
	• @ 105°C	—	9.5	TBD	µA	
I_{DD_VLLS0A}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• @ –40 to 25°C	—	180	TBD	nA	
	• @ 70°C	—	1.6	TBD	µA	
	• @ 105°C	—	9.1	TBD	µA	

- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

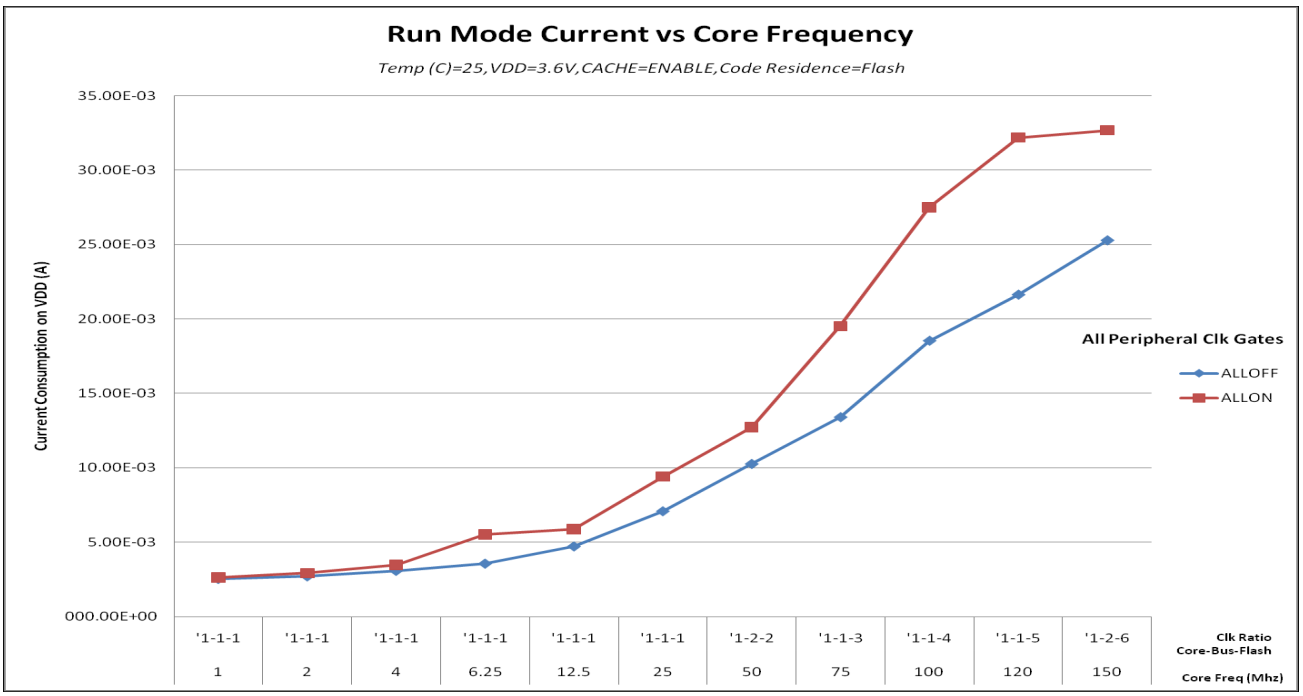


Figure 3. Run mode supply current vs. core frequency

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I^2C signals.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time Fast slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 8 7	 ns ns	3
	Port rise and fall time Slow slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 25 15	 ns ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. For high drive pins with high drive enabled, load is 75pF; other pins load (low drive) is 25pF.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

2.4.2 Thermal attributes

Table 13. Thermal attributes

Board type	Symbol	Description	100 LQFP	64 LQFP	48 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	62	64	81	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	49	46	57	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	52	68	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	43	39	51	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	28	35	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	17	15	25	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	2	7	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD Electricals

Table 14. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation			

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	2929 × f_{fll_ref}					
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz	— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6
	PLL					
f_{pll_ref}	PLL reference frequency range	8	—	16	MHz	
f_{vcoclk_2x}	VCO output frequency	180	—	360	MHz	
f_{vcoclk}	PLL output frequency	90	—	180	MHz	
f_{vcoclk_90}	PLL quadrature output frequency	90	—	180	MHz	
I_{pll}	PLL operating current • VCO @ 176 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 22)	—	2.8	—	mA	7
I_{pll}	PLL operating current • VCO @ 360 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)	—	4.7	—	mA	7
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz	 — —	 120 75	 — —	 ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz	 — —	 1350 600	 — —	 ps ps	8
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	150 × 10^{-6} + 1075(1/f_{pll_ref})	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 4 MHz	—	400	—	µA	
	• 8 MHz	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	

Table continues on the next page...

Table 25. 12-bit ADC electrical specifications (continued)

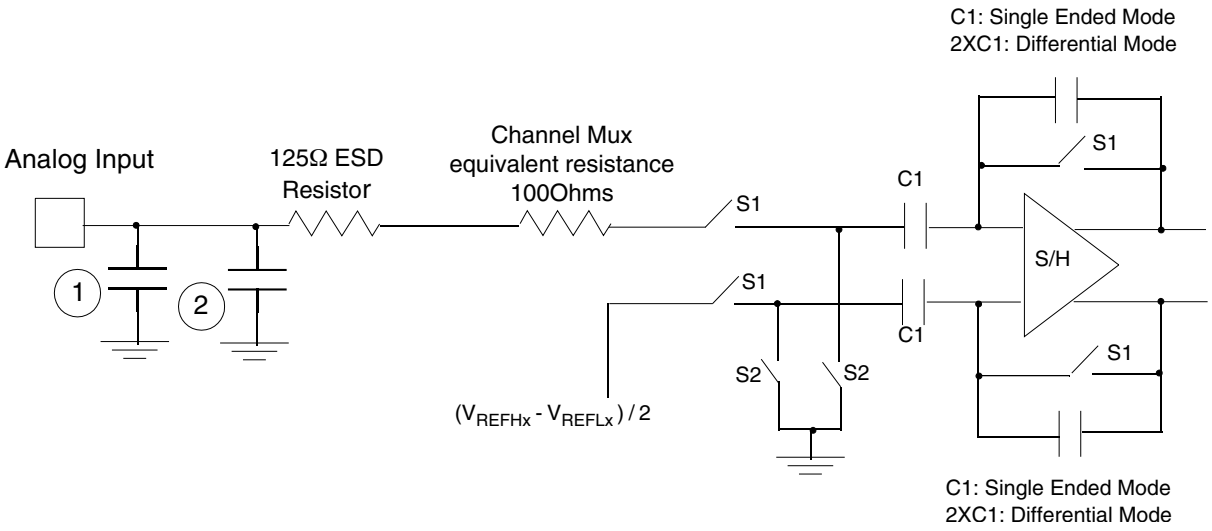
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage Range External Reference Internal Reference	V_{ADIN}	V_{REFL} V_{SSA}		V_{REFH} V_{DDA}	V
Timing and Power					
Conversion Time	t_{ADC}		6		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		13		ADC Clock Cycles
ADC RUN Current (per ADC block) • at 600 kHz ADC Clock, LP mode • ≤ 8.33 MHz ADC Clock, 00 mode • ≤ 12.5 MHz ADC Clock, 01 mode • ≤ 16.67 MHz ADC Clock, 10 mode • ≤ 20 MHz ADC Clock, 11 mode • ≤ 25 MHz ADC Clock	I_{ADRUN}		 1 5.7 10.5 17.7 22.6 TBD		mA
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.02		µA
V_{REFH} Current	I_{VREFH}		0.001		µA
Accuracy (DC or Absolute)					
Integral non-Linearity	I_{NL}		+/- 3	+/- 5	LSB
Differential non-Linearity[1]	DNL		+/- 0.6	+/- 0.9	LSB[2]
Monotonicity					
Offset • 1x gain mode • 2x gain mode • 4x gain mode	V_{OFFSET}			 +/- 17 +/- 20 +/- 25	mV
Gain Error	E_{GAIN}		0.801 to 0.809	0.798 to 0.814	
AC Specifications					
Signal to Noise Ratio	SNR		59		dB
Total Harmonic Distortion	THD		64		dB
Spurious Free Dynamic Range	SFDR		65		dB
Signal to Noise plus Distortion	SINAD		59		dB
Effective Number of Bits	ENOB		9.5		bits
ADC Inputs					
Input Leakage Current	I_{IN}		0	+/-2	µA
Input Injection Current	I_{INJ}			+/-3	mA
Input Capacitance Sampling Capacitor	C_{ADI}		4.8		pF

1. I_{NL} measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$.
2. LSB = Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 Gain Setting

3.6.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 operate at the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 1.4 \times 10^{-12}} + 100ohm + 125ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. Sampling capacitor at the sample and hold circuit. Capacitor C1 (4.8pF) is normally disconnected from the input, and is only connected to the input at sampling time.
4. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency

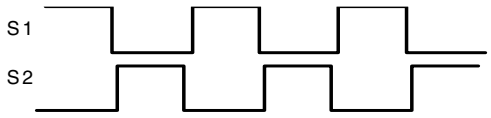


Figure 13. Equivalent circuit for A/D loading

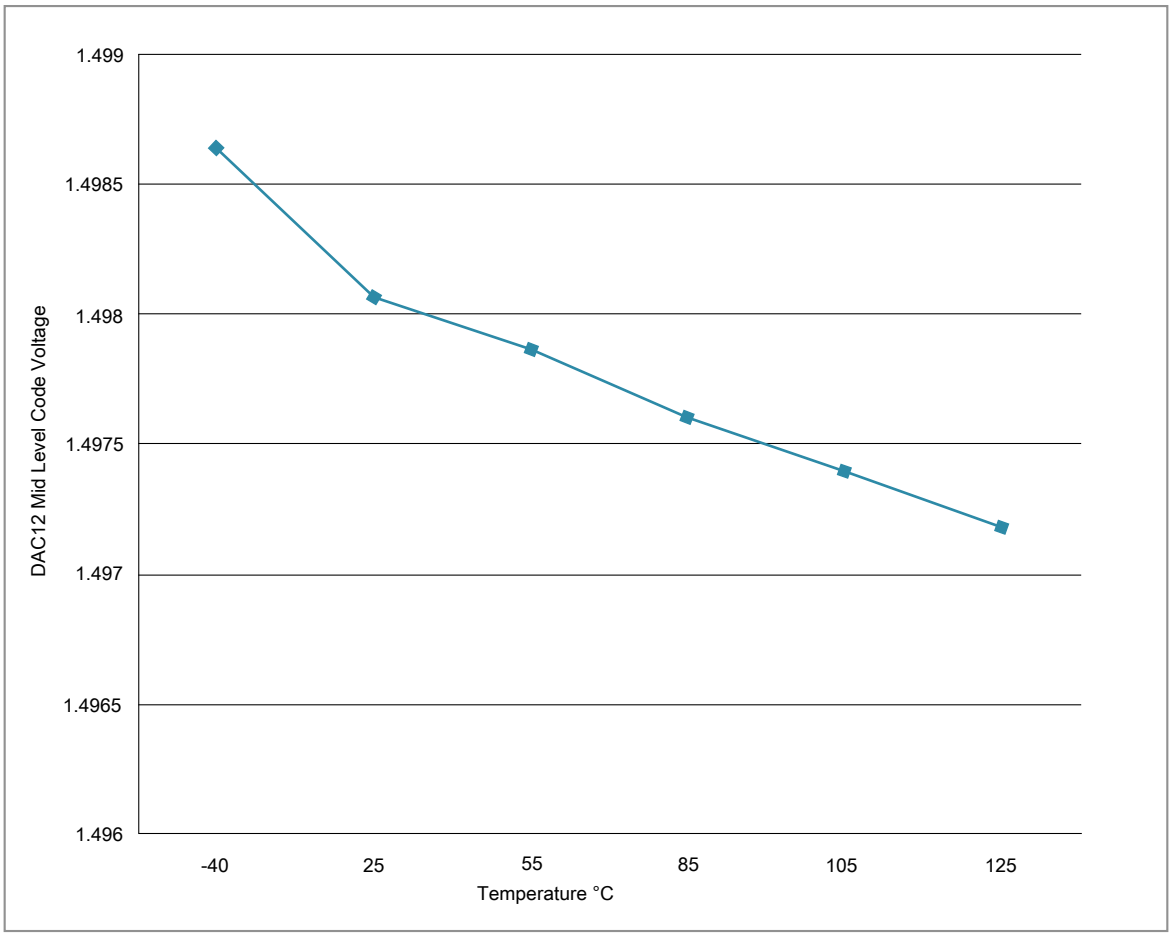


Figure 17. Offset at half scale vs. temperature

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

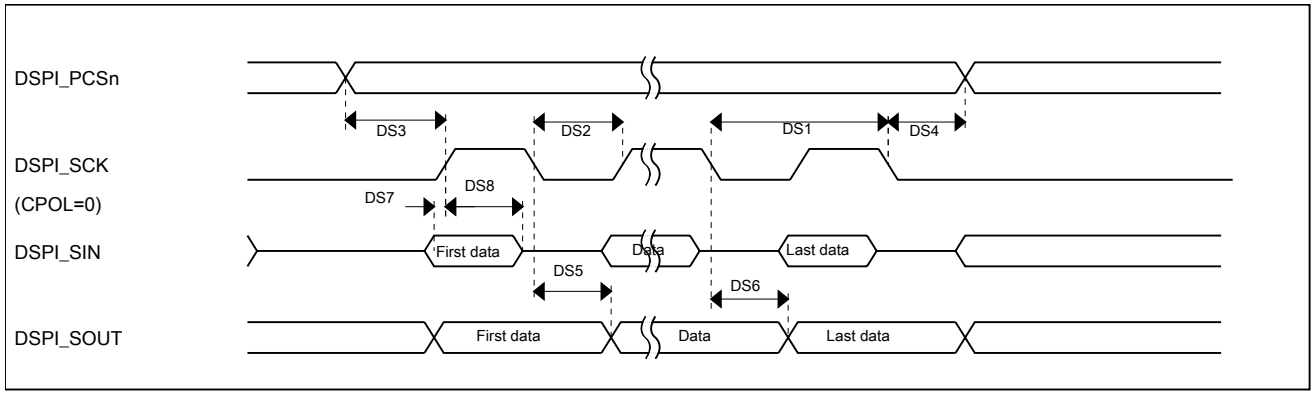


Figure 18. DSPI classic SPI timing — master mode

Table 32. Slave mode DSPI timing for normal pads (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	21	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	15	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	15	ns

Table 33. Slave mode DSPI timing for fast pads (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		25	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	17	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	11	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	11	ns

3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 37. Master mode DSPI timing open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	18.75	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	26	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-7.8	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

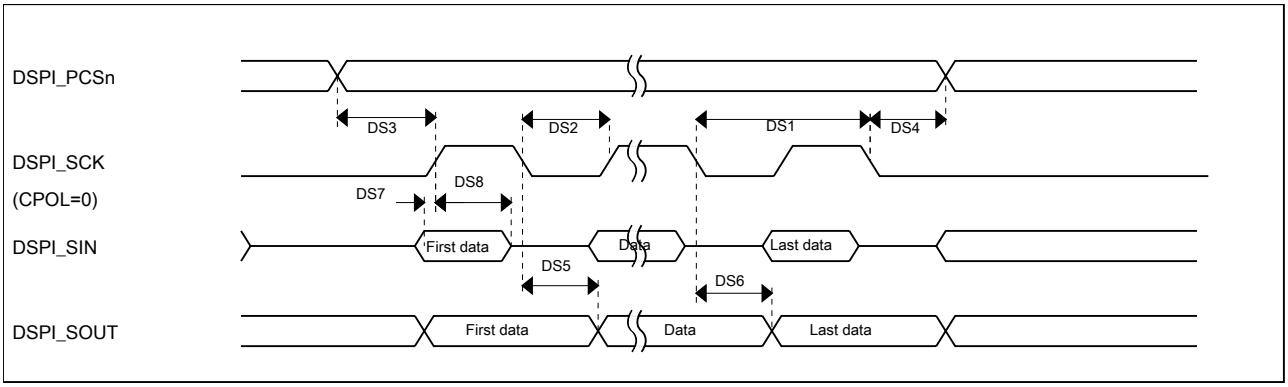


Figure 20. DSPI classic SPI timing — master mode

Table 38. Slave mode DSPI timing for normal pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	12.5	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	27.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns

Table continues on the next page...

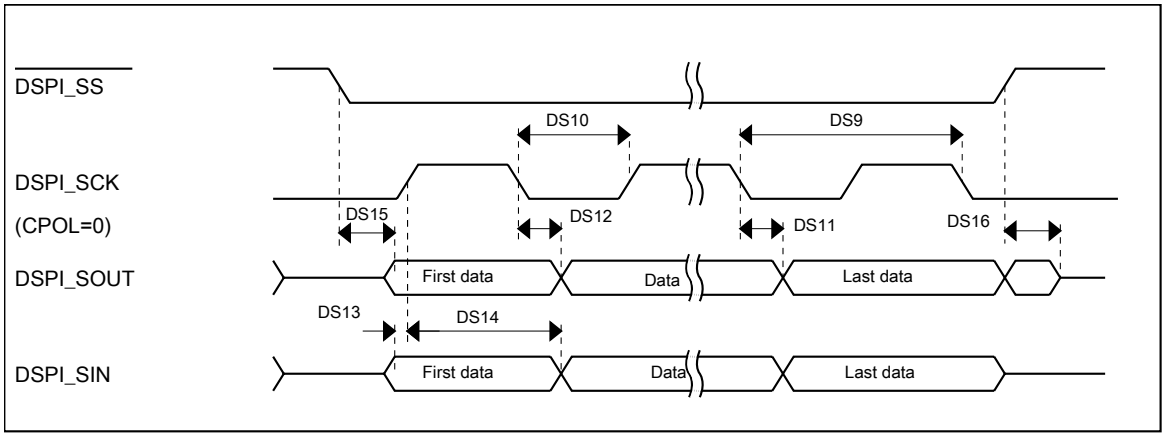


Figure 21. DSPI classic SPI timing — slave mode

3.8.3 I²C

See General switching specifications.

3.8.4 UART

See General switching specifications.

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W

5 Pinout

5.1 KV4x Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

The 48-pin LQFP package for this product is not yet available. However, it is included in a Package Your Way program for Kinetis MCUs. Visit freescale.com/KPYW for more details.

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	126	B5	PTC19	DISABLED		PTC19		UART3_CTS_b	ENET0_1588_TMR3	FLEXPWMB_B3		
—	134	M10	VSS	DISABLED	VSS							
—	135	F8	VDD	DISABLED	VDD							
—	137	C9	PTD8/LLWU_P24	DISABLED		PTD8/LLWU_P24	I2C1_SCL	UART5_RX			FLEXPWMA_A3	
—	138	B9	PTD9	DISABLED		PTD9	I2C1_SDA	UART5_TX			FLEXPWMA_B3	
—	139	B3	PTD10	DISABLED		PTD10		UART5_RTS_b			FLEXPWMA_A2	
—	140	B2	PTD11/LLWU_P25	DISABLED		PTD11/LLWU_P25	SPI2_PCS0	UART5_CTS_b			FLEXPWMA_B2	
—	141	B1	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	XBAR0_IN5	XBAR0_OUT5	FLEXPWMA_A1	
—	142	C3	PTD13	DISABLED		PTD13	SPI2_SOUT		XBAR0_IN7	XBAR0_OUT7	FLEXPWMA_B1	
—	143	C2	PTD14	DISABLED		PTD14	SPI2_SIN		XBAR0_IN11	XBAR0_OUT11	FLEXPWMA_A0	
—	144	C1	PTD15	DISABLED		PTD15	SPI2_PCS1				FLEXPWMA_B0	
1	1	—	PTE0/CLKOUT32K	ADCB_CH6f	ADCB_CH6f	PTE0/CLKOUT32K		UART1_TX	XBAR0_OUT10	XBAR0_IN11		
2	2	—	PTE1/LLWU_P0	ADCB_CH7f	ADCB_CH7f	PTE1/LLWU_P0		UART1_RX	XBAR0_OUT11	XBAR0_IN7		
3	—	—	PTE2/LLWU_P1	ADCB_CH6g	ADCB_CH6g	PTE2/LLWU_P1		UART1_CTS_b				

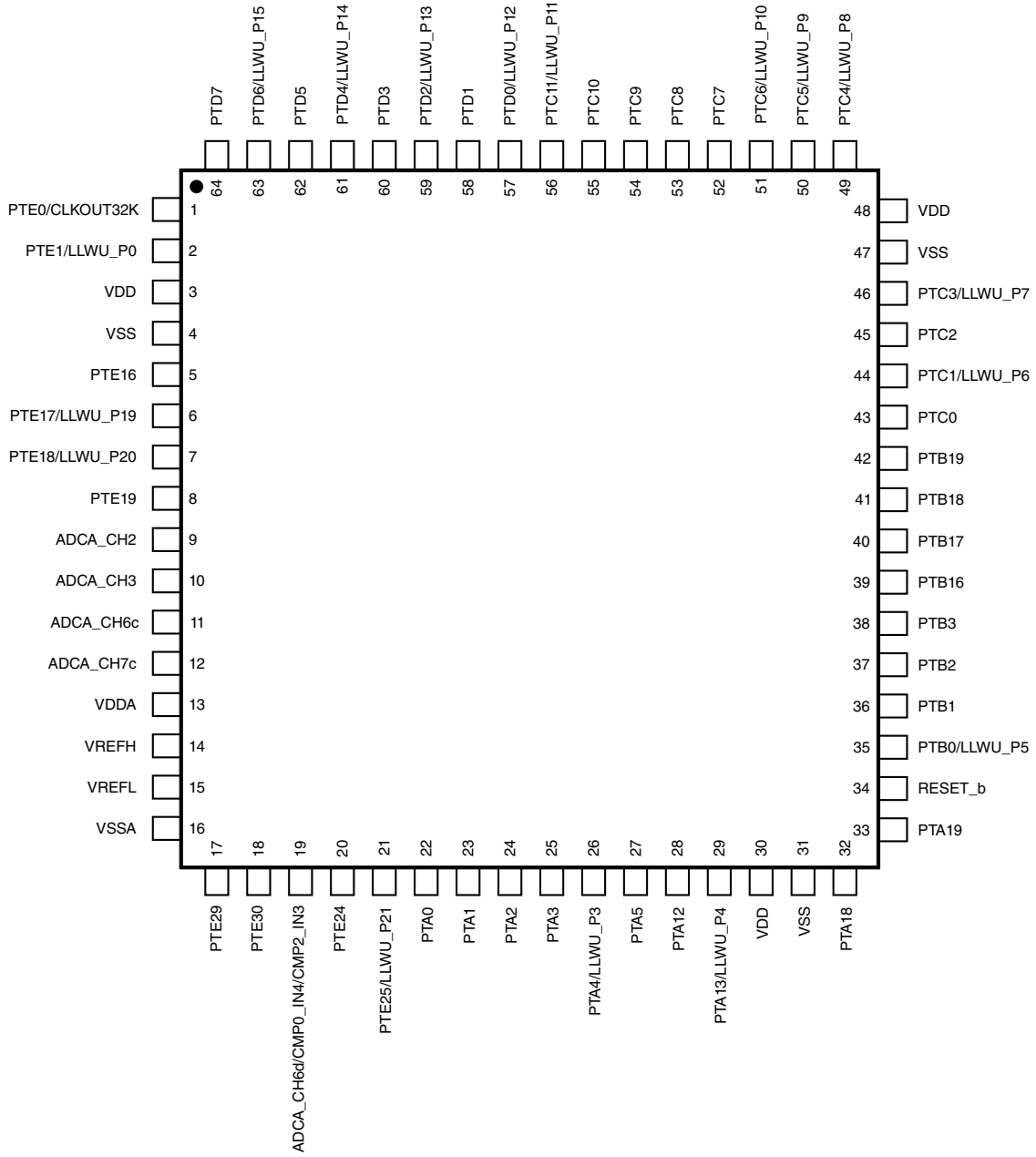


Figure 23. 64-pin LQFP

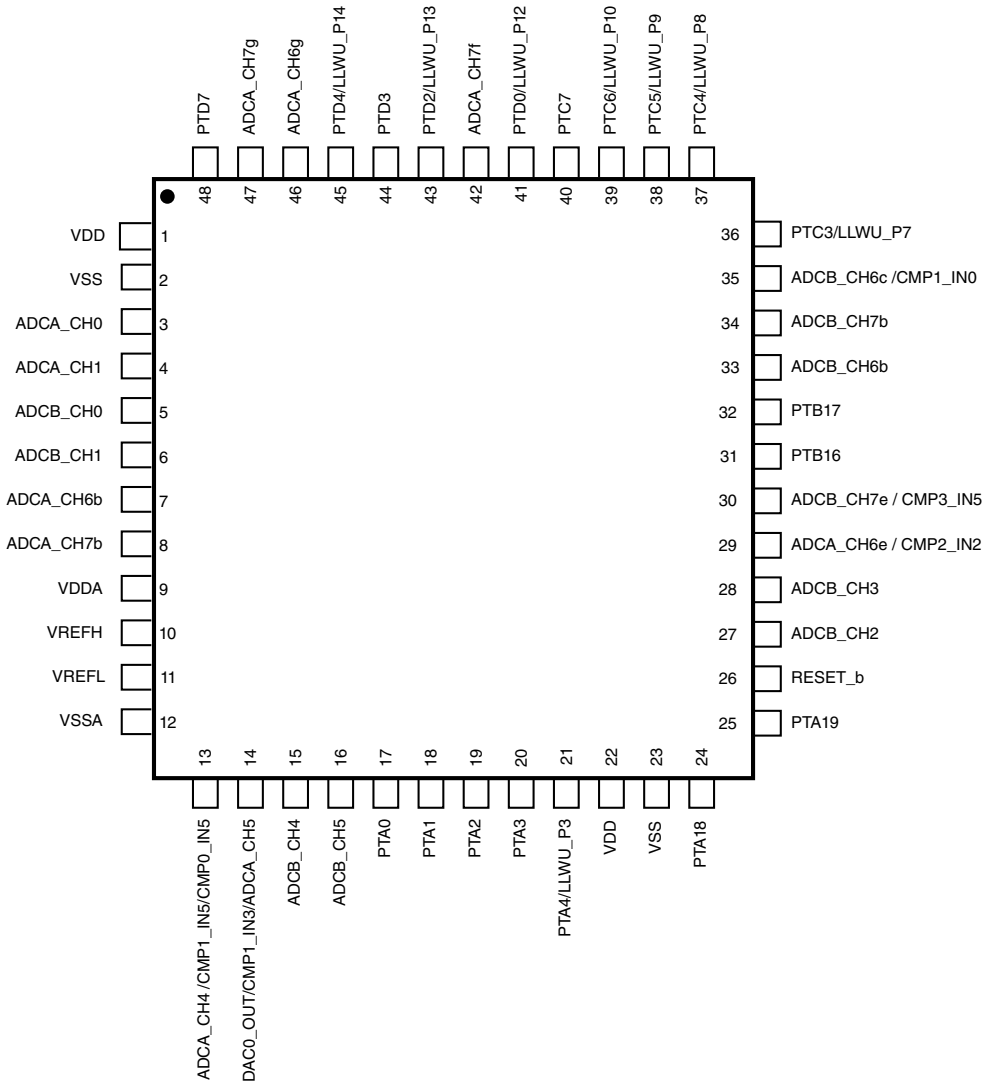


Figure 24. 48-pin LQFP

6 Ordering parts

Field	Description	Values
		• LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CCC	Maximum CPU frequency (MHz)	• 15 = 150 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKV46F256VLL15

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

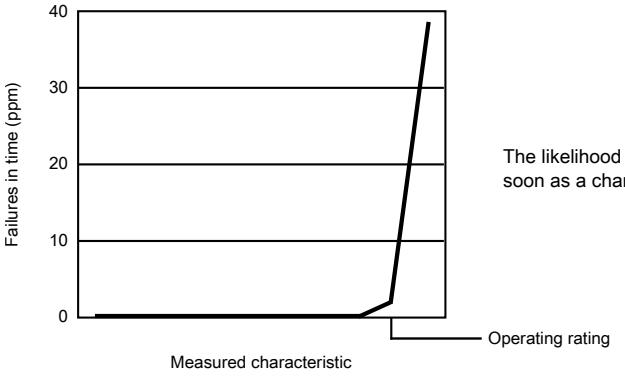
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

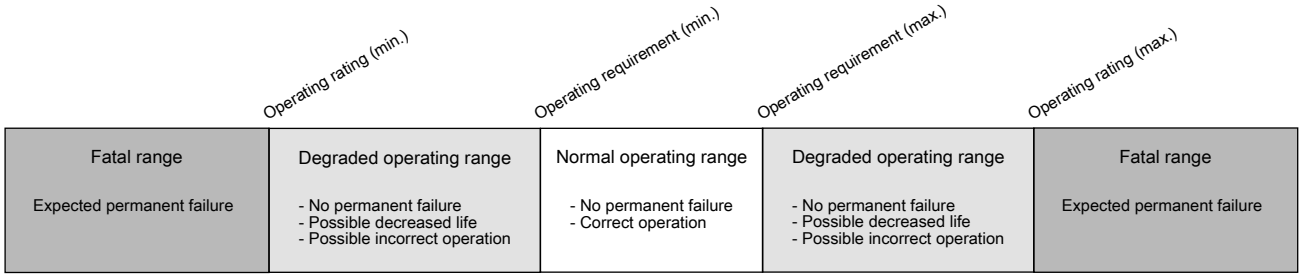
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

8.5 Result of exceeding a rating

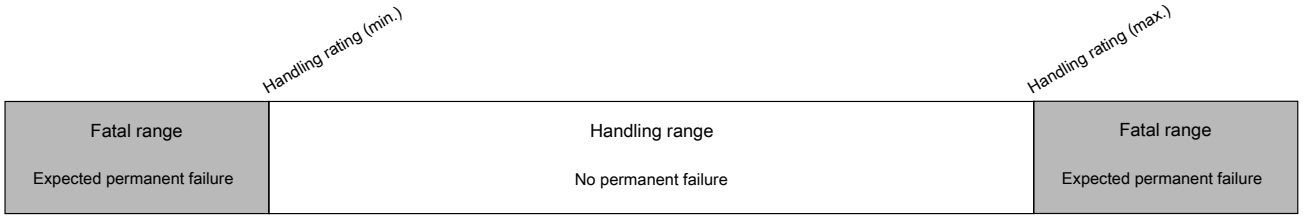


The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

8.6 Relationship between ratings and operating requirements



Operating (power on)



Handling (power off)

8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

Table 41. Revision history

Rev. No.	Date	Substantial Changes
		• Obtaining package dimensions • Pinout • In table "Power consumption operating behaviors", removed the text "Maximum core fequency of 150 Mhz" from note for I_{DDA}. • In table "Typical device clock specifications", removed information about High Speed run mode.