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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	109
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1774fbd144-551

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[5]	166	C12	B11	115	[3]	I; PU	I/O	**P0[5] —** General purpose digital input/output pin.
							I/O	**I2S_RX_WS —** I^2S Receive word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							O	**CAN_TD2 —** CAN2 transmitter output.
							I	**T2_CAP1 —** Capture input for Timer 2, channel 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[1] —** LCD data.
P0[6]	164	D13	D11	113	[3]	I; PU	I/O	**P0[6] —** General purpose digital input/output pin.
							I/O	**I2S_RX_SDA —** I^2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							O	**T2_MAT0 —** Match output for Timer 2, channel 0.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[8] —** LCD data.
P0[7]	162	C13	B12	112	[4]	I; IA	I/O	**P0[7] —** General purpose digital input/output pin.
							I/O	**I2S_TX_SCK —** I^2S transmit clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							I/O	**SSP1_SCK —** Serial Clock for SSP1.
							O	**T2_MAT1 —** Match output for Timer 2, channel 1.
							I	**RTC_EV0 —** Event input 0 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[9] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[16]	180	D10	B8	125	[3]	I; PU	I/O	**P1[16] —** General purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet MIIM clock.
							O	**I2S_TX_MCLK —** I2S transmit master clock.
P1[17]	178	A9	C9	123	[3]	I; PU	I/O	**P1[17] —** General purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
							O	**I2S_RX_MCLK —** I2S receive master clock.
P1[18]	66	P7	L5	46	[3]	I; PU	I/O	**P1[18] —** General purpose digital input/output pin.
							O	**USB_UP_LED1 —** It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
							O	**PWM1[1] —** Pulse Width Modulator 1, channel 1 output.
							I	**T1_CAP0 —** Capture input for Timer 1, channel 0.
							-	**R —** Function reserved.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
P1[19]	68	U6	P5	47	[3]	I; PU	I/O	**P1[19] —** General purpose digital input/output pin.
							O	**$\overline{\text{USB\_TX\_E1}}$ —** Transmit Enable signal for USB port 1 (OTG transceiver).
							O	**$\overline{\text{USB\_PPWR1}}$ —** Port Power enable signal for USB port 1.
							I	**T1_CAP1 —** Capture input for Timer 1, channel 1.
							O	**MC_0A —** Motor control PWM channel 0, output A.
							I/O	**SSP1_SCK —** Serial clock for SSP1.
							O	**U2_OE —** RS-485/EIA-485 output enable signal for UART2.
P1[20]	70	U7	K6	49	[3]	I; PU	I/O	**P1[20] —** General purpose digital input/output pin.
							O	**USB_TX_DP1 —** D+ transmit data for USB port 1 (OTG transceiver).
							O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
							I	**QEI_PHA —** Quadrature Encoder Interface PHA input.
							I	**MC_FB0 —** Motor control PWM channel 0 feedback input.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
							O	**LCD_VD[6] —** LCD data.
							O	**LCD_VD[10] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P2[5]	140	F16	F12	97	[3]	I; PU	I/O	**P2[5] —** General purpose digital input/output pin.
							O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							O	**T2_MAT0 —** Match output for Timer 2, channel 0.
							-	**R —** Function reserved.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
P2[6]	138	E17	F13	96	[3]	I; PU	I/O	**P2[6] —** General purpose digital input/output pin.
							I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
							I	**U1_RI —** Ring Indicator input for UART1.
							I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
							O	**U2_OE —** RS-485/EIA-485 output enable signal for UART2.
							O	**TRACECLK —** Trace clock.
							O	**LCD_VD[0] —** LCD data.
							O	**LCD_VD[4] —** LCD data.
P2[7]	136	G16	G11	95	[3]	I; PU	I/O	**P2[7] —** General purpose digital input/output pin.
							I	**CAN_RD2 —** CAN2 receiver input.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[1] —** LCD data.
							O	**LCD_VD[5] —** LCD data.
P2[8]	134	H15	G14	93	[3]	I; PU	I/O	**P2[8] —** General purpose digital input/output pin.
							O	**CAN_TD2 —** CAN2 transmitter output.
							O	**U2_TXD —** Transmitter output for UART2.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**ENET_MDC —** Ethernet MIIM clock.
							-	**R —** Function reserved.
							O	**LCD_VD[2] —** LCD data.
							O	**LCD_VD[6] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P3[17]	143	F15	-	-	[3]	I; PU	I/O	**P3[17] —** General purpose digital input/output pin.
							I/O	**EMC_D[17] —** External memory data line 17.
							O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
							I	**U1_RXD —** Receiver input for UART1.
P3[18]	151	C15	-	-	[3]	I; PU	I/O	**P3[18] —** General purpose digital input/output pin.
							I/O	**EMC_D[18] —** External memory data line 18.
							O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
							I	**U1_CTS —** Clear to Send input for UART1.
P3[19]	161	B14	-	-	[3]	I; PU	I/O	**P3[19] —** General purpose digital input/output pin.
							I/O	**EMC_D[19] —** External memory data line 19.
							O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
P3[20]	167	A13	-	-	[3]	I; PU	I/O	**P3[20] —** General purpose digital input/output pin.
							I/O	**EMC_D[20] —** External memory data line 20.
							O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
							I	**U1_DSR —** Data Set Ready input for UART1.
P3[21]	175	C10	-	-	[3]	I; PU	I/O	**P3[21] —** General purpose digital input/output pin.
							I/O	**EMC_D[21] —** External memory data line 21.
							O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
P3[22]	195	C6	-	-	[3]	I; PU	I/O	**P3[22] —** General purpose digital input/output pin.
							I/O	**EMC_D[22] —** External memory data line 22.
							I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
							I	**U1_RI —** Ring Indicator input for UART1.
P3[23]	65	T6	M4	45	[3]	I; PU	I/O	**P3[23] —** General purpose digital input/output pin.
							I/O	**EMC_D[23] —** External memory data line 23.
							I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
							I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
P3[24]	58	R5	N3	40	[3]	I; PU	I/O	**P3[24] —** General purpose digital input/output pin.
							I/O	**EMC_D[24] —** External memory data line 24.
							O	**PWM1[1] —** Pulse Width Modulator 1, output 1.
							I	**T0_CAP1 —** Capture input for Timer 0, channel 1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P3[25]	56	U2	M3	39	[3]	I; PU	I/O	**P3[25] —** General purpose digital input/output pin.
							I/O	**EMC_D[25] —** External memory data line 25.
							O	**PWM1[2] —** Pulse Width Modulator 1, output 2.
							O	**T0_MAT0 —** Match output for Timer 0, channel 0.
P3[26]	55	T3	K7	38	[3]	I; PU	I/O	**P3[26] —** General purpose digital input/output pin.
							I/O	**EMC_D[26] —** External memory data line 26.
							O	**PWM1[3] —** Pulse Width Modulator 1, output 3.
							O	**T0_MAT1 —** Match output for Timer 0, channel 1.
							I	**STCLK —** System tick timer clock input. The maximum STCLK frequency is 1/4 of the ARM processor clock frequency CCLK.
P3[27]	203	A1	-	-	[3]	I; PU	I/O	**P3[27] —** General purpose digital input/output pin.
							I/O	**EMC_D[27] —** External memory data line 27.
							O	**PWM1[4] —** Pulse Width Modulator 1, output 4.
							I	**T1_CAP0 —** Capture input for Timer 1, channel 0.
P3[28]	5	D2	-	-	[3]	I; PU	I/O	**P3[28] —** General purpose digital input/output pin.
							I/O	**EMC_D[28] —** External memory data line 28.
							O	**PWM1[5] —** Pulse Width Modulator 1, output 5.
							I	**T1_CAP1 —** Capture input for Timer 1, channel 1.
P3[29]	11	F3	-	-	[3]	I; PU	I/O	**P3[29] —** General purpose digital input/output pin.
							I/O	**EMC_D[29] —** External memory data line 29.
							O	**PWM1[6] —** Pulse Width Modulator 1, output 6.
							O	**T1_MAT0 —** Match output for Timer 1, channel 0.
P3[30]	19	H3	-	-	[3]	I; PU	I/O	**P3[30] —** General purpose digital input/output pin.
							I/O	**EMC_D[30] —** External memory data line 30.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							O	**T1_MAT1 —** Match output for Timer 1, channel 1.
P3[31]	25	J3	-	-	[3]	I; PU	I/O	**P3[31] —** General purpose digital input/output pin.
							I/O	**EMC_D[31] —** External memory data line 31.
							-	**R —** Function reserved.
							O	**T1_MAT2 —** Match output for Timer 1, channel 2.
P4[0] to P4[31]							I/O	**Port 4:** Port 4 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 4 pins depends upon the pin function selected via the pin connect block.
P4[0]	75	U9	L6	52	[3]	I; PU	I/O	**P4[0] —** General purpose digital input/output pin.
							I/O	**EMC_A[0] —** External memory address line 0.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P5[3]	141	G14	G10	98	[11]	I	I/O	**P5[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**U4_RXD —** Receiver input for USART4.
							I/O	**I2C0_SCL —** I^2C0 clock input/output (this pin uses a specialized I^2C pad that supports I^2C Fast Mode Plus).
P5[4]	206	C3	C4	143	[3]	I; PU	I/O	**P5[4] —** General purpose digital input/output pin.
							O	**U0_OE —** RS-485/EIA-485 output enable signal for UART0.
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output for Timer 3, channel 3.
							O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
JTAG_TDO (SWO)	2	D3	B1	1	[3]	O	O	Test Data Out for JTAG interface. Also used as Serial wire trace output.
JTAG_TDI	4	C2	C3	3	[3]	I; PU	I	Test Data In for JTAG interface.
JTAG_TMS (SWDIO)	6	E3	C2	4	[3]	I; PU	I	Test Mode Select for JTAG interface. Also used as Serial wire debug data input/output.
JTAG_$\overline{\text{TRST}}$	8	D1	D4	5	[3]	I; PU	I	Test Reset for JTAG interface.
JTAG_TCK (SWDCLK)	10	E2	D2	7	[3]	i	I	Test Clock for JTAG interface. This clock must be slower than 1/6 of the CPU clock (CCLK) for the JTAG interface to operate. Also used as serial wire clock.
$\overline{\text{RESET}}$	35	M2	J1	24	[12]	I; PU	I	External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
$\overline{\text{RSTOUT}}$	29	K3	H2	20	[3]	OH	O	Reset status output. A LOW output on this pin indicates that the device is in the reset state for any reason. This reflects the $\overline{\text{RESET}}$ input pin and all internal reset sources.
RTC_ALARM	37	N1	H5	26	[13]	OL	O	RTC controlled output. This pin has a low drive strength and is powered by VBAT. It is driven HIGH when an RTC alarm is generated.
RTCX1	34	K2	J2	23	[14] [15]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	36	L2	J3	25	[14] [15]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
USB_D−2	52	U1	N2	37	[9]	-	I/O	USB port 2 bidirectional D− line.

Table 7. External memory controller pin configuration

Part	Data bus pins	Address bus pins	Control pins	
			SRAM	SDRAM
LPC1788FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1788FET208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1788FET180	EMC_D[15:0]	EMC_A[19:0]	EMC_BLS[1:0], EMC_CS[1:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC1788FBD144	EMC_D[7:0]	EMC_A[15:0]	EMC_BLS[3:2], EMC_CS[1:0], EMC_OE, EMC_WE	not available
LPC1787FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS_[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1786FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1785FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1778FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1778FET208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1778FET180	EMC_D[15:0]	EMC_A[19:0]	EMC_BLS[1:0], EMC_CS[1:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC1778FBD144	EMC_D[7:0]	EMC_A[15:0]	EMC_CS[1:0], EMC_OE, EMC_WE	not available
LPC1777FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1776FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1776FET180	EMC_D[15:0]	EMC_A[19:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC1774FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1774FBD144	EMC_D[7:0]	EMC_A[15:0]	EMC_CS[1:0], EMC_OE, EMC_WE	not available

- Physical interface:
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

7.15 USB interface

Remark: The USB Device/Host/OTG controller is available on parts LPC1788/87/86/85 and LPC1778/77/76. The USB Device-only controller is available on parts LPC1774.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

Details on typical USB interfacing solutions can be found in Section 14.1.

7.15.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the USB RAM.

7.15.1.1 Features

- Fully compliant with *USB 2.0 Specification* (full speed).
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the LPC178x/7x can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

7.15.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

7.15.2.1 Features

- OHCI compliant.

7.19.1 Features

- 10-bit DAC.
- Resistor string architecture.
- Buffered output.
- Power-down mode.
- Selectable output drive.
- Dedicated conversion timer.
- DMA support.

7.20 UARTs

Remark: USART4 is not available on part LPC1774FBD144.

The LPC178x/7x contain five UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.20.1 Features

- Maximum UART data bit rate of 7.5 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto-baud capability.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit/EIA-485 mode and multiprocessor addressing.
- All UARTs have DMA support for both transmit and receive.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- USART4 includes an IrDA mode to support infrared communication.
- USART4 supports synchronous mode and a smart card mode conforming to ISO7816-3.

7.21 SSP serial I/O controller

The LPC178x/7x contain three SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus

- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

7.25 General purpose 32-bit timers/external event counters

The LPC178x/7x include four 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.25.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

7.26 Pulse Width Modulator (PWM)

The LPC178x/7x contain two standard PWMs.

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC178x/7x. The Timer is designed to count cycles of the system derived clock and optionally switch pins, generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Backup registers (20 bytes) powered by VBAT.
- RTC power supply is isolated from the rest of the chip.

7.32 Event monitor/recorder

The event monitor/recorder allows recording of tampering events in sealed product enclosures. Sensors report any attempt to open the enclosure, or to tamper with the device in any other way. The event monitor/recorder stores records of such events when the device is powered only by the backup battery.

7.32.1 Features

- Supports three digital event inputs in the VBAT power domain.
- An event is defined as a level change at the digital event inputs.
- For each event channel, two timestamps mark the first and the last occurrence of an event. Each channel also has a dedicated counter tracking the total number of events. Timestamp values are taken from the RTC.
- Runs in VBAT power domain, independent of system power supply. The event/recorder/monitor can therefore operate in Deep power-down mode.
- Very low power consumption.
- Interrupt available if system is running.
- A qualified event can be used as a wake-up trigger.
- State of event interrupts accessible by software through GPIO.

7.33 Clocking and power control

7.33.1 Crystal oscillators

The LPC178x/7x include four independent oscillators. These are the main oscillator, the IRC oscillator, the watchdog oscillator, and the RTC oscillator.

Following reset, the LPC178x/7x will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the boot loader code to operate at a known frequency.

See Figure 7 for an overview of the LPC178x/7x clock generation.

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

The DMA controller can continue to work in Sleep mode and has access to the peripheral RAMs and all peripheral registers. The flash memory and the main SRAM are not available in Sleep mode, they are disabled in order to save power.

Wake-up from Sleep mode will occur whenever any enabled interrupt occurs.

7.33.4.2 Deep-sleep mode

In Deep-sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep-sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down to allow fast wake-up. The RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The clock divider registers are automatically reset to zero.

The Deep-sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Deep-sleep mode reduces chip power consumption to a very low value. Power to the flash memory is left on in Deep-sleep mode, allowing a very quick wake-up.

Wake-up from Deep-sleep mode can initiated by the NMI, External Interrupts $\overline{\text{EINT0}}$ through $\overline{\text{EINT3}}$, GPIO interrupts, the Ethernet Wake-on-LAN interrupt, Brownout Detect, an RTC Alarm interrupt, a USB input pin transition (USB activity interrupt), a CAN input pin transition, or a Watchdog Timer time-out, when the related interrupt is enabled. Wake-up will occur whenever any enabled interrupt occurs.

On wake-up from Deep-sleep mode, the code execution and peripherals activities will resume after four cycles expire if the IRC was used before entering Deep-sleep mode. If the main external oscillator was used, the code execution will resume when 4096 cycles expire. PLL and clock dividers need to be reconfigured accordingly.

7.33.4.3 Power-down mode

Power-down mode does everything that Deep-sleep mode does but also turns off the power to the IRC oscillator and the flash memory. This saves more power but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

When the chip enters Power-down mode, the IRC, the main oscillator, and all clocks are stopped. The RTC remains running if it has been enabled and RTC interrupts may be used to wake up the CPU. The flash is forced into Power-down mode. The PLLs are automatically turned off and the clock selection multiplexers are set to use the system clock sysclk (the reset state). The clock divider control registers are automatically reset to zero. If the Watchdog timer is running, it will continue running in Power-down mode.

10. Static characteristics

Table 13. Static characteristics

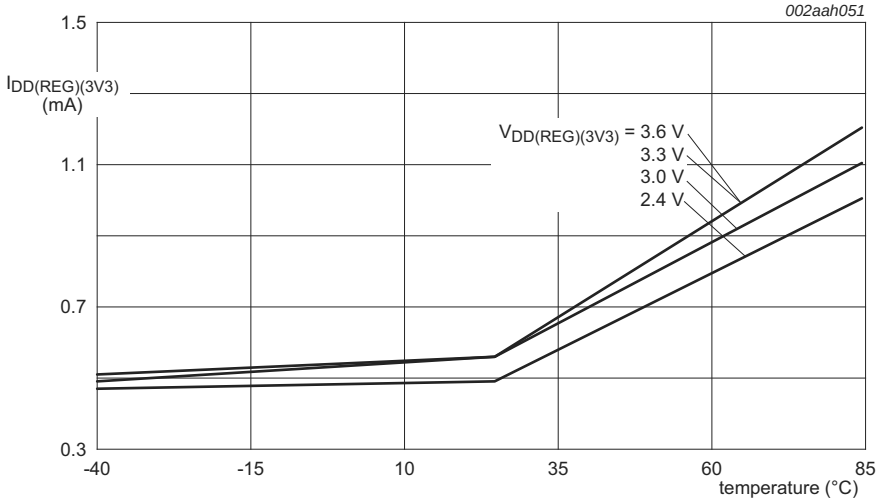
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	2.4	3.3	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			2.4	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[3]	2.7	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[4]	2.1	3.0	3.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[3]	2.7	3.3	V_{DDA}	V
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	active mode; code `while(1){}` executed from flash; all peripherals disabled PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]	-	7	-	mA
		CCLK = 120 MHz; PLL enabled	[5][7]	-	51	-	mA
		active mode; code `while(1){}` executed from flash; all peripherals enabled; PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]		14		
		CCLK = 120 MHz; PLL enabled	[5][7]		100		mA
		Sleep mode	[5][8]	-	5	-	mA
		Deep-sleep mode	[5][9]	-	550	-	µA
		Power-down mode	[5][9]	-	280	-	µA
I_{BAT}	battery supply current	RTC running; part powered down; $V_{DD(REG)(3V3)}$ =0 V; $V_{i(VBAT)}$ = 3.0 V; $V_{DD(3V3)}$ = 0 V.	[10]	-	1	-	µA
		part powered; $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{i(VBAT)}$ = 3.0 V	[11]		<10		nA

Table 13. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

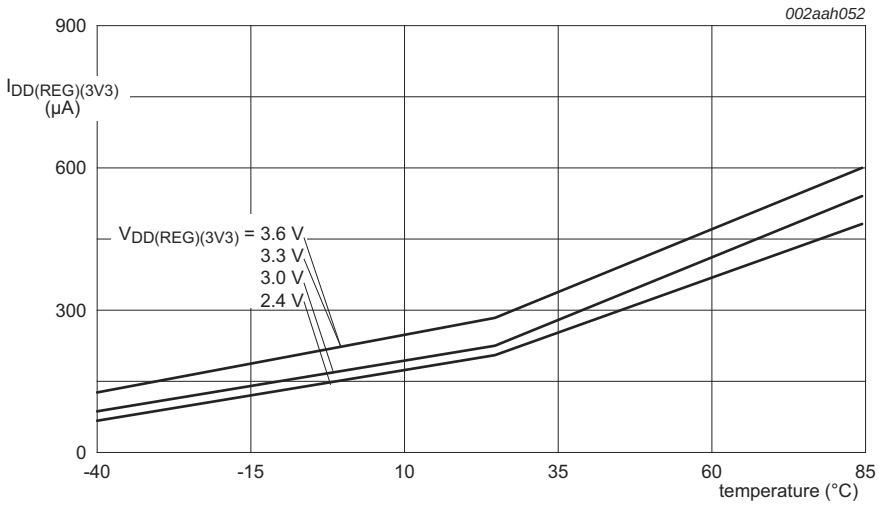
Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[15][16][17]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[18]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[18]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	µA
		$V_{DD(3V3)} < V_I < 5$ V		0	0	0	µA
I^2C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05 \times V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[19]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[20]	-	-	±10	µA
V_{BUS}	bus supply voltage		[20]	-	-	5.25	V

10.1 Power consumption



Conditions: BOD disabled.

Fig 9. Deep-sleep mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ versus temperature



Conditions: BOD disabled.

Fig 10. Power-down mode: Typical regulator supply current $I_{DD(REG)(3V3)}$ versus temperature

11. Dynamic characteristics

11.1 Flash memory

Table 15. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance	-	[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time	-	[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 16. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(REG)(3V3)}$ = 2.7 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency	-		200	375	400	kHz
N_{endu}	endurance	-		100000	500000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	64 bytes	[1]	-	1.8	-	ms
t_{prog}	programming time	64 bytes	[1]	-	1.1	-	ms

[1] EEPROM clock frequency = 375 kHz. Programming/erase times increase with decreasing EEPROM clock frequency.

Table 17. Dynamic characteristics: Static external memory interface *…continued*

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
t_{deact}	deactivation time	WR_8; PB = 0; PB = 1	[3]	−2.7	−3.4	−4.7	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	WR_9; PB = 0	[3]	2.8 + $T_{cy(clk)}$ × (1 + WAITWEN)	3.7 + $T_{cy(clk)}$ × (1 + WAITWEN)	5.1 + $T_{cy(clk)}$ × (1 + WAITWEN)	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	WR_{10}; PB = 0	[3]	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 2.6	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 3.4	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 4.9	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	WR_{11}; PB = 0	[3][6]	2.6 + $T_{cy(clk)}$	3.3 + $T_{cy(clk)}$	4.4 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	WR12; PB = 0	[3]	2.7 + $T_{cy(clk)}$	3.6 + $T_{cy(clk)}$	4.8 + $T_{cy(clk)}$	ns

[1] Parameters are shown as RD_n or WD_n in Figure 16 as indicated in the Conditions column.

[2] Parameters specified for 40 % of $V_{DD(3V3)}$ for rising edges and 60 % of $V_{DD(3V3)}$ for falling edges.

[3] $T_{cy(clk)}$ = 1/EMC_CLK (see *LPC178x/7x User manual UM10470*).

[4] Latest of address valid, $\overline{EMC\_CSx}$ LOW, $\overline{EMC\_OE}$ LOW, $\overline{EMC\_BLSx}$ LOW (PB = 1).

[5] After End Of Read (EOR): Earliest of $\overline{EMC\_CSx}$ HIGH, $\overline{EMC\_OE}$ HIGH, $\overline{EMC\_BLSx}$ HIGH (PB = 1), address invalid.

[6] End Of Write (EOW): Earliest of address invalid, $\overline{EMC\_CSx}$ HIGH, $\overline{EMC\_BLSx}$ HIGH (PB = 1).

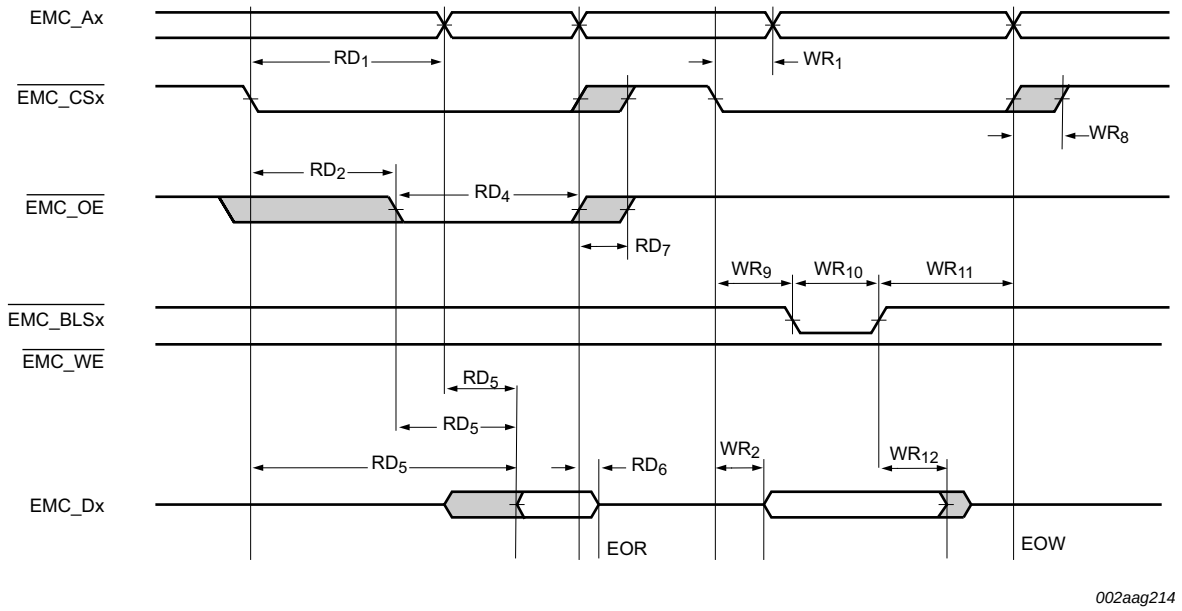
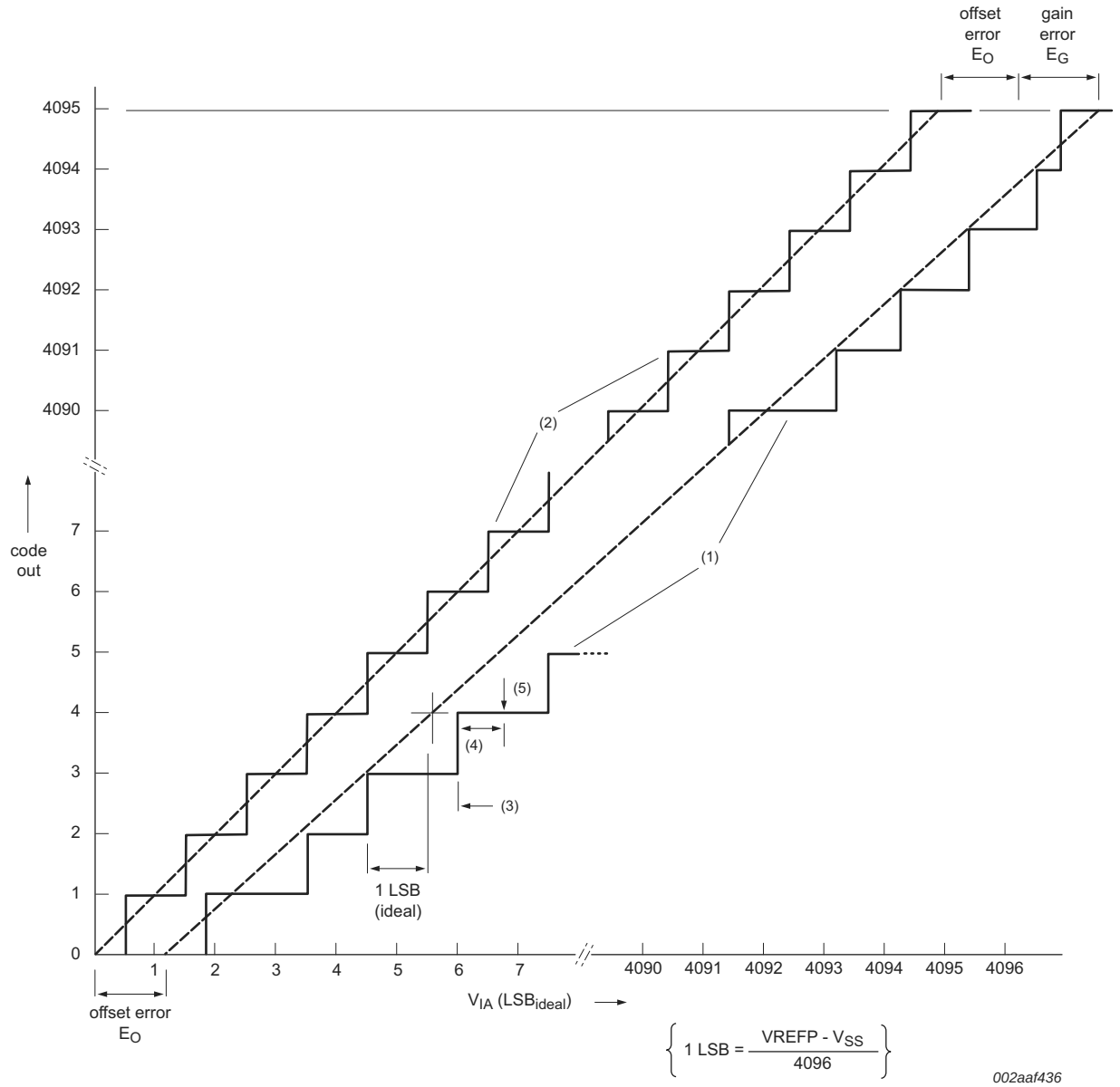


Fig 16. External static memory read/write access (PB = 0)



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 28. 12-bit ADC characteristics

To eliminate the loss of time counts in the RTC due to voltage swing or ramp rate of the $\overline{\text{RESET}}$ signal, connect an RC filter between the $\overline{\text{RESET}}$ pin and the external reset input.

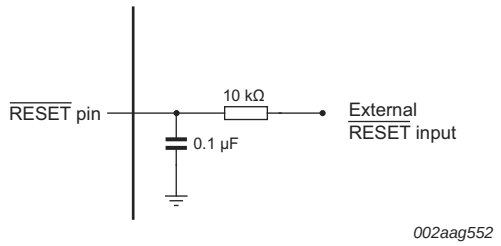


Fig 40. Reset input with RC filter

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continued >>