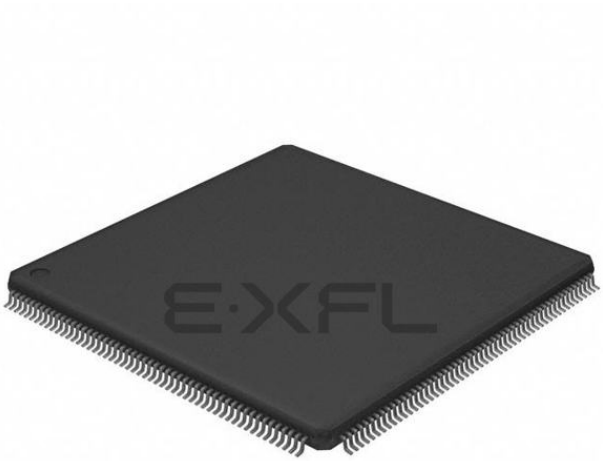

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	165
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1774fbd208-551

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[8]	160	A15	C12	111	[4]	I; IA	I/O	**P0[8] —** General purpose digital input/output pin.
							I/O	**I2S_TX_WS —** I^2S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
							I	**RTC_EV1 —** Event input 1 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[16] —** LCD data.
P0[9]	158	C14	A13	109	[4]	I; IA	I/O	**P0[9] —** General purpose digital input/output pin.
							I/O	**I2S_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
							I	**RTC_EV2 —** Event input 2 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[17] —** LCD data.
P0[10]	98	T15	L10	69	[3]	I; PU	I/O	**P0[10] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for UART2.
							I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P0[11]	100	R14	P12	70	[3]	I; PU	I/O	**P0[11] —** General purpose digital input/output pin.
							I	**U2_RXD —** Receiver input for UART2.
							I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT1 —** Match output for Timer 3, channel 1.
P0[12]	41	R1	J4	29	[5]	I; PU	I/O	**P0[12] —** General purpose digital input/output pin.
							O	**$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							I	**ADC0_IN[6] —** A/D converter 0, input 6. When configured as an ADC input, the digital function of the pin must be disabled.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[13]	45	R2	J5	32	[5]	I; PU	I/O	**P0[13] —** General purpose digital input/output pin.
							O	**USB_UP_LED2 —** USB port 2 GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							I	**ADC0_IN[7] —** A/D converter 0, input 7. When configured as an ADC input, the digital function of the pin must be disabled.
P0[14]	69	T7	M5	48	[3]	I; PU	I/O	**P0[14] —** General purpose digital input/output pin.
							O	**$\overline{\text{USB\_HSTEN2}}$ —** Host Enabled status for USB port 2.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							O	**USB_CONNECT2 —** SoftConnect control for USB port 2. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
P0[15]	128	J16	H13	89	[3]	I; PU	I/O	**P0[15] —** General purpose digital input/output pin.
							O	**U1_TXD —** Transmitter output for UART1.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
P0[16]	130	J14	H14	90	[3]	I; PU	I/O	**P0[16] —** General purpose digital input/output pin.
							I	**U1_RXD —** Receiver input for UART1.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
P0[17]	126	K17	J12	87	[3]	I; PU	I/O	**P0[17] —** General purpose digital input/output pin.
							I	**U1_CTS —** Clear to Send input for UART1.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
P0[18]	124	K15	J13	86	[3]	I; PU	I/O	**P0[18] —** General purpose digital input/output pin.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							I/O	**SSP0_MOSI —** Master Out Slave In for SSP0.
P0[19]	122	L17	J10	85	[3]	I; PU	I/O	**P0[19] —** General purpose digital input/output pin.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**SD_CLK —** Clock output line for SD card interface.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[21]	72	R8	N6	50	[3]	I; PU	I/O	**P1[21] —** General purpose digital input/output pin.
							O	**USB_TX_DM1 —** D− transmit data for USB port 1 (OTG transceiver).
							O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I	**$\overline{\text{MC\_ABORT}}$ —** Motor control PWM, active low fast abort.
							-	**R —** Function reserved.
							O	**LCD_VD[7] —** LCD data.
							O	**LCD_VD[11] —** LCD data.
P1[22]	74	U8	M6	51	[3]	I; PU	I/O	**P1[22] —** General purpose digital input/output pin.
							I	**USB_RCV1 —** Differential receive data for USB port 1 (OTG transceiver).
							I	**USB_PWRD1 —** Power Status for USB port 1 (host power switch).
							O	**T1_MAT0 —** Match output for Timer 1, channel 0.
							O	**MC_0B —** Motor control PWM channel 0, output B.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							O	**LCD_VD[8] —** LCD data.
							O	**LCD_VD[12] —** LCD data.
P1[23]	76	P9	N7	53	[3]	I; PU	I/O	**P1[23] —** General purpose digital input/output pin.
							I	**USB_RX_DP1 —** D+ receive data for USB port 1 (OTG transceiver).
							O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
							I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
							I	**MC_FB1 —** Motor control PWM channel 1 feedback input.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							O	**LCD_VD[9] —** LCD data.
							O	**LCD_VD[13] —** LCD data.
P1[24]	78	T9	P7	54	[3]	I; PU	I/O	**P1[24] —** General purpose digital input/output pin.
							I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).
							O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
							I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
							I	**MC_FB2 —** Motor control PWM channel 2 feedback input.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							O	**LCD_VD[10] —** LCD data.
							O	**LCD_VD[14] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P3[17]	143	F15	-	-	[3]	I; PU	I/O	**P3[17] —** General purpose digital input/output pin.
							I/O	**EMC_D[17] —** External memory data line 17.
							O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
							I	**U1_RXD —** Receiver input for UART1.
P3[18]	151	C15	-	-	[3]	I; PU	I/O	**P3[18] —** General purpose digital input/output pin.
							I/O	**EMC_D[18] —** External memory data line 18.
							O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
							I	**U1_CTS —** Clear to Send input for UART1.
P3[19]	161	B14	-	-	[3]	I; PU	I/O	**P3[19] —** General purpose digital input/output pin.
							I/O	**EMC_D[19] —** External memory data line 19.
							O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
P3[20]	167	A13	-	-	[3]	I; PU	I/O	**P3[20] —** General purpose digital input/output pin.
							I/O	**EMC_D[20] —** External memory data line 20.
							O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
							I	**U1_DSR —** Data Set Ready input for UART1.
P3[21]	175	C10	-	-	[3]	I; PU	I/O	**P3[21] —** General purpose digital input/output pin.
							I/O	**EMC_D[21] —** External memory data line 21.
							O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
P3[22]	195	C6	-	-	[3]	I; PU	I/O	**P3[22] —** General purpose digital input/output pin.
							I/O	**EMC_D[22] —** External memory data line 22.
							I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
							I	**U1_RI —** Ring Indicator input for UART1.
P3[23]	65	T6	M4	45	[3]	I; PU	I/O	**P3[23] —** General purpose digital input/output pin.
							I/O	**EMC_D[23] —** External memory data line 23.
							I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
							I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
P3[24]	58	R5	N3	40	[3]	I; PU	I/O	**P3[24] —** General purpose digital input/output pin.
							I/O	**EMC_D[24] —** External memory data line 24.
							O	**PWM1[1] —** Pulse Width Modulator 1, output 1.
							I	**T0_CAP1 —** Capture input for Timer 0, channel 1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P4[1]	79	U10	M7	55	[3]	I; PU	I/O	**P4[1] —** General purpose digital input/output pin.
							I/O	**EMC_A[1] —** External memory address line 1.
P4[2]	83	T11	M8	58	[3]	I; PU	I/O	**P4[2] —** General purpose digital input/output pin.
							I/O	**EMC_A[2] —** External memory address line 2.
P4[3]	97	U16	K9	68	[3]	I; PU	I/O	**P4[3] —** General purpose digital input/output pin.
							I/O	**EMC_A[3] —** External memory address line 3.
P4[4]	103	R15	P13	72	[3]	I; PU	I/O	**P4[4] —** General purpose digital input/output pin.
							I/O	**EMC_A[4] —** External memory address line 4.
P4[5]	107	R16	H10	74	[3]	I; PU	I/O	**P4[5] —** General purpose digital input/output pin.
							I/O	**EMC_A[5] —** External memory address line 5.
P4[6]	113	M14	K10	78	[3]	I; PU	I/O	**P4[6] —** General purpose digital input/output pin.
							I/O	**EMC_A[6] —** External memory address line 6.
P4[7]	121	L16	K12	84	[3]	I; PU	I/O	**P4[7] —** General purpose digital input/output pin.
							I/O	**EMC_A[7] —** External memory address line 7.
P4[8]	127	J17	J11	88	[3]	I; PU	I/O	**P4[8] —** General purpose digital input/output pin.
							I/O	**EMC_A[8] —** External memory address line 8.
P4[9]	131	H17	H12	91	[3]	I; PU	I/O	**P4[9] —** General purpose digital input/output pin.
							I/O	**EMC_A[9] —** External memory address line 9.
P4[10]	135	G17	G12	94	[3]	I; PU	I/O	**P4[10] —** General purpose digital input/output pin.
							I/O	**EMC_A[10] —** External memory address line 10.
P4[11]	145	F14	F11	101	[3]	I; PU	I/O	**P4[11] —** General purpose digital input/output pin.
							I/O	**EMC_A[11] —** External memory address line 11.
P4[12]	149	C16	F10	104	[3]	I; PU	I/O	**P4[12] —** General purpose digital input/output pin.
							I/O	**EMC_A[12] —** External memory address line 12.
P4[13]	155	B16	B14	108	[3]	I; PU	I/O	**P4[13] —** General purpose digital input/output pin.
							I/O	**EMC_A[13] —** External memory address line 13.
P4[14]	159	B15	E8	110	[3]	I; PU	I/O	**P4[14] —** General purpose digital input/output pin.
							I/O	**EMC_A[14] —** External memory address line 14.
P4[15]	173	A11	C10	120	[3]	I; PU	I/O	**P4[15] —** General purpose digital input/output pin.
							I/O	**EMC_A[15] —** External memory address line 15.
P4[16]	101	U17	N12	-	[3]	I; PU	I/O	**P4[16] —** General purpose digital input/output pin.
							I/O	**EMC_A[16] —** External memory address line 16.
P4[17]	104	P14	N13	-	[3]	I; PU	I/O	**P4[17] —** General purpose digital input/output pin.
							I/O	**EMC_A[17] —** External memory address line 17.
P4[18]	105	P15	P14	-	[3]	I; PU	I/O	**P4[18] —** General purpose digital input/output pin.
							I/O	**EMC_A[18] —** External memory address line 18.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P4[29]	176	B10	B9	122	[3]	I; PU	I/O	**P4[29] —** General purpose digital input/output pin.
							O	**EMC_BLS3 —** LOW active Byte Lane select signal 3.
							I	**U3_RXD —** Receiver input for UART3.
							O	**T2_MAT1 —** Match output for Timer 2, channel 1.
							I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
							O	**LCD_VD[7] —** LCD data.
							O	**LCD_VD[11] —** LCD data.
							O	**LCD_VD[3] —** LCD data.
P4[30]	187	B7	C7	130	[3]	I; PU	I/O	**P4[30] —** General purpose digital input/output pin.
							O	**EMC_CS0 —** LOW active Chip Select 0 signal.
P4[31]	193	A4	E7	134	[3]	I; PU	I/O	**P4[31] —** General purpose digital input/output pin.
							O	**EMC_CS1 —** LOW active Chip Select 1 signal.
P5[0] to P5[4]							I/O	**Port 5:** Port 5 is a 5-bit I/O port with individual direction controls for each bit. The operation of port 5 pins depends upon the pin function selected via the pin connect block.
P5[0]	9	F4	E5	6	[3]	I; PU	I/O	**P5[0] —** General purpose digital input/output pin.
							I/O	**EMC_A[24] —** External memory address line 24.
							I/O	**SSP2_MOSI —** Master Out Slave In for SSP2.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
P5[1]	30	J4	H1	21	[3]	I; PU	I/O	**P5[1] —** General purpose digital input/output pin.
							I/O	**EMC_A[25] —** External memory address line 25.
							I/O	**SSP2_MISO —** Master In Slave Out for SSP2.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
P5[2]	117	L14	L12	81	[11]	I	I/O	**P5[2] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output for Timer 3, channel 2.
							-	**R —** Function reserved.
							I/O	**I2C0_SDA —** I^2C0 data input/output (this pin uses a specialized I^2C pad that supports I^2C Fast Mode Plus).

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
VBAT	38	M3	K1	27		-	I	RTC power supply: 3.0 V on this pin supplies power to the RTC.
$V_{DD(REG)(3V3)}$	26, 86, 174	H4, P11, D11	G1, N9, E9	18, 60, 121		-	S	3.3 V regulator supply voltage: This is the power supply for the on-chip voltage regulator that supplies internal logic.
V_{DDA}	20	G4	F2	14		-	S	Analog 3.3 V pad supply voltage: This can be connected to the same supply as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC. **Note: This pin should be tied to 3.3 V if the ADC and DAC are not used.**
$V_{DD(3V3)}$	15, 60, 71, 89, 112, 125, 146, 165, 181, 198	G3, P6, P8, U13, P17, K16, C17, B13, C9, D7	E2, L4, K8, L11, J14, E12, E10, C5	41, 62, 77, 102, 114, 138		-	S	3.3 V supply voltage: This is the power supply voltage for I/O other than pins in the VBAT domain.
VREFP	24	K1	G2	17		-	S	ADC positive reference voltage: This should be the same voltage as V_{DDA}, but should be isolated to minimize noise and error. The voltage level on this pin is used as a reference for ADC and DAC. **Note: This pin should be tied to 3.3 V if the ADC and DAC are not used.**
V_{SS}	33, 63, 77, 93, 114, 133, 148, 169, 189, 200	L3, T5, R9, P12, N16, H14, E15, A12, B6, A2	H4, P4, L9, L13, G13, D13, C11, B4	44, 65, 79, 103, 117, 139		-	G	Ground: 0 V reference for digital IO pins.
V_{SSREG}	32, 84, 172	D12, K4, P10	H3, L8, A10	22, 59, 119		-	G	Ground: 0 V reference for internal logic.
V_{SSA}	22	J2	F3	15		-	G	Analog ground: 0 V power supply and reference for the ADC and DAC. This should be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
XTAL1	44	M4	L2	31	[14] [16]	-	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	46	N4	K4	33	[14] [16]	-	O	Output from the oscillator amplifier.

[1] PU = internal pull-up enabled (for $V_{DD(REG)(3V3)}$ = 3.3 V, pulled up to 3.3 V); IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] I = Input; O = Output; OL = Output driving LOW; G = Ground; S = Supply.

[3] 5 V tolerant pad (5 V tolerant if $V_{DD(3V3)}$ present; if $V_{DD(3V3)}$ not present, do not exceed 3.6 V) providing digital I/O functions with TTL levels and hysteresis.

[4] 5 V tolerant standard pad (5 V tolerant if $V_{DD(3V3)}$ present; if $V_{DD(3V3)}$ not present, do not exceed 3.6 V) providing digital I/O functions with TTL levels and hysteresis. This pad can be powered by VBAT.

[5] 5 V tolerant pad (5 V tolerant if $V_{DD(3V3)}$ present; if $V_{DD(3V3)}$ not present or configured for an analog function, do not exceed 3.6 V) providing digital I/O functions with TTL levels and hysteresis and analog input. When configured as a ADC input, digital section of the pad is disabled.

[6] 5 V tolerant fast pad (5 V tolerant if $V_{DD(3V3)}$ present; if $V_{DD(3V3)}$ not present, do not exceed 3.6 V) providing digital I/O functions with TTL levels and hysteresis.

[7] 5 V tolerant pad (5 V tolerant if $V_{DD(3V3)}$ present; if $V_{DD(3V3)}$ not present or configured for an analog function, do not exceed 3.6 V) providing digital I/O with TTL levels and hysteresis and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[8] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 400 kHz specification. It requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[9] Not 5 V tolerant. Pad provides digital I/O and USB functions. It is designed in accordance with the *USB specification, revision 2.0* (Full-speed and Low-speed mode only).

[10] 5 V tolerant pad (5 V tolerant if $V_{DD(3V3)}$ present; if $V_{DD(3V3)}$ not present, do not exceed 3.6 V) with 5 ns glitch filter providing digital I/O functions with TTL levels and hysteresis.

[11] Open-drain 5 V tolerant digital I/O pad, compatible with I^2C-bus 1 MHz specification. It requires an external pull-up to provide output functionality. When power is switched off, this pin connected to the I^2C-bus is floating and does not disturb the I^2C lines. Open-drain configuration applies to all functions on this pin.

[12] 5 V tolerant pad (5 V tolerant if $V_{DD(3V3)}$ present; if $V_{DD(3V3)}$ not present, do not exceed 3.6 V) with 20 ns glitch filter providing digital I/O function with TTL levels and hysteresis.

[13] This pad can be powered from VBAT.

[14] Pad provides special analog functionality. A 32 kHz crystal oscillator must be used with the RTC. An external clock (32 kHz) can't be used to drive the RTCX1 pin.

[15] If the RTC is not used, these pins can be left floating.

[16] When the main oscillator is not used, connect XTAL1 and XTAL2 as follows: XTAL1 can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTAL2 should be left floating.

Table 4. Pin allocation table TFBGA208

Not all functions are available on all parts. See Table 2 and Table 7 (EMC pins).

Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol
Row A							
1	P3[27]	2	V_{SS}	3	P1[0]	4	P4[31]
5	P1[4]	6	P1[9]	7	P1[14]	8	P1[15]
9	P1[17]	10	P1[3]	11	P4[15]	12	V_{SS}
13	P3[20]	14	P1[11]	15	P0[8]	16	P1[12]
17	P1[5]		-		-		-
Row B							
1	P3[2]	2	P3[10]	3	P3[1]	4	P3[0]
5	P1[1]	6	V_{SS}	7	P4[30]	8	P4[24]
9	P4[25]	10	P4[29]	11	P1[6]	12	P0[4]
13	$V_{DD(3V3)}$	14	P3[19]	15	P4[14]	16	P4[13]
17	P2[0]		-		-		-
Row C							

Table 5. Pin allocation table TFBGA180

Not all functions are available on all parts. See Table 2 and Table 7 (EMC pins).

Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol
13	P2[6]	14	P4[27]		-		-
Row G							
1	$V_{DD(REG)(3V3)}$	2	VREFP	3	P3[7]	4	P3[15]
5	P3[3]	6	-	7	-	8	-
9	-	10	P5[3]	11	P2[7]	12	P4[10]
13	V_{SS}	14	P2[8]		-		-
Row H							
1	P5[1]	2	$\overline{\text{RSTOUT}}$	3	V_{SSREG}	4	V_{SS}
5	RTC_ALARM	6	-	7	-	8	-
9	-	10	P4[5]	11	P2[9]	12	P4[9]
13	P0[15]	14	P0[16]		-		-

Table 7. External memory controller pin configuration

Part	Data bus pins	Address bus pins	Control pins	
			SRAM	SDRAM
LPC1788FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1788FET208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1788FET180	EMC_D[15:0]	EMC_A[19:0]	EMC_BLS[1:0], EMC_CS[1:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC1788FBD144	EMC_D[7:0]	EMC_A[15:0]	EMC_BLS[3:2], EMC_CS[1:0], EMC_OE, EMC_WE	not available
LPC1787FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS_[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1786FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1785FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1778FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1778FET208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1778FET180	EMC_D[15:0]	EMC_A[19:0]	EMC_BLS[1:0], EMC_CS[1:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC1778FBD144	EMC_D[7:0]	EMC_A[15:0]	EMC_CS[1:0], EMC_OE, EMC_WE	not available
LPC1777FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1776FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1776FET180	EMC_D[15:0]	EMC_A[19:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC1774FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1774FBD144	EMC_D[7:0]	EMC_A[15:0]	EMC_CS[1:0], EMC_OE, EMC_WE	not available

7.19.1 Features

- 10-bit DAC.
- Resistor string architecture.
- Buffered output.
- Power-down mode.
- Selectable output drive.
- Dedicated conversion timer.
- DMA support.

7.20 UARTs

Remark: USART4 is not available on part LPC1774FBD144.

The LPC178x/7x contain five UARTs. In addition to standard transmit and receive data lines, UART1 also provides a full modem control handshake interface and support for RS-485/9-bit mode allowing both software address detection and automatic address detection using 9-bit mode.

The UARTs include a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.20.1 Features

- Maximum UART data bit rate of 7.5 MBit/s.
- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Auto-baud capability.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit/EIA-485 mode and multiprocessor addressing.
- All UARTs have DMA support for both transmit and receive.
- UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).
- USART4 includes an IrDA mode to support infrared communication.
- USART4 supports synchronous mode and a smart card mode conforming to ISO7816-3.

7.21 SSP serial I/O controller

The LPC178x/7x contain three SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus

7.33.1.3 RTC oscillator

The RTC oscillator provides a 1 Hz clock to the RTC and a 32 kHz clock output that can be output on the CLKOUT pin in order to allow trimming the RTC oscillator without interference from a probe.

7.33.1.4 Watchdog oscillator

The Watchdog Timer has a dedicated watchdog oscillator that provides a 500 kHz clock to the Watchdog Timer. The watchdog oscillator is always running if the Watchdog Timer is enabled. The Watchdog oscillator clock can be output on the CLKOUT pin in order to allow observe its frequency.

In order to allow Watchdog Timer operation with minimum power consumption, which can be important in reduced power modes, the Watchdog oscillator frequency is not tightly controlled. The Watchdog oscillator frequency will vary over temperature and power supply within a particular part, and may vary by processing across different parts. This variation should be taken into account when determining Watchdog reload values.

Within a particular part, temperature and power supply variations can produce up to a ±17 % frequency variation. Frequency variation between devices under the same operating conditions can be up to ±30 %.

7.33.2 Main PLL (PLL0) and Alternate PLL (PLL1)

PLL0 (also called the Main PLL) and PLL1 (also called the Alternate PLL) are functionally identical but have somewhat different input possibilities and output connections. These possibilities are shown in Figure 7. The Main PLL can receive its input from either the IRC or the main oscillator and can potentially be used to provide the clocks to nearly everything on the device. The Alternate PLL receives its input only from the main oscillator and is intended to be used as an alternate source of clocking to the USB. The USB has timing needs that may not always be filled by the Main PLL.

Both PLLs are disabled and powered off on reset. If the Alternate PLL is left disabled, the USB clock can be supplied by PLL0 if everything is set up to provide 48 MHz to the USB clock through that route. The source for each clock must be selected via the CLKSEL registers and can be further reduced by clock dividers as needed.

PLL0 accepts an input clock frequency from either the IRC or the main oscillator. If only the Main PLL is used, then its output frequency must be an integer multiple of all other clocks needed in the system. PLL1 takes its input only from the main oscillator, requiring an external crystal in the range of 10 to 25 MHz. In each PLL, the Current Controlled Oscillator (CCO) operates in the range of 156 MHz to 320 MHz, so there are additional dividers to bring the output down to the desired frequencies. The minimum output divider value is 2, insuring that the output of the PLLs have a 50 % duty cycle.

If the USB is used, the possibilities for the CPU clock and other clocks will be limited by the requirements that the frequency be precise and very low jitter, and that the PLL0 output must be a multiple of 48 MHz. Even multiples of 48 MHz that are within the operating range of the PLL are 192 MHz and 288 MHz. Also, only the main oscillator in conjunction with the PLL can meet the precision and jitter specifications for USB. It is due to these limitations that the Alternate PLL is provided.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.34.4 APB interface

The APB peripherals are split into two separate APB buses in order to distribute the bus bandwidth and thereby reducing stalls caused by contention between the CPU and the GPDMA controller.

7.34.5 AHB multilayer matrix

The LPC178x/7x use an AHB multilayer matrix. This matrix connects the instruction (I-code) and data (D-code) CPU buses of the ARM Cortex-M3 to the flash memory, the main (64 kB) SRAM, and the Boot ROM. The GPDMA can also access all of these memories. Additionally, the matrix connects the CPU system bus and all of the DMA controllers to the various peripheral functions.

7.34.6 External interrupt inputs

The LPC178x/7x include up to 30 edge sensitive interrupt inputs combined with one level sensitive external interrupt input as selectable pin function. The external interrupt input can optionally be used to wake up the processor from Power-down mode.

7.34.7 Memory mapping control

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M3 address space. The vector table must be located on a 128 word (512 byte) boundary because the NVIC on the LPC178x/7x is configured for 128 total interrupts.

7.35 Debug control

Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to eight breakpoints and four watch points.

Table 14. Power consumption for individual analog and digital blocks *…continued*
T_{amb} = 25 °C; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 3.3 V; PCLK = CCLK/4.

Peripheral	Conditions	Typical supply current in mA		
		12 MHz[1]	48 MHz[1]	120 MHz[2]
EMC	-	0.82	3.17	7.63
RTC	-	0.01	0.01	0.05
USB + PLL1	-	0.62	0.97	1.67
Ethernet	PCENET bit set to 1 in the PCONP register	0.54	2.08	5.03

[1] Boost control bits in the PBOOST register set to 0x0 (see *LPC178x/7x User manual UM10470*).

[2] Boost control bits in the PBOOST register set to 0x3 (see *LPC178x/7x User manual UM10470*).

14. Application information

14.1 Suggested USB interface solutions

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC1788/87/86/85 and LPC1778/77/76 and as device-only controller on parts LPC1774.

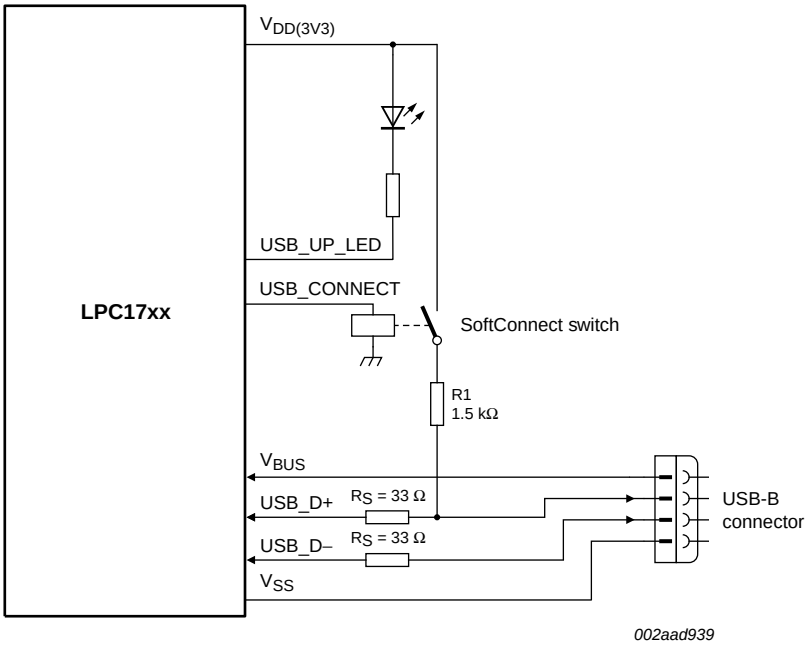


Fig 30. USB interface on a self-powered device

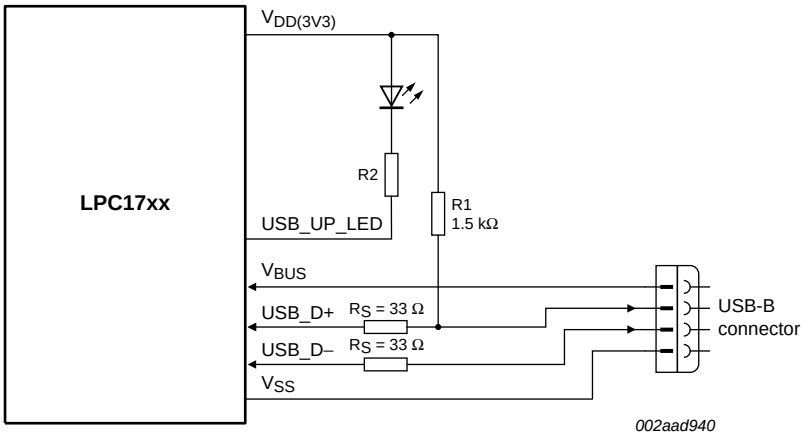


Fig 31. USB interface on a bus-powered device

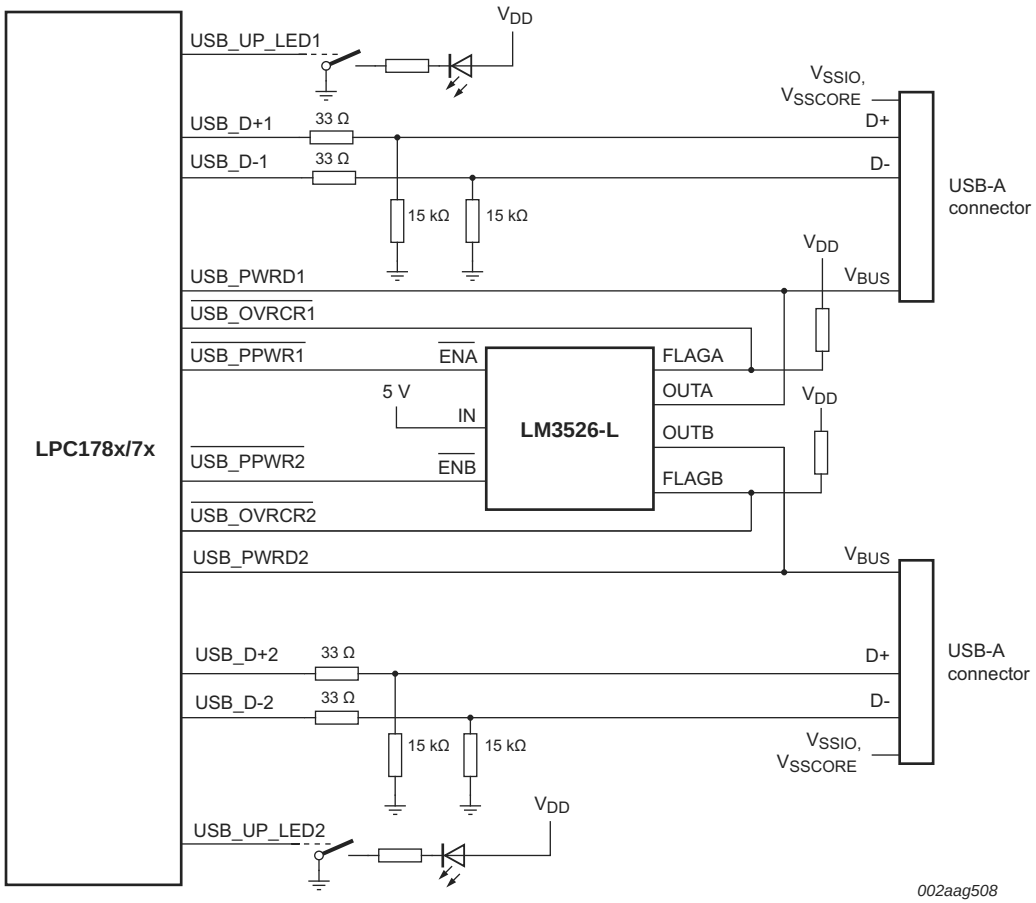


Fig 34. USB host port configuration: port 1 and port 2 as hosts

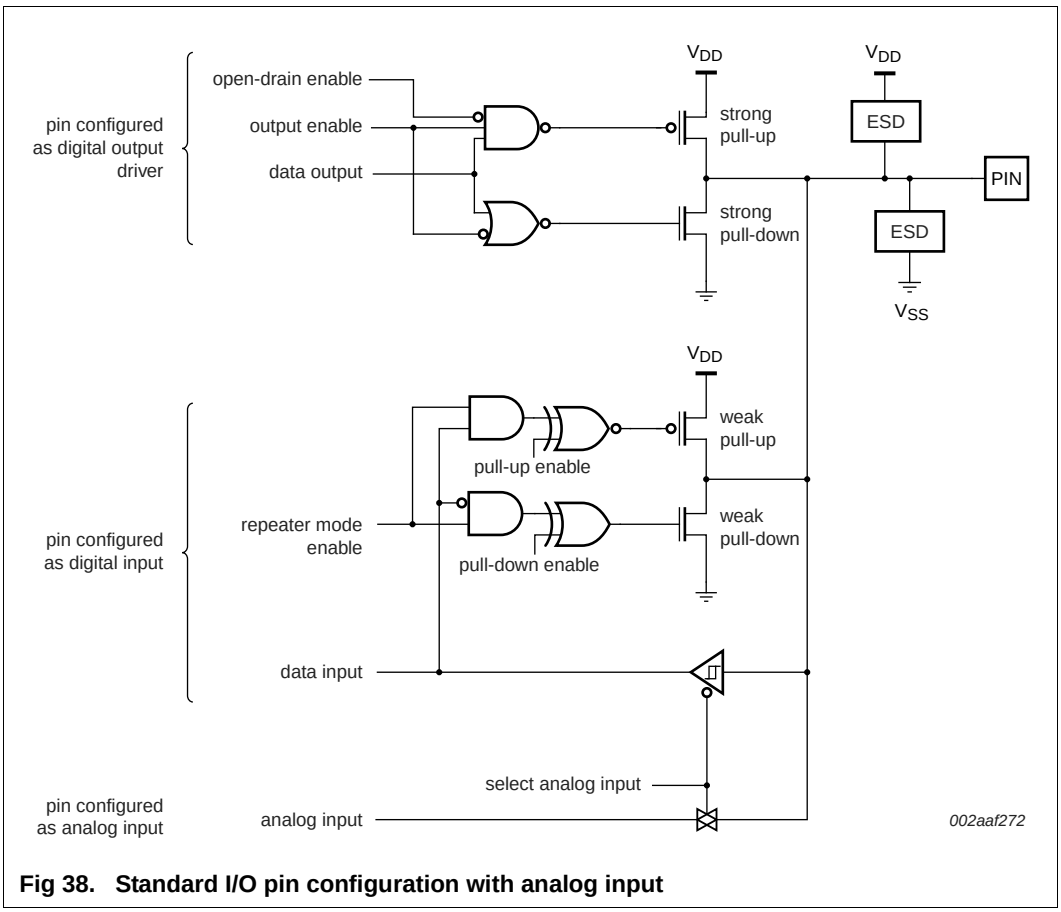


Fig 38. Standard I/O pin configuration with analog input

14.5 Reset pin configuration

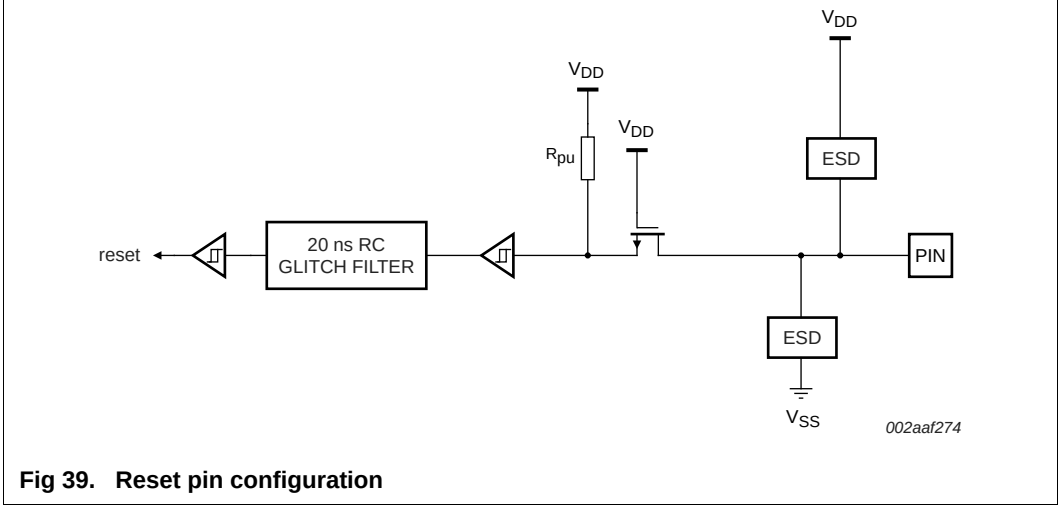
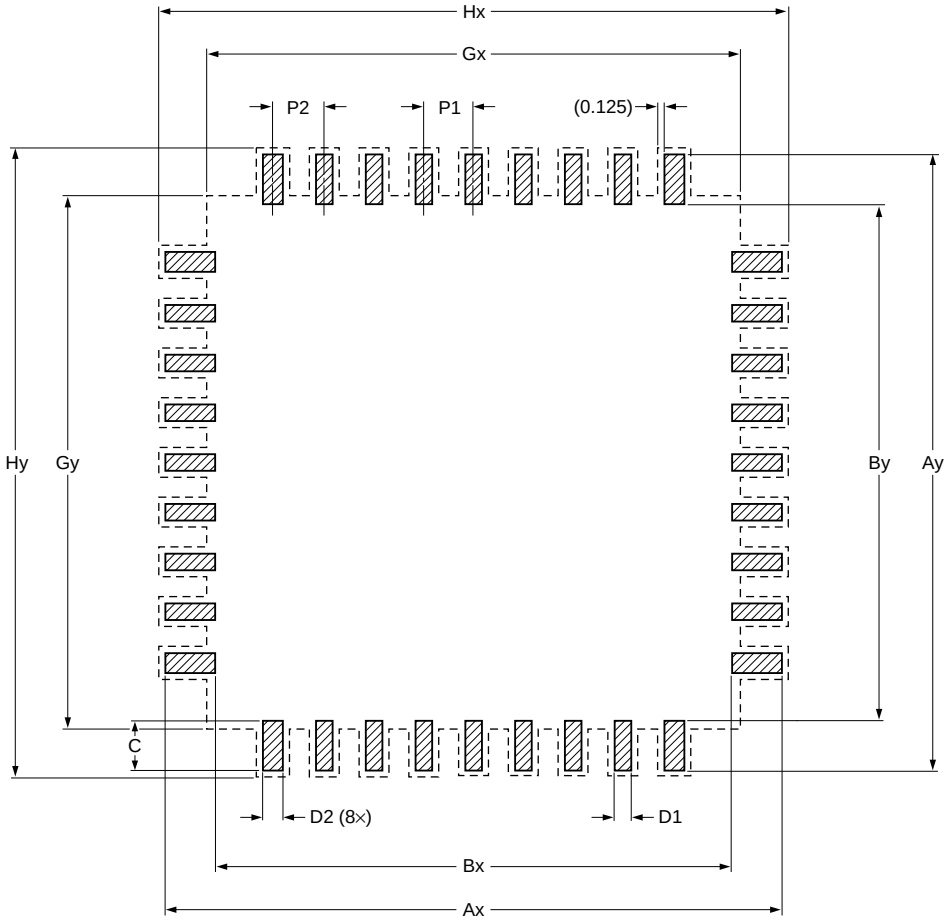


Fig 39. Reset pin configuration

14.6 Reset pin configuration for RTC operation

Under certain circumstances, the RTC may temporarily pause and lose fractions of a second during the rising and falling edges of the RESET signal.

Footprint information for reflow soldering of LQFP144 package **SOT486-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550

sot486-1_fr

Fig 47. Reflow soldering of the LQFP144 package

17. Abbreviations

Table 36. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
ETM	Embedded Trace Macrocell
GPIO	General Purpose Input/Output
GPS	Global Positioning System
HVAC	Heating, Venting, and Air Conditioning
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
MAC	Media Access Control
MIIM	Media Independent Interface Management
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLC	Programmable Logic Controller
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCM	Tightly Coupled Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

22. Contents

continued >>