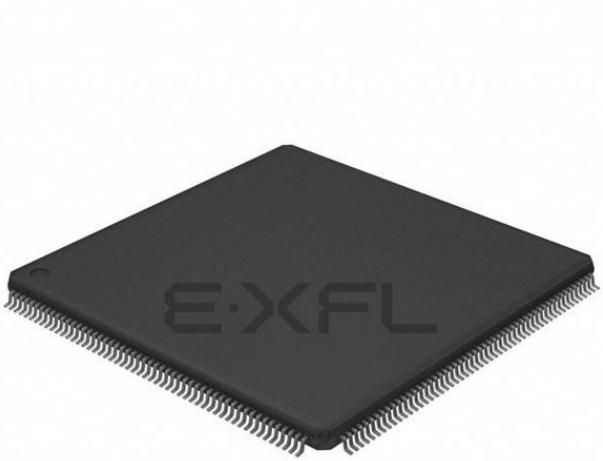

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	165
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1776fbd208-551

6. Pinning information

6.1 Pinning

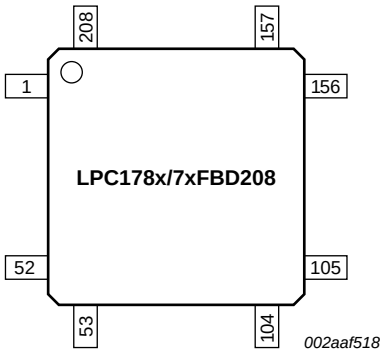


Fig 2. Pin configuration (LQFP208)

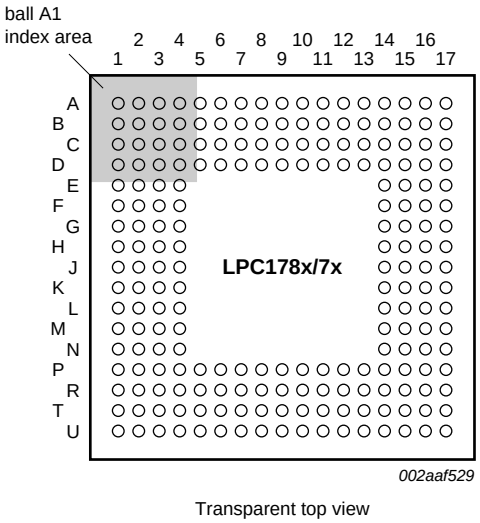


Fig 3. Pin configuration (TFBGA208)

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[8]	160	A15	C12	111	[4]	I; IA	I/O	**P0[8] —** General purpose digital input/output pin.
							I/O	**I2S_TX_WS —** I^2S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
							I	**RTC_EV1 —** Event input 1 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[16] —** LCD data.
P0[9]	158	C14	A13	109	[4]	I; IA	I/O	**P0[9] —** General purpose digital input/output pin.
							I/O	**I2S_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
							I	**RTC_EV2 —** Event input 2 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[17] —** LCD data.
P0[10]	98	T15	L10	69	[3]	I; PU	I/O	**P0[10] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for UART2.
							I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P0[11]	100	R14	P12	70	[3]	I; PU	I/O	**P0[11] —** General purpose digital input/output pin.
							I	**U2_RXD —** Receiver input for UART2.
							I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT1 —** Match output for Timer 3, channel 1.
P0[12]	41	R1	J4	29	[5]	I; PU	I/O	**P0[12] —** General purpose digital input/output pin.
							O	**$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							I	**ADC0_IN[6] —** A/D converter 0, input 6. When configured as an ADC input, the digital function of the pin must be disabled.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P2[1]	152	E14	C14	106	[3]	I; PU	I/O	**P2[1] —** General purpose digital input/output pin.
							O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
							I	**U1_RXD —** Receiver input for UART1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_LE —** Line end signal.
P2[2]	150	D15	E11	105	[3]	I; PU	I/O	**P2[2] —** General purpose digital input/output pin.
							O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
							-	**R —** Function reserved.
							O	**TRACEDATA[3] —** Trace data, bit 3.
							-	**R —** Function reserved.
							O	**LCD_DCLK —** LCD panel clock.
P2[3]	144	E16	E13	100	[3]	I; PU	I/O	**P2[3] —** General purpose digital input/output pin.
							O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
							-	**R —** Function reserved.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							-	**R —** Function reserved.
							O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
P2[4]	142	D17	E14	99	[3]	I; PU	I/O	**P2[4] —** General purpose digital input/output pin.
							O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**T2_MAT1 —** Match output for Timer 2, channel 1.
							-	**R —** Function reserved.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							-	**R —** Function reserved.
							O	**LCD_ENAB_M —** STN AC bias drive or TFT data enable output.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P5[3]	141	G14	G10	98	[11]	I	I/O	**P5[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**U4_RXD —** Receiver input for USART4.
							I/O	**I2C0_SCL —** I^2C0 clock input/output (this pin uses a specialized I^2C pad that supports I^2C Fast Mode Plus).
P5[4]	206	C3	C4	143	[3]	I; PU	I/O	**P5[4] —** General purpose digital input/output pin.
							O	**U0_OE —** RS-485/EIA-485 output enable signal for UART0.
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output for Timer 3, channel 3.
							O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
JTAG_TDO (SWO)	2	D3	B1	1	[3]	O	O	Test Data Out for JTAG interface. Also used as Serial wire trace output.
JTAG_TDI	4	C2	C3	3	[3]	I; PU	I	Test Data In for JTAG interface.
JTAG_TMS (SWDIO)	6	E3	C2	4	[3]	I; PU	I	Test Mode Select for JTAG interface. Also used as Serial wire debug data input/output.
JTAG_$\overline{\text{TRST}}$	8	D1	D4	5	[3]	I; PU	I	Test Reset for JTAG interface.
JTAG_TCK (SWDCLK)	10	E2	D2	7	[3]	i	I	Test Clock for JTAG interface. This clock must be slower than 1/6 of the CPU clock (CCLK) for the JTAG interface to operate. Also used as serial wire clock.
$\overline{\text{RESET}}$	35	M2	J1	24	[12]	I; PU	I	External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
$\overline{\text{RSTOUT}}$	29	K3	H2	20	[3]	OH	O	Reset status output. A LOW output on this pin indicates that the device is in the reset state for any reason. This reflects the $\overline{\text{RESET}}$ input pin and all internal reset sources.
RTC_ALARM	37	N1	H5	26	[13]	OL	O	RTC controlled output. This pin has a low drive strength and is powered by VBAT. It is driven HIGH when an RTC alarm is generated.
RTCX1	34	K2	J2	23	[14] [15]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	36	L2	J3	25	[14] [15]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
USB_D−2	52	U1	N2	37	[9]	-	I/O	USB port 2 bidirectional D− line.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the PWMMR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

7.26.1 Features

- LPC178x/7x has two PWM blocks with Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

7.27 Motor control PWM

The LPC178x/7x contain one motor control PWM.

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

The DMA controller can continue to work in Sleep mode and has access to the peripheral RAMs and all peripheral registers. The flash memory and the main SRAM are not available in Sleep mode, they are disabled in order to save power.

Wake-up from Sleep mode will occur whenever any enabled interrupt occurs.

7.33.4.2 Deep-sleep mode

In Deep-sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep-sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down to allow fast wake-up. The RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The clock divider registers are automatically reset to zero.

The Deep-sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Deep-sleep mode reduces chip power consumption to a very low value. Power to the flash memory is left on in Deep-sleep mode, allowing a very quick wake-up.

Wake-up from Deep-sleep mode can initiated by the NMI, External Interrupts $\overline{\text{EINT0}}$ through $\overline{\text{EINT3}}$, GPIO interrupts, the Ethernet Wake-on-LAN interrupt, Brownout Detect, an RTC Alarm interrupt, a USB input pin transition (USB activity interrupt), a CAN input pin transition, or a Watchdog Timer time-out, when the related interrupt is enabled. Wake-up will occur whenever any enabled interrupt occurs.

On wake-up from Deep-sleep mode, the code execution and peripherals activities will resume after four cycles expire if the IRC was used before entering Deep-sleep mode. If the main external oscillator was used, the code execution will resume when 4096 cycles expire. PLL and clock dividers need to be reconfigured accordingly.

7.33.4.3 Power-down mode

Power-down mode does everything that Deep-sleep mode does but also turns off the power to the IRC oscillator and the flash memory. This saves more power but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

When the chip enters Power-down mode, the IRC, the main oscillator, and all clocks are stopped. The RTC remains running if it has been enabled and RTC interrupts may be used to wake up the CPU. The flash is forced into Power-down mode. The PLLs are automatically turned off and the clock selection multiplexers are set to use the system clock sysclk (the reset state). The clock divider control registers are automatically reset to zero. If the Watchdog timer is running, it will continue running in Power-down mode.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this, four IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 12 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. Users need to reconfigure the PLL and clock dividers accordingly.

7.33.4.4 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

To optimize power conservation, the user has the additional option of turning off or retaining power to the 32 kHz oscillator. It is also possible to use external circuitry to turn off power to the on-chip regulator via the $V_{DD(REG)(3V3)}$ pins and/or the I/O power via the $V_{DD(3V3)}$ pins after entering Deep Power-down mode. Power must be restored before device operation can be restarted.

The LPC178x/7x can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

7.33.4.5 Wake-up Interrupt Controller (WIC)

The WIC allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep-sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC.This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

7.33.5 Peripheral power control

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

7.33.6 Power domains

The LPC178x/7x provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup registers.

On the LPC178x/7x, I/O pads are powered by $V_{DD(3V3)}$, while $V_{DD(REG)(3V3)}$ powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC178x/7x application, a design can use two power options to manage power consumption.

10.2 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the PCONP register. All other blocks are disabled and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. The peripheral clock was set to PCLK = CCLK/4 with CCLK = 12 MHz, 48 MHz, and 120 MHz.

The combined current of several peripherals running at the same time can be less than the sum of each individual peripheral current measured separately.

Table 14. Power consumption for individual analog and digital blocks

T_{amb} = 25 °C; $V_{DD(REG)(3V3)} = V_{DD(3V3)} = V_{DDA}$ = 3.3 V; PCLK = CCLK/4.

Peripheral	Conditions	Typical supply current in mA		
		12 MHz[1]	48 MHz[1]	120 MHz[2]
Timer0	-	0.01	0.06	0.15
Timer1	-	0.02	0.07	0.16
Timer2	-	0.02	0.07	0.17
Timer3	-	0.01	0.07	0.16
Timer0 + Timer1 + Timer2 + Timer3	-	0.07	0.28	0.67
UART0	-	0.05	0.19	0.45
UART1	-	0.06	0.24	0.56
UART2	-	0.05	0.2	0.47
UART3	-	0.06	0.23	0.56
USART4	-	0.07	0.27	0.66
UART0 + UART1 + UART2 + UART3 + USART4	-	0.29	1.13	2.74
PWM0 + PWM1	-	0.08	0.31	0.75
Motor control PWM	-	0.04	0.15	0.36
I2C0	-	0.01	0.03	0.08
I2C1	-	0.01	0.03	0.1
I2C2	-	0.01	0.03	0.08
I2C0 + I2C1 + I2C2	-	0.02	0.1	0.26
SSP0	-	0.03	0.1	0.26
SSP1	-	0.02	0.11	0.27
DAC	-	0.3	0.31	0.33
ADC (12 MHz clock)	-	1.51	1.61	1.7
CAN1	-	0.11	0.44	1.08
CAN2	-	0.1	0.4	0.98
CAN1 + CAN2	-	0.15	0.59	1.44
DMA	PCLK = CCLK	1.1	4.27	10.27
QEI	-	0.02	0.11	0.28
GPIO	-	0.4	1.72	4.16
LCD	-	0.99	3.84	9.25
I2S	-	0.04	0.18	0.46

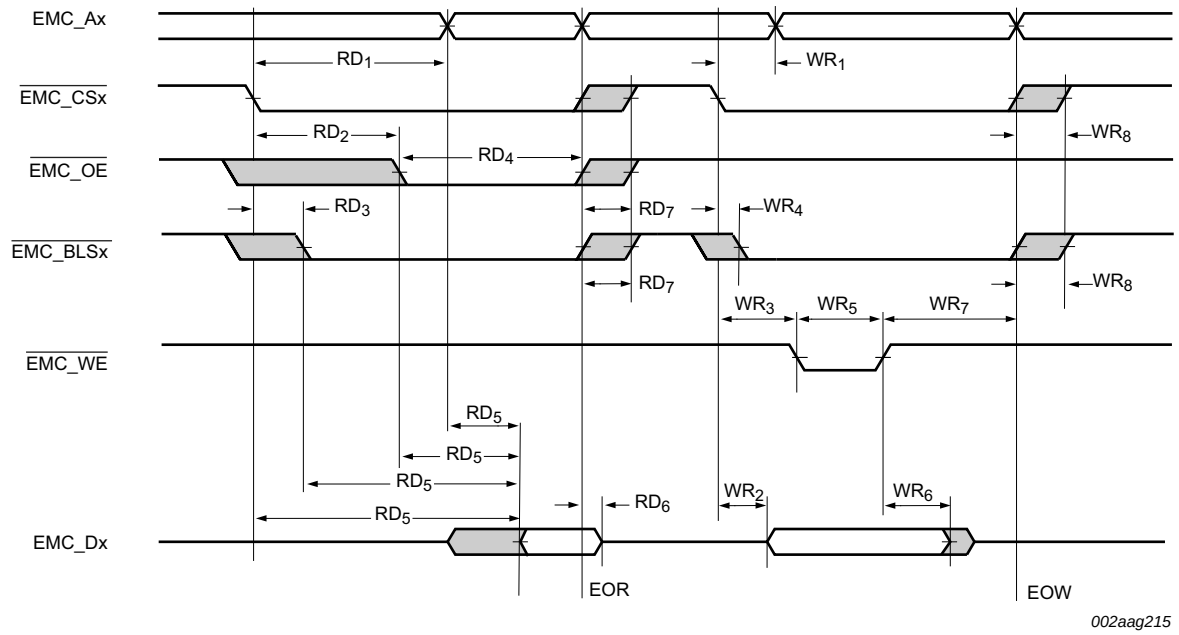


Fig 17. External static memory read/write access (PB =1)

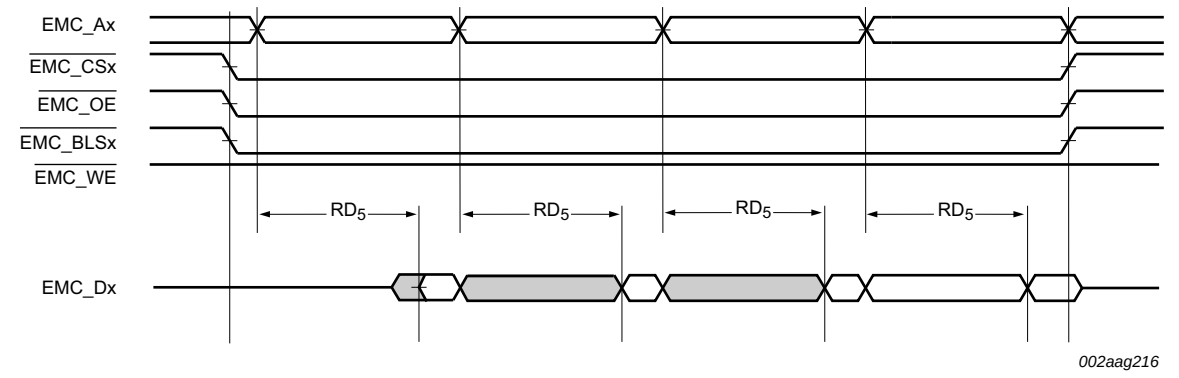


Fig 18. External static memory burst read cycle

Table 20. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1 $t_{clk0dly}$ = 0 and $t_{clk1dly}$ = 0						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	12.5	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	t_{cmddly} + 4.1	t_{cmddly} + 6.0	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 1.0	t_{cmddly} + 1.6	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		-	t_{cmddly} + 4.1	t_{cmddly} + 6.0	ns
$t_{h(RAS)}$	row address strobe hold time		t_{cmddly} + 1.1	t_{cmddly} + 1.7	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	t_{cmddly} + 4.1	t_{cmddly} + 6.1	ns
$t_{h(CAS)}$	column address strobe hold time		t_{cmddly} + 1.2	t_{cmddly} + 1.8	-	ns
$t_{d(WV)}$	write valid delay time		-	t_{cmddly} + 4.8	t_{cmddly} + 7.1	ns
$t_{h(W)}$	write hold time		t_{cmddly} + 1.6	t_{cmddly} + 2.3	-	ns
$t_{d(AV)}$	address valid delay time		-	t_{cmddly} + 4.9	t_{cmddly} + 7.3	ns
$t_{h(A)}$	address hold time		t_{cmddly} + 1.0	t_{cmddly} + 1.6	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		7.1 - t_{fbdly}	4.8 - t_{fbdly}	-	ns
$t_{h(D)}$	data input hold time		-1.9 + t_{fbdly}	-2.5 + t_{fbdly}	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	t_{cmddly} + 4.9	t_{cmddly} + 7.3	ns
$t_{h(Q)}$	data output hold time		t_{cmddly} + 0.2	t_{cmddly} + 0.5	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

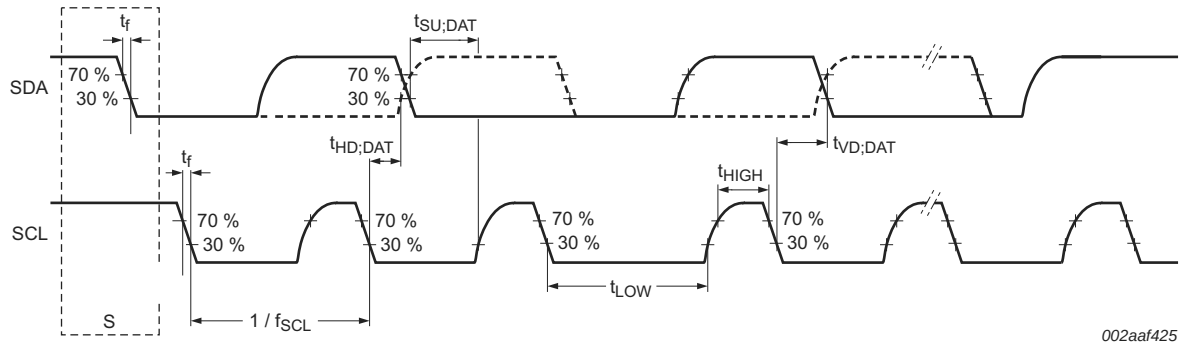


Fig 23. I²C-bus pins clock timing

11.8 I²S-bus interface

Table 28. Dynamic characteristics: I²S-bus interface pins

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
common to input and output						
t_r	rise time		[1]	-	6.7	ns
t_f	fall time		[1]	-	8.0	ns
t_{WH}	pulse width HIGH	on pins I2S_TX_SCK and I2S_RX_SCK	[1]	25	-	-
t_{WL}	pulse width LOW	on pins I2S_TX_SCK and I2S_RX_SCK	[1]	-	25	ns
output						
$t_{v(Q)}$	data output valid time	on pin I2S_TX_SDA;	[1]	-	6	ns
input						
$t_{su(D)}$	data input set-up time	on pin I2S_RX_SDA	[1]	5	-	ns
$t_{h(D)}$	data input hold time	on pin I2S_RX_SDA	[1]	2	-	ns

[1] CCLK = 100 MHz; peripheral clock to the I²S-bus interface PCLK = CCLK / 4. I²S clock cycle time $T_{cy(clk)}$ = 1600 ns, corresponds to the SCK signal in the *I²S-bus specification*.

12. ADC electrical characteristics

Table 31. 12-bit ADC characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
12-bit resolution							
E_D	differential linearity error		[2][3][4]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[2][5]	-	-	±6	LSB
E_O	offset error		[2][6]	-	-	±5	LSB
E_G	gain error		[2][7]	-	-	±5	LSB
E_T	absolute error		[2][8]	-	-	< ±8	LSB
$f_{clk(ADC)}$	ADC clock frequency			-	-	12.4	MHz
$f_{c(ADC)}$	ADC conversion frequency	single conversion mode		-	-	400	kSample/s
		burst mode		-	-	375	kSample/s
C_{ia}	analog input capacitance			-	-	5	pF
R_{vsi}	voltage source interface resistance		[9]	-	-	1	kΩ
8-bit resolution[10]							
E_D	differential linearity error		[2][3][4]	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		[2][5]	-	±1	-	LSB
E_O	offset error		[2][6]	-	±1	-	LSB
E_G	gain error		[2][7]	-	±1	-	LSB
E_T	absolute error		[2][8]	-	-	< ±1.5	LSB
$f_{clk(ADC)}$	ADC clock frequency			-	-	36	MHz
$f_{c(ADC)}$	ADC conversion frequency			-	-	1.16	Msample/s
C_{ia}	analog input capacitance			-	-	5	pF
R_{vsi}	voltage source interface resistance		[9]	-	-	1	kΩ

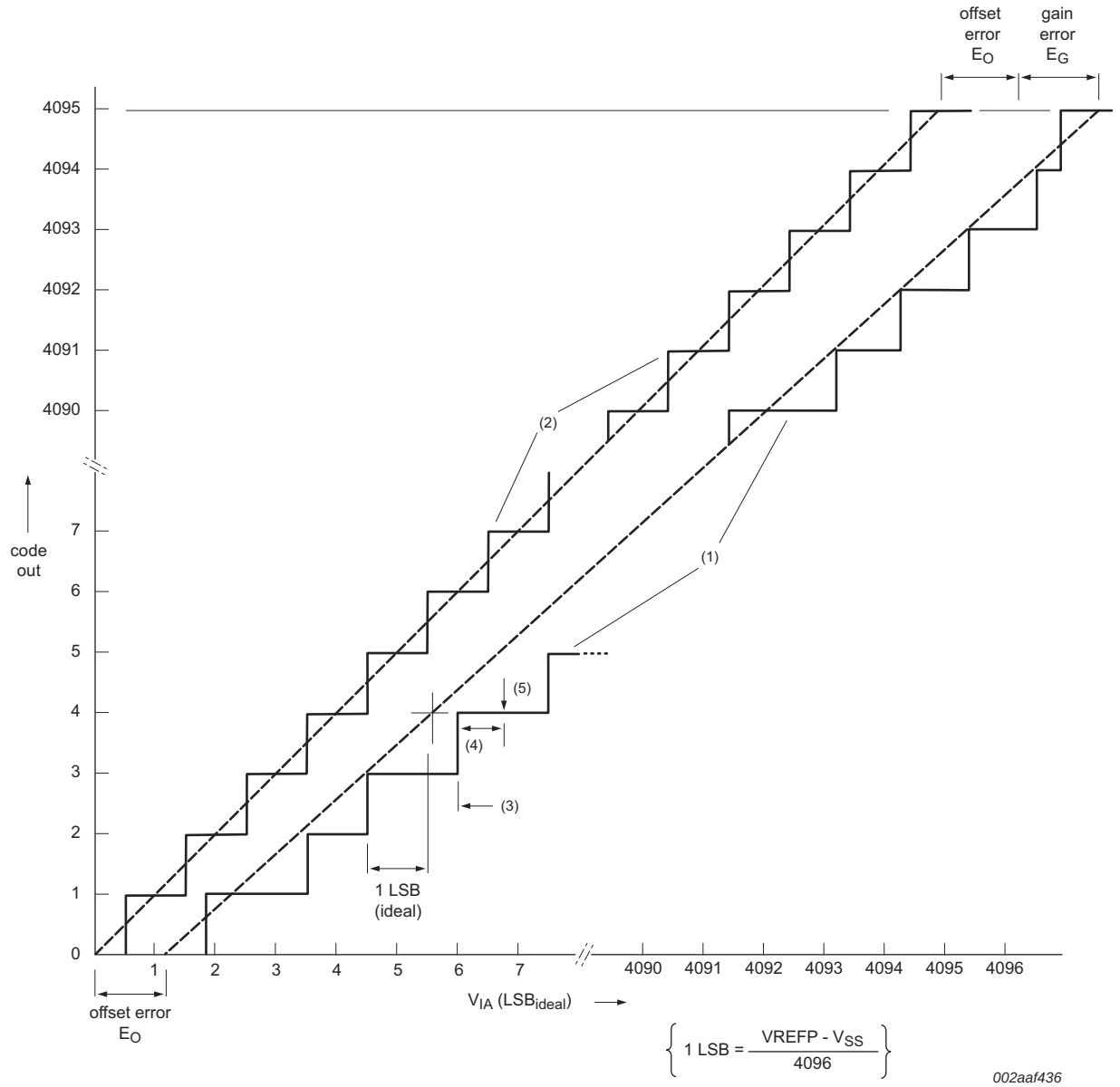
[1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[2] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[3] The ADC is monotonic, there are no missing codes.

[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 28.

[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 28.



(1) Example of an actual transfer curve.

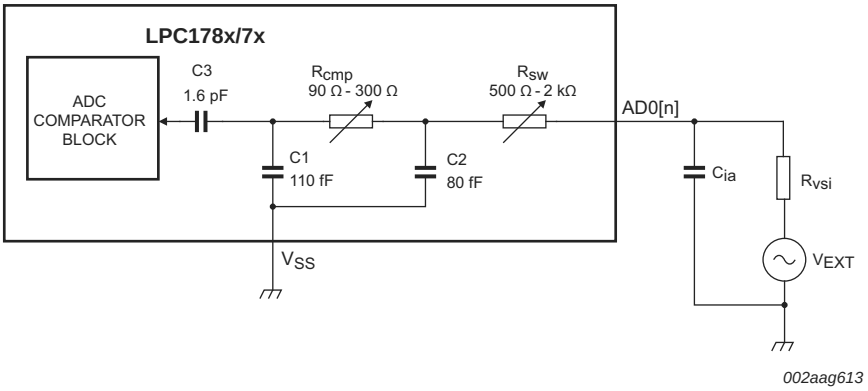
(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 28. 12-bit ADC characteristics



The values of resistor components R_{cmp} and R_{sw} vary with temperature and input voltage and are process-dependent.

Fig 29. ADC interface to pins ADC0_IN[n]

Table 32. ADC interface components

Component	Range	Description
R_{cmp}	90 Ω to 300 Ω	Switch-on resistance for the comparator input switch. Varies with temperature, input voltage, and process.
R_{sw}	500 Ω to 2 kΩ	Switch-on resistance for channel selection switch. Varies with temperature, input voltage, and process.
C1	110 fF	Parasitic capacitance from the ADC block level.
C2	80 fF	Parasitic capacitance from the ADC block level.
C3	1.6 pF	Sampling capacitor.

13. DAC electrical characteristics

Table 33. 10-bit DAC electrical characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
E_D	differential linearity error	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity	-	±1.5	-	LSB
E_O	offset error	-	0.6	-	%
E_G	gain error	-	0.6	-	%
C_L	load capacitance	-	-	200	pF
R_L	load resistance	1	-	-	kΩ

14. Application information

14.1 Suggested USB interface solutions

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC1788/87/86/85 and LPC1778/77/76 and as device-only controller on parts LPC1774.

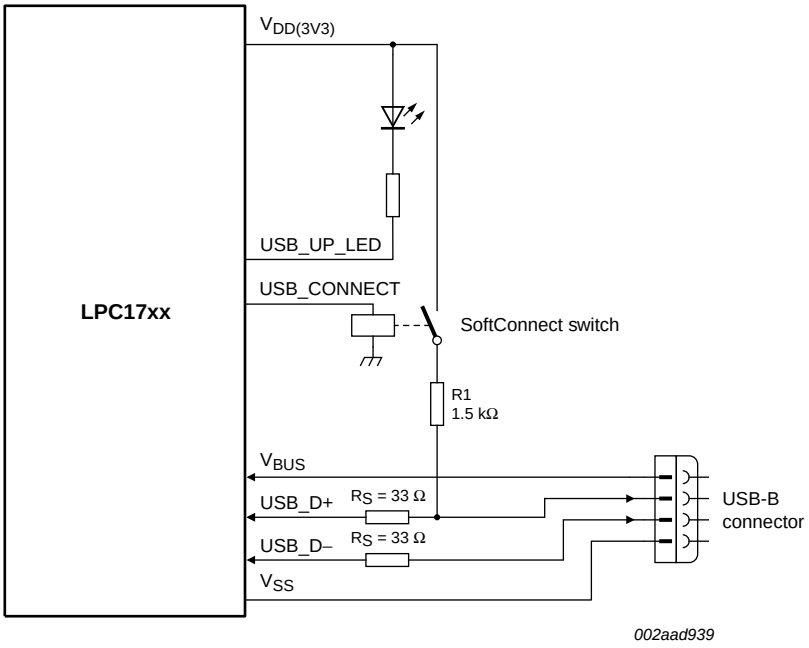


Fig 30. USB interface on a self-powered device

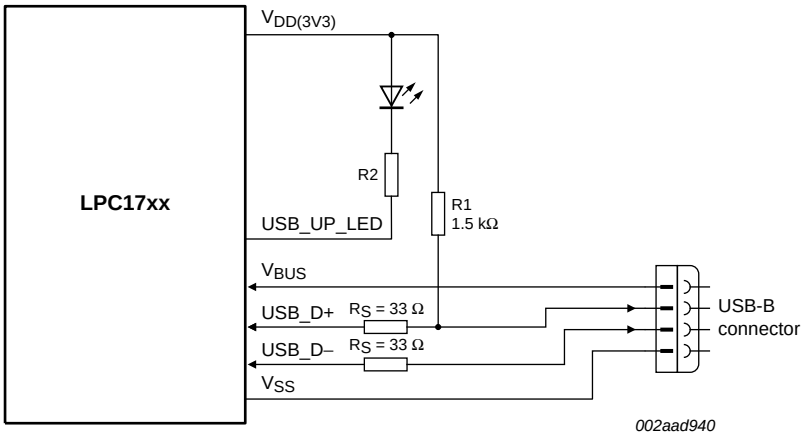


Fig 31. USB interface on a bus-powered device

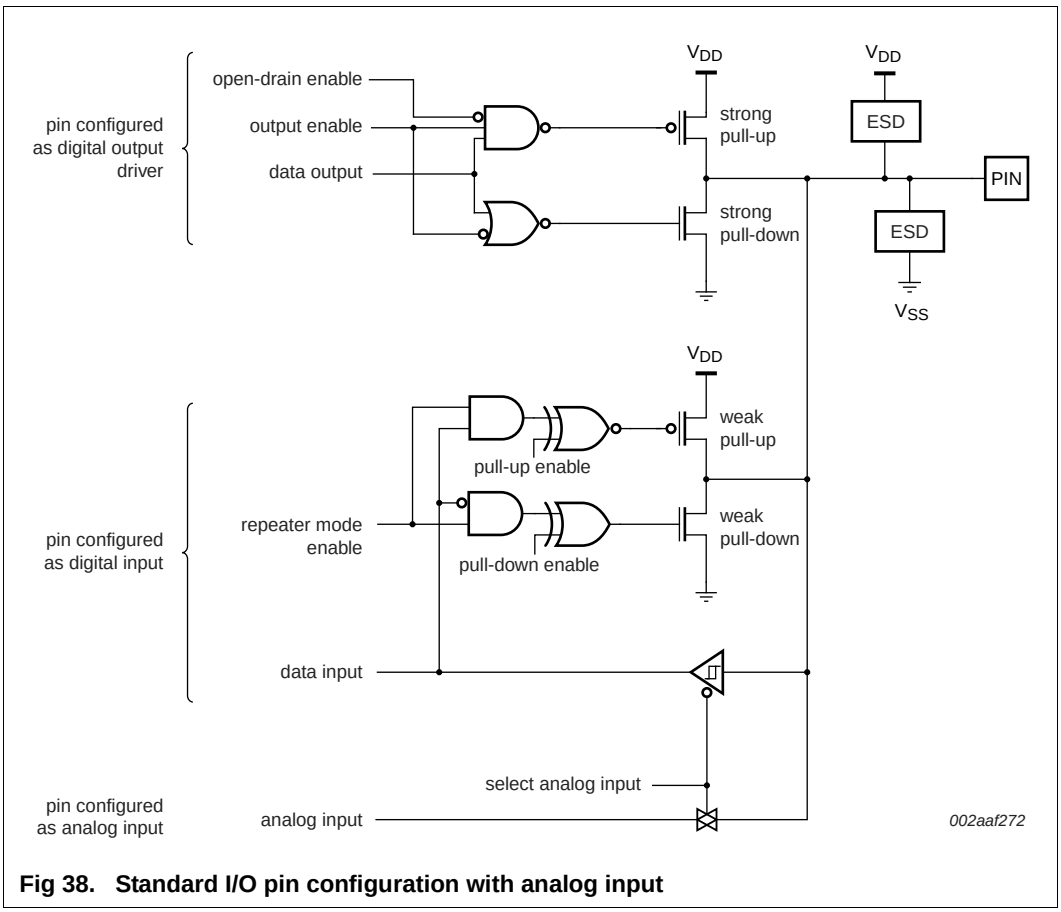


Fig 38. Standard I/O pin configuration with analog input

14.5 Reset pin configuration

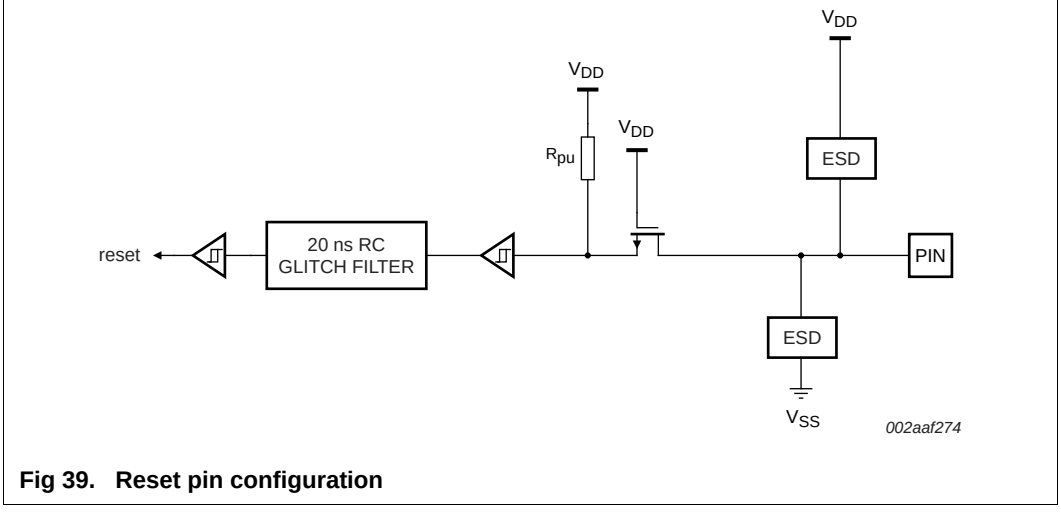
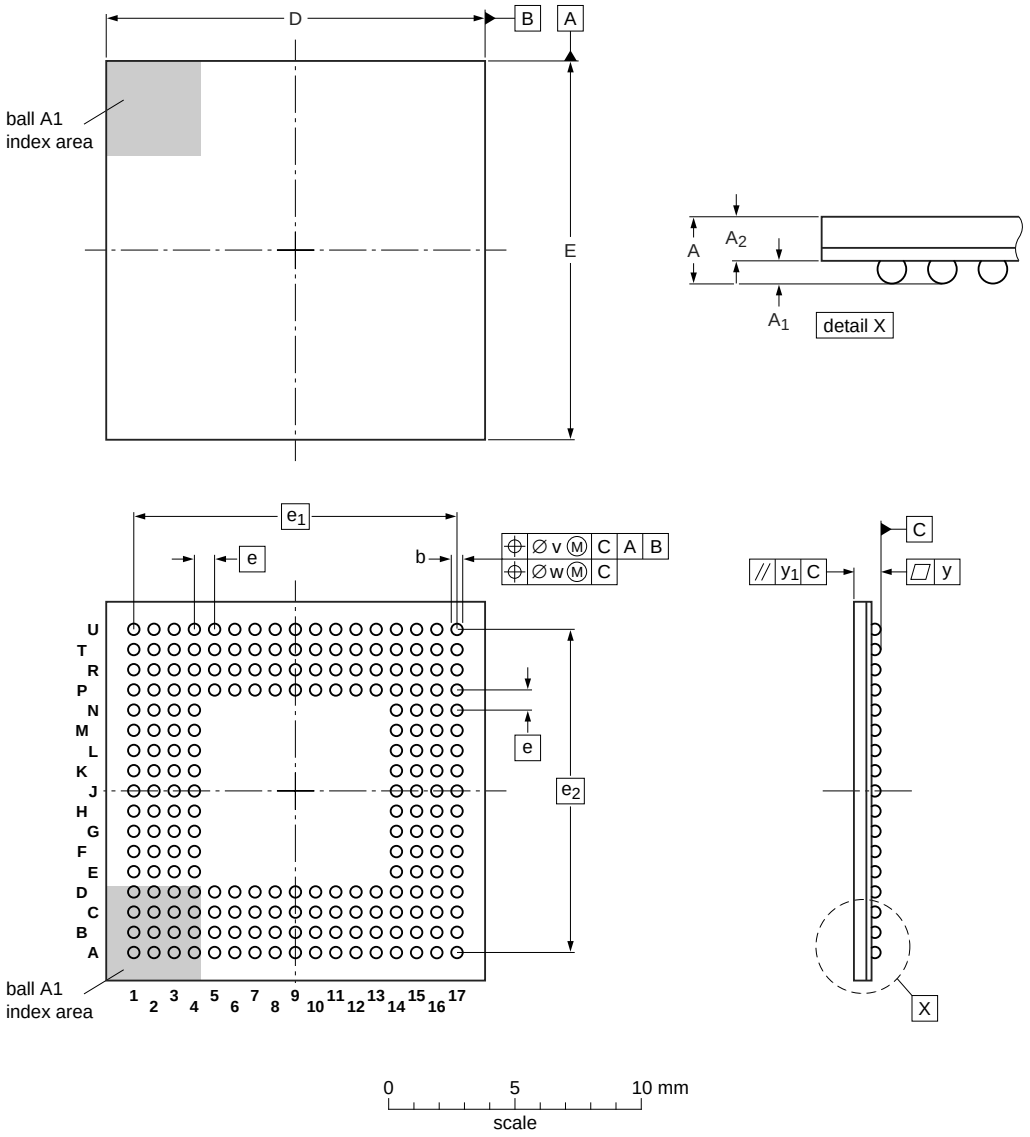


Fig 39. Reset pin configuration

14.6 Reset pin configuration for RTC operation

Under certain circumstances, the RTC may temporarily pause and lose fractions of a second during the rising and falling edges of the RESET signal.

TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 15 x 15 x 0.7 mm **SOT950-1**



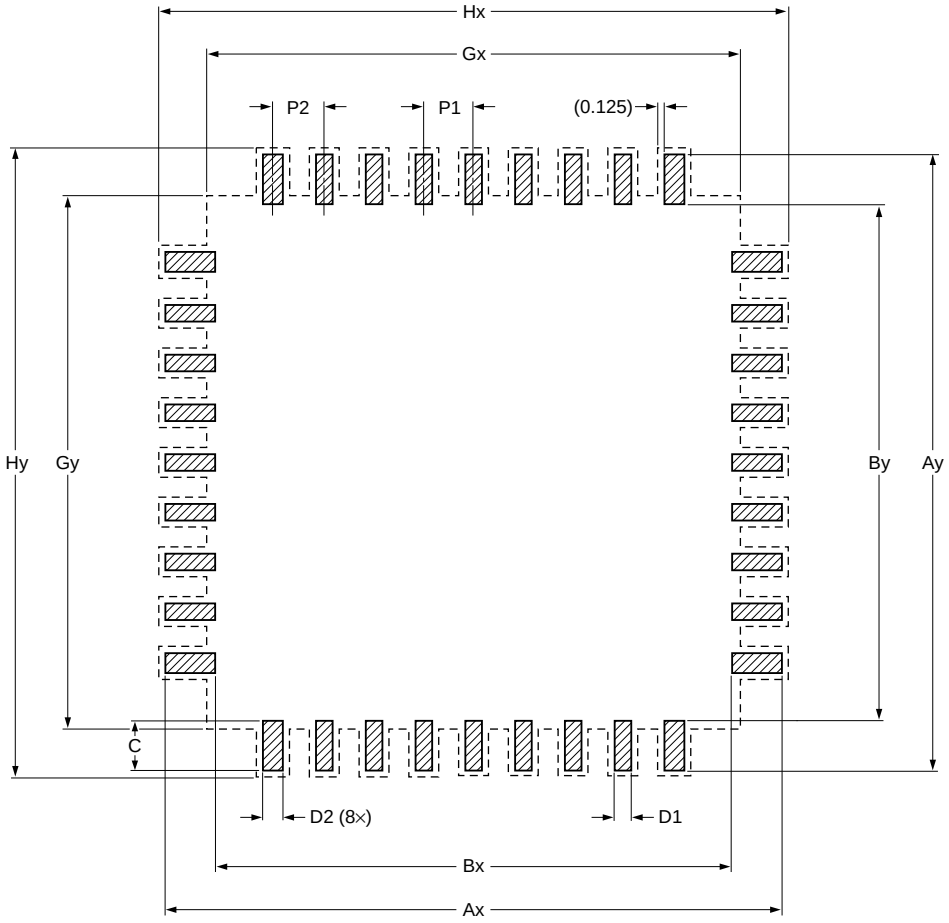
DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.6	0.5 0.4	15.1 14.9	15.1 14.9	0.8	12.8	12.8	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT950-1		- - -				~~06-06-01~~ 06-06-14

Fig 42. TFBGA208 package

Footprint information for reflow soldering of LQFP144 package **SOT486-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550

sot486-1_fr

Fig 47. Reflow soldering of the LQFP144 package

19. Revision history

Table 37. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC178X_7X v.5.5	20160426	Product data sheet	-	LPC178X_7X v.5.4
Modifications:	• Updated Table 29 “Dynamic characteristics: LCD”: $t_{d(QV)}$ max value is 9 ns for accuracy; was 12 ns.			
LPC178X_7X v.5.4	20160321	Product data sheet	CIN 201603016I	LPC178X_7X v.5.3
Modifications:	• Added Table 18 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00” for 10 pF load. • Updated Table 19 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00” for 30 pF load. • Added Table 20 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01” for 10 pF load. • Updated Table 21 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01” for 30 pF load. • Updated Table 22 “Dynamic characteristics: Dynamic external memory interface programmable clock delays (CMDDLY, FBCLKDLY, CLKOUT0DLY and CLKOUT1DLY)”. • Updated Figure 19 “Dynamic external memory interface signal timing”.			
LPC178X_7X v.5.3	20151015	Product data sheet	-	LPC178X_7X v.5.2
Modifications:	• Corrected max value of $t_{v(Q)}$ (data output valid time) in SPI mode to $3*T_{cy(PCLK)}$ + 6.3 ns. Was: $3*T_{cy(PCLK)}$ + 2.5 ns. See Table 26 “Dynamic characteristics: SSP pins in SPI mode”.			
LPC178X_7X v.5.2	20150814	Product data sheet	-	LPC178X_7X v.5.1
Modifications:	• Updated max value of $t_{v(Q)}$ (data output valid time) in SPI mode to $3*T_{cy(PCLK)}$ + 2.5 ns. See Table 24 “Dynamic characteristics: SSP pins in SPI mode”. • Added a column for GPIO pins and device order part number to the ordering options table. See Table 2 “LPC178x/7x ordering options”.			
LPC178X_7X v.5.1	20140501	Product data sheet	-	LPC178X_7X v.5
Modifications:	• Updated parameter $t_{su(D)}$ in Table 18 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00”: Minimum value changed to (FBCLKDLY + 1) × 0.25 + 0.3. Maximum value removed. • Removed max value from parameter $t_{h(D)}$ in Table 17. • Removed min value from parameter t_{deact} in Table 17. • Specified ADC conversion rate in burst mode in Table 29 “12-bit ADC characteristics”.			

22. Contents

continued >>