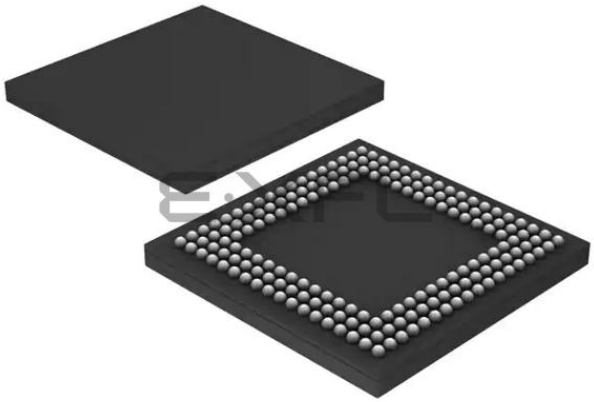

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	141
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1776fet180-551

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1788			
LPC1788FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1788FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 ´ 15 ´ 0.7 mm	SOT950-1
LPC1788FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1788FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1787			
LPC1787FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1786			
LPC1786FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1785			
LPC1785FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1778			
LPC1778FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1778FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 ´ 15 ´ 0.7 mm	SOT950-1
LPC1778FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1778FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1777			
LPC1777FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1776			
LPC1776FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1776FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1774			
LPC1774FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1774FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

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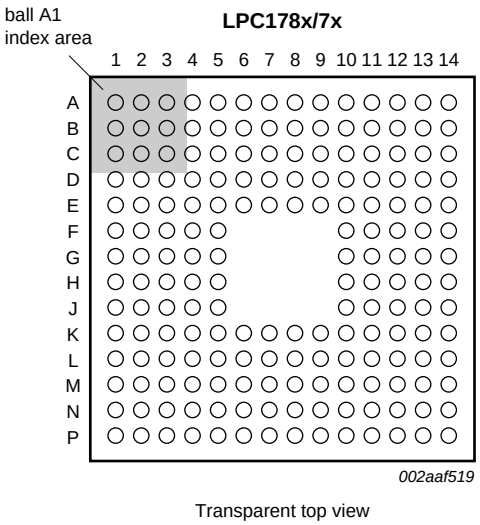

Fig 4. Pin configuration (TFBGA180)

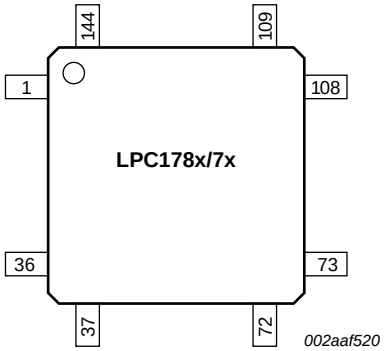

Fig 5. Pin configuration (LQFP144)

6.2 Pin description

I/O pins on the LPC178x/7x are 5 V tolerant and have input hysteresis unless otherwise indicated in the table below. Crystal pins, power pins, and reference voltage pins are not 5 V tolerant. In addition, when pins are selected to be ADC inputs, they are no longer 5 V tolerant and the input voltage must be limited to the voltage at the ADC positive reference pin (VREFP).

All port pins Pn[m] are multiplexed, and the multiplexed functions appear in Table 3 in the order defined by the FUNC bits of the corresponding IOCON register up to the highest used function number. Each port pin can support up to eight multiplexed functions. IOCON register FUNC values which are reserved are noted as ‘R’ in the pin configuration table.

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Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[8]	160	A15	C12	111	[4]	I; IA	I/O	**P0[8] —** General purpose digital input/output pin.
							I/O	**I2S_TX_WS —** I^2S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
							I	**RTC_EV1 —** Event input 1 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[16] —** LCD data.
P0[9]	158	C14	A13	109	[4]	I; IA	I/O	**P0[9] —** General purpose digital input/output pin.
							I/O	**I2S_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
							I	**RTC_EV2 —** Event input 2 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[17] —** LCD data.
P0[10]	98	T15	L10	69	[3]	I; PU	I/O	**P0[10] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for UART2.
							I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P0[11]	100	R14	P12	70	[3]	I; PU	I/O	**P0[11] —** General purpose digital input/output pin.
							I	**U2_RXD —** Receiver input for UART2.
							I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT1 —** Match output for Timer 3, channel 1.
P0[12]	41	R1	J4	29	[5]	I; PU	I/O	**P0[12] —** General purpose digital input/output pin.
							O	**$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							I	**ADC0_IN[6] —** A/D converter 0, input 6. When configured as an ADC input, the digital function of the pin must be disabled.

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Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P3[17]	143	F15	-	-	[3]	I; PU	I/O	**P3[17] —** General purpose digital input/output pin.
							I/O	**EMC_D[17] —** External memory data line 17.
							O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
							I	**U1_RXD —** Receiver input for UART1.
P3[18]	151	C15	-	-	[3]	I; PU	I/O	**P3[18] —** General purpose digital input/output pin.
							I/O	**EMC_D[18] —** External memory data line 18.
							O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
							I	**U1_CTS —** Clear to Send input for UART1.
P3[19]	161	B14	-	-	[3]	I; PU	I/O	**P3[19] —** General purpose digital input/output pin.
							I/O	**EMC_D[19] —** External memory data line 19.
							O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
P3[20]	167	A13	-	-	[3]	I; PU	I/O	**P3[20] —** General purpose digital input/output pin.
							I/O	**EMC_D[20] —** External memory data line 20.
							O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
							I	**U1_DSR —** Data Set Ready input for UART1.
P3[21]	175	C10	-	-	[3]	I; PU	I/O	**P3[21] —** General purpose digital input/output pin.
							I/O	**EMC_D[21] —** External memory data line 21.
							O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
P3[22]	195	C6	-	-	[3]	I; PU	I/O	**P3[22] —** General purpose digital input/output pin.
							I/O	**EMC_D[22] —** External memory data line 22.
							I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
							I	**U1_RI —** Ring Indicator input for UART1.
P3[23]	65	T6	M4	45	[3]	I; PU	I/O	**P3[23] —** General purpose digital input/output pin.
							I/O	**EMC_D[23] —** External memory data line 23.
							I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
							I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
P3[24]	58	R5	N3	40	[3]	I; PU	I/O	**P3[24] —** General purpose digital input/output pin.
							I/O	**EMC_D[24] —** External memory data line 24.
							O	**PWM1[1] —** Pulse Width Modulator 1, output 1.
							I	**T0_CAP1 —** Capture input for Timer 0, channel 1.

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Table 5. Pin allocation table TFBGA180

Not all functions are available on all parts. See Table 2 and Table 7 (EMC pins).

Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol
13	P2[6]	14	P4[27]		-		-
Row G							
1	$V_{DD(REG)(3V3)}$	2	VREFP	3	P3[7]	4	P3[15]
5	P3[3]	6	-	7	-	8	-
9	-	10	P5[3]	11	P2[7]	12	P4[10]
13	V_{SS}	14	P2[8]		-		-
Row H							
1	P5[1]	2	$\overline{\text{RSTOUT}}$	3	V_{SSREG}	4	V_{SS}
5	RTC_ALARM	6	-	7	-	8	-
9	-	10	P4[5]	11	P2[9]	12	P4[9]
13	P0[15]	14	P0[16]		-		-

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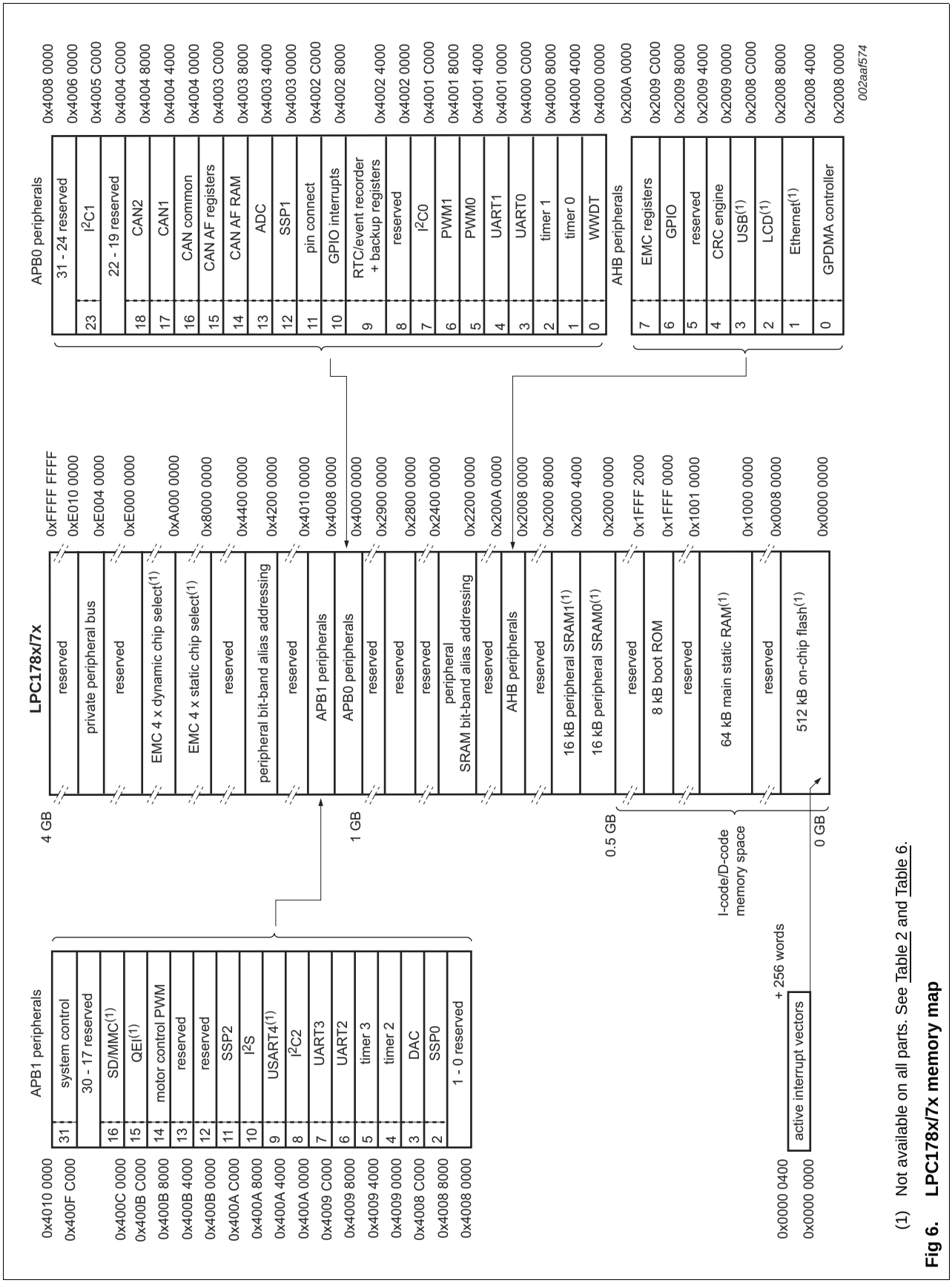

(1) Not available on all parts. See Table 2 and Table 6.

Fig 6. LPC178x/7x memory map

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- GPIO registers are accessed through the AHB multilayer bus so that the fastest possible I/O timing can be achieved.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte and half-word addressable.
- Entire port value can be written in one instruction.
- Support for Cortex-M3 bit banding.
- Support for use with the GPDMA controller.

Additionally, any pin on Port 0 and Port 2 providing a digital function can be programmed to generate an interrupt on a rising edge, a falling edge, or both. The edge detection is asynchronous, so it may operate when clocks are not present such as during Power-down mode. Each enabled interrupt can be used to wake up the chip from Power-down mode.

7.17.1 Features

- Bit level set and clear registers allow a single instruction to set or clear any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- Pull-up/pull-down resistor configuration and open-drain configuration can be programmed through the pin connect block for each GPIO pin.

7.18 12-bit ADC

The LPC178x/7x contain one ADC. It is a single 12-bit successive approximation ADC with eight channels and DMA support.

7.18.1 Features

- 12-bit successive approximation ADC.
- Input multiplexing among eight pins.
- Power-down mode.
- Measurement range V_{SS} to VREFP.
- 12-bit conversion rate: up to 400 kHz.
- Individual channels can be selected for conversion.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or Timer Match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.
- DMA support.

7.19 10-bit DAC

The LPC178x/7x contain one DAC. The DAC allows to generate a variable analog output. The maximum output value of the DAC is VREFP.

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7.23 I²S-bus serial I/O controllers

The LPC178x/7x contain one I²S-bus interface. The I²S-bus provides a standard communication interface for digital audio applications.

The I²S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S connection has one master, which is always the master, and one slave. The I²S interface on the LPC178x/7x provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.23.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz (16, 22.05, 32, 44.1, 48) kHz.
- Configurable word select period in master mode (separately for I²S input and output).
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S input and I²S output.

7.24 CAN controller and acceptance filters

The LPC178x/7x contain one CAN controller with two channels.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.24.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.

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PWM to immediately release all motor drive outputs. At the same time, the motor control PWM is highly configurable for other generalized timing, counting, capture, and compare applications.

The maximum PWM speed is determined by the PWM resolution (n) and the operating frequency f: PWM speed = $f/2^n$ (see Table 8).

Table 8. PWM speed at operating frequency 120 MHz

PWM resolution	PWM speed
6 bit	1.875 MHz
8 bit	0.468 MHz
10 bit	0.117 MHz

7.28 Quadrature Encoder Interface (QEI)

Remark: The QEI is available on parts LPC1788/87/86 and LPC1778/77/76

A quadrature encoder, also known as a 2-channel incremental encoder, converts angular displacement into two pulse signals. By monitoring both the number of pulses and the relative phase of the two signals, the user can track the position, direction of rotation, and velocity. In addition, a third channel, or index signal, can be used to reset the position counter. The quadrature encoder interface decodes the digital pulses from a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, the QEI can capture the velocity of the encoder wheel.

7.28.1 Features

- Tracks encoder position.
- Increments/decrements depending on direction.
- Programmable for 2× or 4× position counting.
- Velocity capture using built-in timer.
- Velocity compare function with “less than” interrupt.
- Uses 32-bit registers for position and velocity.
- Three position compare registers with interrupts.
- Index counter for revolution counting.
- Index compare register with interrupts.
- Can combine index and position interrupts to produce an interrupt for whole and partial revolution displacement.
- Digital filter with programmable delays for encoder input signals.
- Can accept decoded signal inputs (clk and direction).
- Connected to APB.

7.29 ARM Cortex-M3 system tick timer

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a 10 ms interval. In the LPC178x/7x, this timer can be clocked from the internal AHB clock or from a device pin.

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7.33.1.3 RTC oscillator

The RTC oscillator provides a 1 Hz clock to the RTC and a 32 kHz clock output that can be output on the CLKOUT pin in order to allow trimming the RTC oscillator without interference from a probe.

7.33.1.4 Watchdog oscillator

The Watchdog Timer has a dedicated watchdog oscillator that provides a 500 kHz clock to the Watchdog Timer. The watchdog oscillator is always running if the Watchdog Timer is enabled. The Watchdog oscillator clock can be output on the CLKOUT pin in order to allow observe its frequency.

In order to allow Watchdog Timer operation with minimum power consumption, which can be important in reduced power modes, the Watchdog oscillator frequency is not tightly controlled. The Watchdog oscillator frequency will vary over temperature and power supply within a particular part, and may vary by processing across different parts. This variation should be taken into account when determining Watchdog reload values.

Within a particular part, temperature and power supply variations can produce up to a ±17 % frequency variation. Frequency variation between devices under the same operating conditions can be up to ±30 %.

7.33.2 Main PLL (PLL0) and Alternate PLL (PLL1)

PLL0 (also called the Main PLL) and PLL1 (also called the Alternate PLL) are functionally identical but have somewhat different input possibilities and output connections. These possibilities are shown in Figure 7. The Main PLL can receive its input from either the IRC or the main oscillator and can potentially be used to provide the clocks to nearly everything on the device. The Alternate PLL receives its input only from the main oscillator and is intended to be used as an alternate source of clocking to the USB. The USB has timing needs that may not always be filled by the Main PLL.

Both PLLs are disabled and powered off on reset. If the Alternate PLL is left disabled, the USB clock can be supplied by PLL0 if everything is set up to provide 48 MHz to the USB clock through that route. The source for each clock must be selected via the CLKSEL registers and can be further reduced by clock dividers as needed.

PLL0 accepts an input clock frequency from either the IRC or the main oscillator. If only the Main PLL is used, then its output frequency must be an integer multiple of all other clocks needed in the system. PLL1 takes its input only from the main oscillator, requiring an external crystal in the range of 10 to 25 MHz. In each PLL, the Current Controlled Oscillator (CCO) operates in the range of 156 MHz to 320 MHz, so there are additional dividers to bring the output down to the desired frequencies. The minimum output divider value is 2, insuring that the output of the PLLs have a 50 % duty cycle.

If the USB is used, the possibilities for the CPU clock and other clocks will be limited by the requirements that the frequency be precise and very low jitter, and that the PLL0 output must be a multiple of 48 MHz. Even multiples of 48 MHz that are within the operating range of the PLL are 192 MHz and 288 MHz. Also, only the main oscillator in conjunction with the PLL can meet the precision and jitter specifications for USB. It is due to these limitations that the Alternate PLL is provided.

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On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this, four IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 12 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. Users need to reconfigure the PLL and clock dividers accordingly.

7.33.4.4 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

To optimize power conservation, the user has the additional option of turning off or retaining power to the 32 kHz oscillator. It is also possible to use external circuitry to turn off power to the on-chip regulator via the $V_{DD(REG)(3V3)}$ pins and/or the I/O power via the $V_{DD(3V3)}$ pins after entering Deep Power-down mode. Power must be restored before device operation can be restarted.

The LPC178x/7x can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

7.33.4.5 Wake-up Interrupt Controller (WIC)

The WIC allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep-sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC.This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

7.33.5 Peripheral power control

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

7.33.6 Power domains

The LPC178x/7x provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup registers.

On the LPC178x/7x, I/O pads are powered by $V_{DD(3V3)}$, while $V_{DD(REG)(3V3)}$ powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC178x/7x application, a design can use two power options to manage power consumption.

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The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(REG)(3V3)}$). Having the on-chip voltage regulator powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly” while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC domain. The RTC operates at very low power, which can be supplied by an external battery. The device core power ($V_{DD(REG)(3V3)}$) is used to operate the RTC whenever $V_{DD(REG)(3V3)}$ is present. There is no power drain from the RTC battery when $V_{DD(REG)(3V3)}$ is at nominal levels and $V_{DD(REG)(3V3)} > V_{BAT}$.

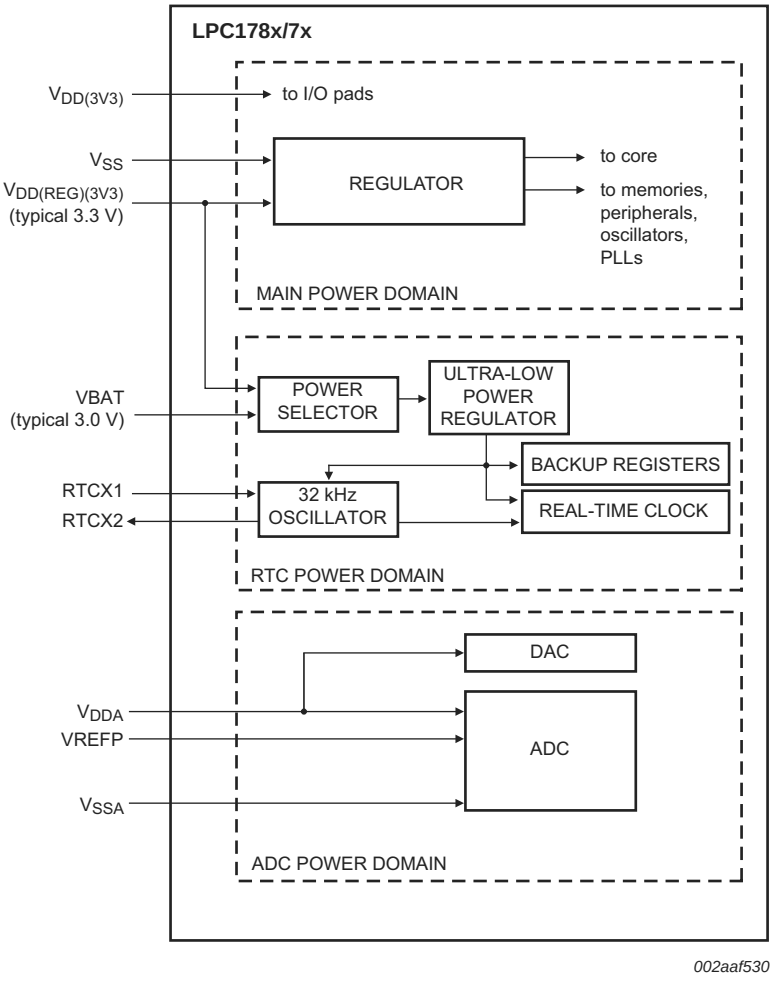

Fig 8. Power distribution

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9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

Table 10. Thermal characteristics
V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

Symbol	Parameter	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature	-	-	125	°C

Table 11. Thermal resistance (LQFP packages)
T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Conditions	Thermal resistance in °C/W ±15 %	
		LQFP208	LQFP144
θja	JEDEC (4.5 in × 4 in)		
	0 m/s	27.4	31.5
	1 m/s	25.7	28.1
	2.5 m/s	24.4	26.2
	Single-layer (4.5 in × 3 in)		
	0 m/s	35.4	43.2
	1 m/s	31.2	35.7
	2.5 m/s	29.2	32.8
θjc	-	8.8	7.8
θjb	-	15.4	13.8

Table 12. Thermal resistance value (TFBGA packages)
T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Conditions	Thermal resistance in °C/W ±15 %	
		TFBGA208	TFBGA180
θja	JEDEC (4.5 in × 4 in)		
	0 m/s	41	45.5
	1 m/s	35	38.3
	2.5 m/s	31	33.8
	8-layer (4.5 in × 3 in)		
	0 m/s	34.9	38
	1 m/s	30.9	33.5
	2.5 m/s	28	29.8
θjc	-	8.3	8.9
θjb	-	13.6	12

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10. Static characteristics

Table 13. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	2.4	3.3	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			2.4	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[3]	2.7	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[4]	2.1	3.0	3.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[3]	2.7	3.3	V_{DDA}	V
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	active mode; code `while(1){}` executed from flash; all peripherals disabled PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]	-	7	-	mA
		CCLK = 120 MHz; PLL enabled	[5][7]	-	51	-	mA
		active mode; code `while(1){}` executed from flash; all peripherals enabled; PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]		14		
		CCLK = 120 MHz; PLL enabled	[5][7]		100		mA
		Sleep mode	[5][8]	-	5	-	mA
		Deep-sleep mode	[5][9]	-	550	-	µA
		Power-down mode	[5][9]	-	280	-	µA
I_{BAT}	battery supply current	RTC running; part powered down; $V_{DD(REG)(3V3)}$ =0 V; $V_{i(VBAT)}$ = 3.0 V; $V_{DD(3V3)}$ = 0 V.	[10]	-	1	-	µA
		part powered; $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{i(VBAT)}$ = 3.0 V	[11]		<10		nA

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11.2 External memory interface

Table 17. Dynamic characteristics: Static external memory interface

C_L = 30 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		2.7	3.5	4.7	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[3]	2.7 + $T_{cy(clk)}$ × WAITOEN	3.4 + $T_{cy(clk)}$ × WAITOEN	4.6 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[3]	2.8	3.8	5.1	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[3]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.26	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.83	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 3.7	ns
t_{am}	memory access time	RD_5	[3][4]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 8.6	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 11.9	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 18.0	ns
$t_{h(D)}$	data input hold time	RD_6	[3][5]	−4.1	−5.8	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1		2.8	3.7	5.1	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[3]	2.7	3.5	4.6	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		[3]	0.1	0.1	0.16	ns
t_{deact}	deactivation time	RD_7	[3]	-	−3.4	−4.7	ns
Write cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		2.7	3.5	4.7	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		2.8	3.9	5.1	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[3]	2.7 + $T_{cy(clk)}$ × (1 + WAITWEN)	3.5 + $T_{cy(clk)}$ × (1 + WAITWEN)	4.6 + $T_{cy(clk)}$ × (1 + WAITWEN)	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[3]	2.8	3.9	5.1	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[3]	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 2.3	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 2.8	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 3.8	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[3]	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 2.6	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 3.4	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 4.9	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[3]	2.5 + $T_{cy(clk)}$	3.3 + $T_{cy(clk)}$	4.3 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[3][6]	$T_{cy(clk)}$ − 2.7	$T_{cy(clk)}$ − 3.4	$T_{cy(clk)}$ − 4.6	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1		2.7	3.6	4.8	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	PB = 1	[3]	2.4 + $T_{cy(clk)}$	3.0 + $T_{cy(clk)}$	3.9 + $T_{cy(clk)}$	ns

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11.7 I²C-bus

Table 27. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

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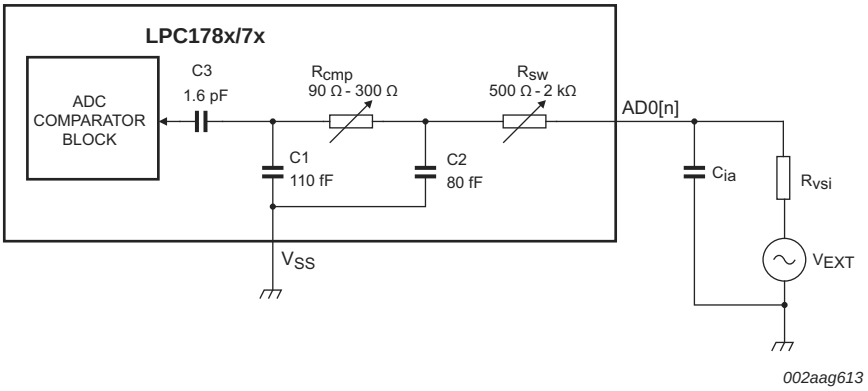

The values of resistor components R_{cmp} and R_{sw} vary with temperature and input voltage and are process-dependent.

Fig 29. ADC interface to pins ADC0_IN[n]

Table 32. ADC interface components

Component	Range	Description
R_{cmp}	90 Ω to 300 Ω	Switch-on resistance for the comparator input switch. Varies with temperature, input voltage, and process.
R_{sw}	500 Ω to 2 kΩ	Switch-on resistance for channel selection switch. Varies with temperature, input voltage, and process.
C1	110 fF	Parasitic capacitance from the ADC block level.
C2	80 fF	Parasitic capacitance from the ADC block level.
C3	1.6 pF	Sampling capacitor.

13. DAC electrical characteristics

Table 33. 10-bit DAC electrical characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
E_D	differential linearity error	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity	-	±1.5	-	LSB
E_O	offset error	-	0.6	-	%
E_G	gain error	-	0.6	-	%
C_L	load capacitance	-	-	200	pF
R_L	load resistance	1	-	-	kΩ

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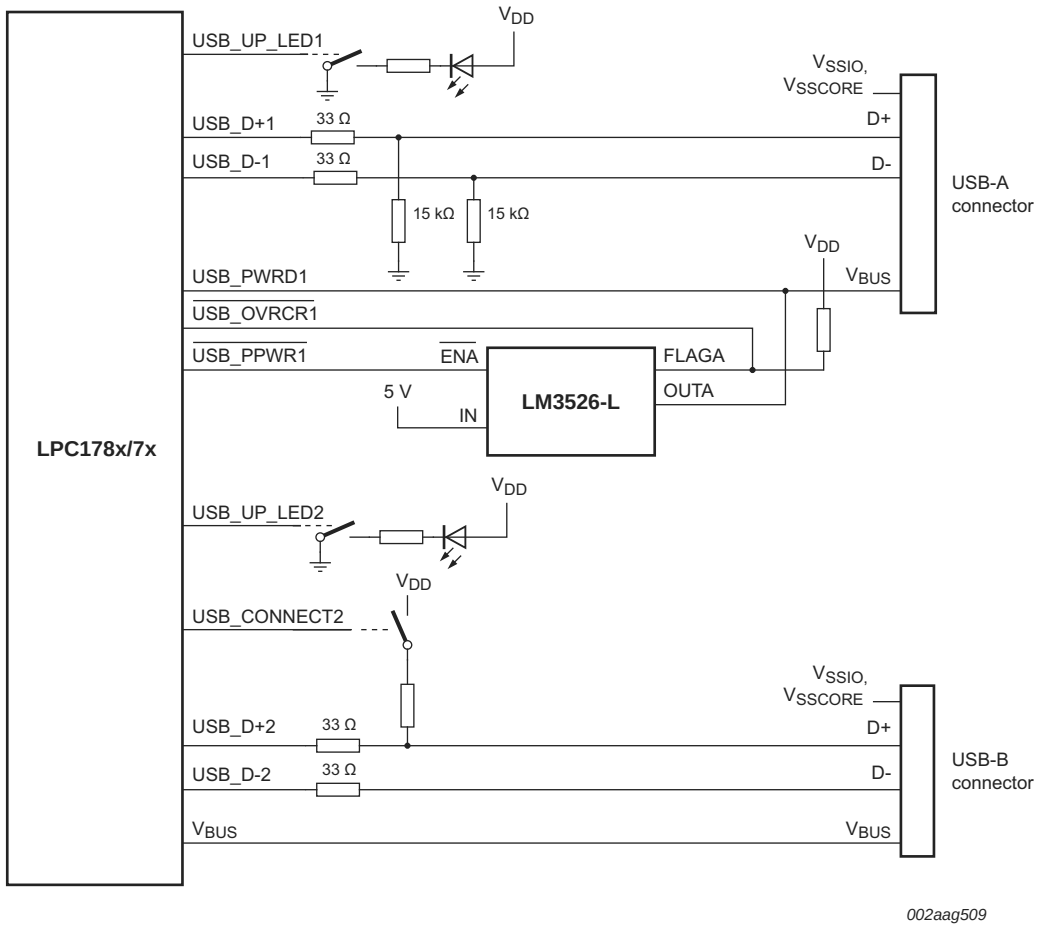

Fig 35. USB device port configuration: port 1 host and port 2 device

14.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

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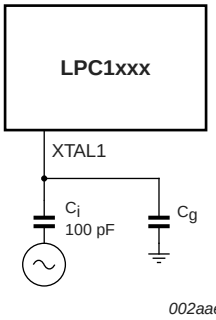

Fig 36. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 36), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 37 and in Table 34 and Table 35. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 37 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

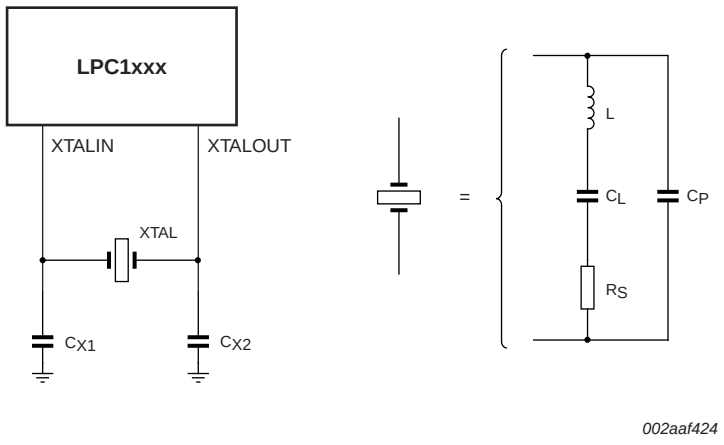

Fig 37. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 34. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
1 MHz to 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF

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Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC178X_7X v.4.1	20121115	Product data sheet	-	LPC178X_7X v.4
Modifications:	• LCD timing characteristics updated in Table 27 “Dynamic characteristics: LCD” and Figure 26 added. • Removed table note “The peak current is limited to 25 times the corresponding maximum current.” in Table 9. • Removed deep power-down spec Table 13 and associated table note. • Updated min value for t_{WEHEOW} Table 15. • Removed Fig 21 Internal RC oscillator frequency versus temperature. • Updated 12-bit and 8-bit values for E_T Table 29. • Changed data sheet status to Product.			
LPC178X_7X v.4	20120501	Preliminary data sheet	-	LPC178X_7X v.3
Modifications:	• Editorial updates. • BOD values added in Section 7.34.2. • Parameters $t_{CSLBLSL}$, t_{CSHOEH}, t_{OEHANV}, t_{deact}, $t_{BLSHEOW}$, $t_{BLSHDNV}$ updated in Table 17. • C_L = 10 pF added to Table 24, Table 26, Table 28. • $I_{DD(REG)(3V3)}$ corrected in Table 13 for conditions Deep-sleep mode, Power-down mode, and Deep-power down mode. • I_{BAT} corrected in Table 13 for condition Deep power-down mode. • Power consumption data in Figure 9 and Figure 10 corrected. • I/O voltage $V_{DD(3V3)}$ specified in Table 17, Table 18, Table 19, Table 24, Table 28. • $V_{DD(3V3)}$ range corrected in Table 23. • Parameter C_L changed to 10 pF for EMC timing in Table 17 to Table 20. • USB and Ethernet dynamic characteristics removed. Timing characteristics follow *USB 2.0 Specification* (full speed) and IEEE standard 802.3 standards (see Section 7.15 and Section 7.14 for compliance statements). • Pad characteristics updated in Table 3. • Parameter I_{BAT} updated in Table 13. • Figure 11 added. • SDRAM timing corrected in Figure 19. • EEPROM erase and programming times added (Table 16). • Data sheet status changed to preliminary.			

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