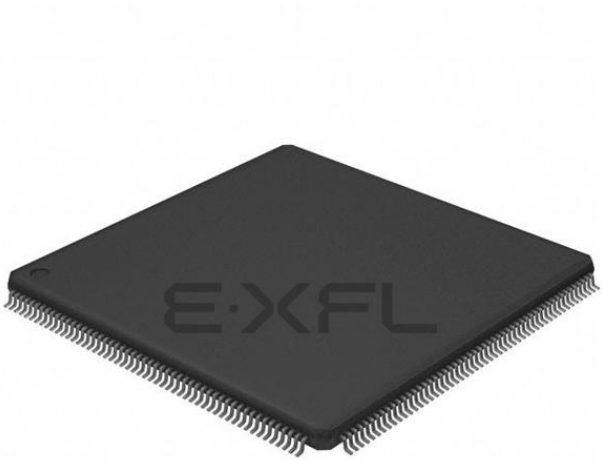

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	165
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1777fbd208-551

- Multilayer AHB matrix interconnect provides a separate bus for each AHB master. AHB masters include the CPU, USB, Ethernet, and the General Purpose DMA controller. This interconnect provides communication with no arbitration delays unless two masters attempt to access the same slave at the same time.
- Split APB bus allows for higher throughput with fewer stalls between the CPU and DMA. A single level of write buffering allows the CPU to continue without waiting for completion of APB writes if the APB was not already busy.
- Cortex-M3 system tick timer, including an external clock input option.
- Standard JTAG test/debug interface as well as Serial Wire Debug and Serial WireTrace Port options.
- Embedded Trace Macrocell (ETM) module supports real-time trace.
- Boundary scan for simplified board testing.
- Non-maskable Interrupt (NMI) input.

- Memory:
  - Up to 512 kB on-chip flash program memory with In-System Programming (ISP) and In-Application Programming (IAP) capabilities. The combination of an enhanced flash memory accelerator and location of the flash memory on the CPU local code/data bus provides high code performance from flash.
  - Up to 96 kB on-chip SRAM includes:

    64 kB of main SRAM on the CPU with local code/data bus for high-performance CPU access.

    Two 16 kB peripheral SRAM blocks with separate access paths for higher throughput. These SRAM blocks may be used for DMA memory as well as for general purpose instruction and data storage.
  - Up to 4032 byte on-chip EEPROM.
- LCD controller, supporting both Super-Twisted Nematic (STN) and Thin-Film Transistors (TFT) displays.
  - Dedicated DMA controller.
  - Selectable display resolution (up to 1024 $\times$ 768 pixels).
  - Supports up to 24-bit true-color mode.
- External Memory Controller (EMC) provides support for asynchronous static memory devices such as RAM, ROM and flash, as well as dynamic memories such as single data rate SDRAM with an SDRAM clock of up to 80 MHz.
- Eight channel General Purpose DMA controller (GPDMA) on the AHB multilayer matrix that can be used with the SSP, I2S, UART, CRC engine, Analog-to-Digital and Digital-to-Analog converter peripherals, timer match signals, GPIO, and for memory-to-memory transfers.
- Serial interfaces:
  - Ethernet MAC with MII/RMII interface and associated DMA controller. These functions reside on an independent AHB.
  - USB 2.0 full-speed dual-port device/host/OTG controller with on-chip PHY and associated DMA controller.
  - Five UARTs with fractional baud rate generation, internal FIFO, DMA support, and RS-485/EIA-485 support. One UART (UART1) has full modem control I/O, and one UART (USART4) supports IrDA, synchronous mode, and a smart card mode conforming to ISO7816-3.
  - Three SSP controllers with FIFO and multi-protocol capabilities. The SSP controllers can be used with the GPDMA.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[25]	80	T10	L7	56	[3]	I; PU	I/O	**P1[25] —** General purpose digital input/output pin.
							O	**USB_LS1 —** Low Speed status for USB port 1 (OTG transceiver).
							O	**USB_HSTEN1 —** Host Enabled status for USB port 1.
							O	**T1_MAT1 —** Match output for Timer 1, channel 1.
							O	**MC_1A —** Motor control PWM channel 1, output A.
							O	**CLKOUT —** Selectable clock output.
							O	**LCD_VD[11] —** LCD data.
							O	**LCD_VD[15] —** LCD data.
P1[26]	82	R10	P8	57	[3]	I; PU	I/O	**P1[26] —** General purpose digital input/output pin.
							O	**USB_SSPND1 —** USB port 1 Bus Suspend status (OTG transceiver).
							O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
							I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
							O	**MC_1B —** Motor control PWM channel 1, output B.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							O	**LCD_VD[12] —** LCD data.
							O	**LCD_VD[20] —** LCD data.
P1[27]	88	T12	M9	61	[3]	I; PU	I/O	**P1[27] —** General purpose digital input/output pin.
							I	**USB_INT1 —** USB port 1 OTG transceiver interrupt (OTG transceiver).
							I	**USB_OVRCR1 —** USB port 1 Over-Current status.
							I	**T0_CAP1 —** Capture input for Timer 0, channel 1.
							O	**CLKOUT —** Selectable clock output.
							-	**R —** Function reserved.
							O	**LCD_VD[13] —** LCD data.
							O	**LCD_VD[21] —** LCD data.
P1[28]	90	T13	P10	63	[3]	I; PU	I/O	**P1[28] —** General purpose digital input/output pin.
							I/O	**USB_SCL1 —** USB port 1 I^2C serial clock (OTG transceiver).
							I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
							O	**T0_MAT0 —** Match output for Timer 0, channel 0.
							O	**MC_2A —** Motor control PWM channel 2, output A.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							O	**LCD_VD[14] —** LCD data.
							O	**LCD_VD[22] —** LCD data.

Table 3. Pin description *…continued*

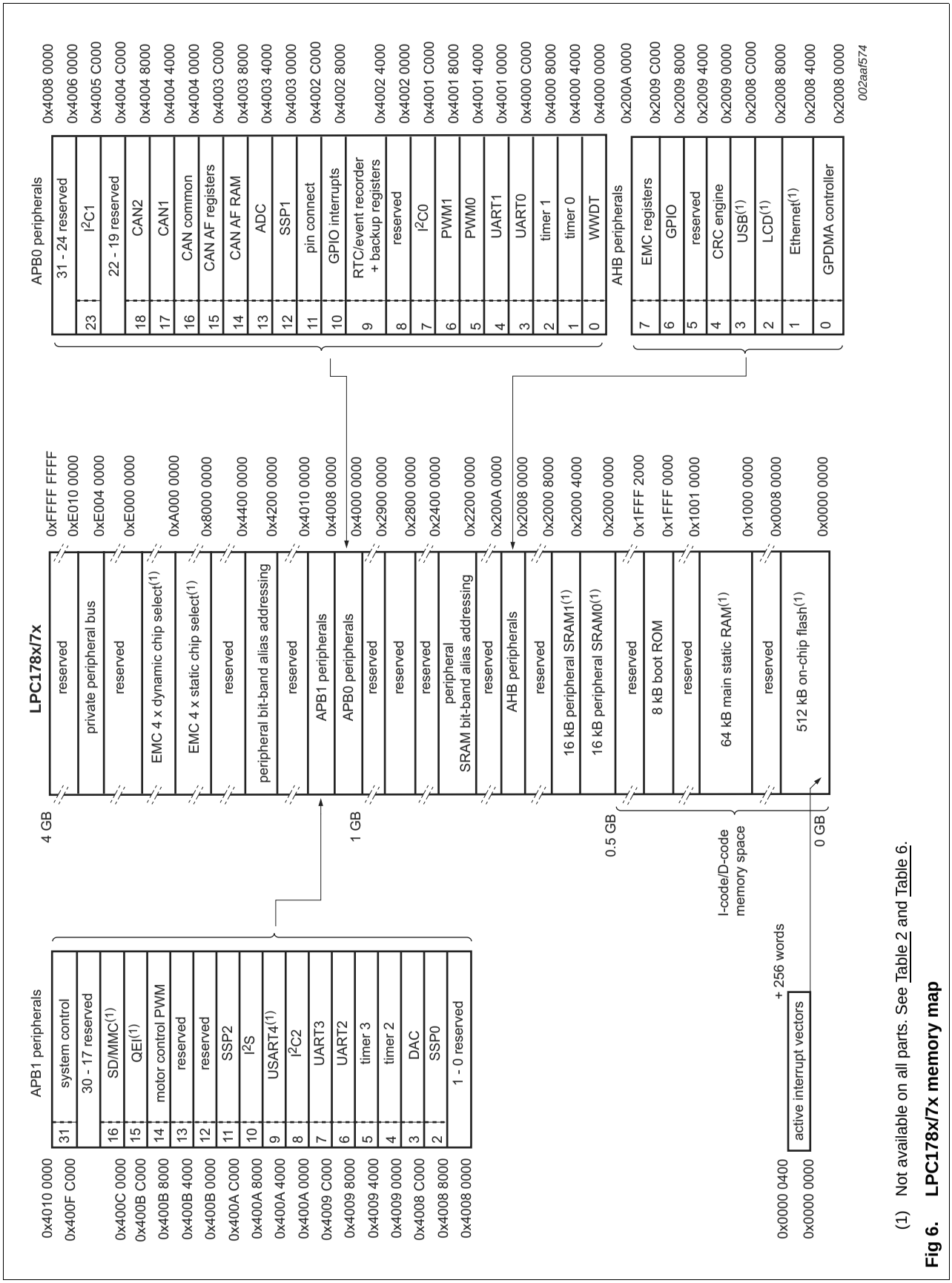
Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P4[1]	79	U10	M7	55	[3]	I; PU	I/O	**P4[1] —** General purpose digital input/output pin.
							I/O	**EMC_A[1] —** External memory address line 1.
P4[2]	83	T11	M8	58	[3]	I; PU	I/O	**P4[2] —** General purpose digital input/output pin.
							I/O	**EMC_A[2] —** External memory address line 2.
P4[3]	97	U16	K9	68	[3]	I; PU	I/O	**P4[3] —** General purpose digital input/output pin.
							I/O	**EMC_A[3] —** External memory address line 3.
P4[4]	103	R15	P13	72	[3]	I; PU	I/O	**P4[4] —** General purpose digital input/output pin.
							I/O	**EMC_A[4] —** External memory address line 4.
P4[5]	107	R16	H10	74	[3]	I; PU	I/O	**P4[5] —** General purpose digital input/output pin.
							I/O	**EMC_A[5] —** External memory address line 5.
P4[6]	113	M14	K10	78	[3]	I; PU	I/O	**P4[6] —** General purpose digital input/output pin.
							I/O	**EMC_A[6] —** External memory address line 6.
P4[7]	121	L16	K12	84	[3]	I; PU	I/O	**P4[7] —** General purpose digital input/output pin.
							I/O	**EMC_A[7] —** External memory address line 7.
P4[8]	127	J17	J11	88	[3]	I; PU	I/O	**P4[8] —** General purpose digital input/output pin.
							I/O	**EMC_A[8] —** External memory address line 8.
P4[9]	131	H17	H12	91	[3]	I; PU	I/O	**P4[9] —** General purpose digital input/output pin.
							I/O	**EMC_A[9] —** External memory address line 9.
P4[10]	135	G17	G12	94	[3]	I; PU	I/O	**P4[10] —** General purpose digital input/output pin.
							I/O	**EMC_A[10] —** External memory address line 10.
P4[11]	145	F14	F11	101	[3]	I; PU	I/O	**P4[11] —** General purpose digital input/output pin.
							I/O	**EMC_A[11] —** External memory address line 11.
P4[12]	149	C16	F10	104	[3]	I; PU	I/O	**P4[12] —** General purpose digital input/output pin.
							I/O	**EMC_A[12] —** External memory address line 12.
P4[13]	155	B16	B14	108	[3]	I; PU	I/O	**P4[13] —** General purpose digital input/output pin.
							I/O	**EMC_A[13] —** External memory address line 13.
P4[14]	159	B15	E8	110	[3]	I; PU	I/O	**P4[14] —** General purpose digital input/output pin.
							I/O	**EMC_A[14] —** External memory address line 14.
P4[15]	173	A11	C10	120	[3]	I; PU	I/O	**P4[15] —** General purpose digital input/output pin.
							I/O	**EMC_A[15] —** External memory address line 15.
P4[16]	101	U17	N12	-	[3]	I; PU	I/O	**P4[16] —** General purpose digital input/output pin.
							I/O	**EMC_A[16] —** External memory address line 16.
P4[17]	104	P14	N13	-	[3]	I; PU	I/O	**P4[17] —** General purpose digital input/output pin.
							I/O	**EMC_A[17] —** External memory address line 17.
P4[18]	105	P15	P14	-	[3]	I; PU	I/O	**P4[18] —** General purpose digital input/output pin.
							I/O	**EMC_A[18] —** External memory address line 18.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P4[19]	111	P16	M14	-	[3]	I; PU	I/O	**P4[19] —** General purpose digital input/output pin.
							I/O	**EMC_A[19] —** External memory address line 19.
P4[20]	109	R17	-	-	[3]	I; PU	I/O	**P4[20] —** General purpose digital input/output pin.
							I/O	**EMC_A[20] —** External memory address line 20.
							I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
							I/O	**SSP1_SCK —** Serial Clock for SSP1.
P4[21]	115	M15	-	-	[3]	I; PU	I/O	**P4[21] —** General purpose digital input/output pin.
							I/O	**EMC_A[21] —** External memory address line 21.
							I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
P4[22]	123	K14	-	-	[3]	I; PU	I/O	**P4[22] —** General purpose digital input/output pin.
							I/O	**EMC_A[22] —** External memory address line 22.
							O	**U2_TXD —** Transmitter output for UART2.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
P4[23]	129	J15	-	-	[3]	I; PU	I/O	**P4[23] —** General purpose digital input/output pin.
							I/O	**EMC_A[23] —** External memory address line 23.
							I	**U2_RXD —** Receiver input for UART2.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
P4[24]	183	B8	C8	127	[3]	I; PU	I/O	**P4[24] —** General purpose digital input/output pin.
							O	**$\overline{\text{EMC\_OE}}$ —** LOW active Output Enable signal.
P4[25]	179	B9	D9	124	[3]	I; PU	I/O	**P4[25] —** General purpose digital input/output pin.
							O	**$\overline{\text{EMC\_WE}}$ —** LOW active Write Enable signal.
P4[26]	119	L15	K13	-	[3]	I; PU	I/O	**P4[26] —** General purpose digital input/output pin.
							O	**$\overline{\text{EMC\_BLS0}}$ —** LOW active Byte Lane select signal 0.
P4[27]	139	G15	F14	-	[3]	I; PU	I/O	**P4[27] —** General purpose digital input/output pin.
							O	**$\overline{\text{EMC\_BLS1}}$ —** LOW active Byte Lane select signal 1.
P4[28]	170	C11	D10	118	[3]	I; PU	I/O	**P4[28] —** General purpose digital input/output pin.
							O	**$\overline{\text{EMC\_BLS2}}$ —** LOW active Byte Lane select signal 2.
							O	**U3_TXD —** Transmitter output for UART3.
							O	**T2_MAT0 —** Match output for Timer 2, channel 0.
							-	**R —** Function reserved.
							O	**LCD_VD[6] —** LCD data.
							O	**LCD_VD[10] —** LCD data.
							O	**LCD_VD[2] —** LCD data.



(1) Not available on all parts. See Table 2 and Table 6.

Fig 6. LPC178x/7x memory map

The LPC178x/7x EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

See Table 6 for EMC memory access.

7.10.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.11 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral and can be accessed through the AHB master. The GPDMA controller allows data transfers between the various on-chip SRAM areas and supports the SD/MMC card interface, all SSPs, the I^2S, all UARTs, the A/D Converter, and the D/A Converter peripherals. DMA can also be triggered by selected timer match conditions. Memory-to-memory transfers and transfers to or from GPIO are supported.

7.11.1 Features

- Eight DMA channels. Each channel can support an unidirectional transfer.
- 16 DMA request lines.
- Single DMA and burst DMA request signals. Each peripheral connected to the DMA Controller can assert either a burst DMA request or a single DMA request. The DMA burst size is set by programming the DMA Controller.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers are supported.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Hardware DMA channel priority.
- AHB slave DMA programming interface. The DMA Controller is programmed by writing to the DMA control registers over the AHB slave interface.
- One AHB bus master for transferring data. The interface transfers data when a DMA request goes active.
- 32-bit AHB master bus width.
- Incrementing or non-incrementing addressing for source and destination.
- Programmable DMA burst size. The DMA burst size can be programmed to more efficiently transfer data.
- Internal four-word FIFO per channel.
- Supports 8, 16, and 32-bit wide transactions.
- Big-endian and little-endian support. The DMA Controller defaults to little-endian mode on reset.
- An interrupt to the processor can be generated on a DMA completion or when a DMA error has occurred.
- Raw interrupt status. The DMA error and DMA count raw interrupt status can be read prior to masking.

7.12 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

7.12.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1’s complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.

- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

7.13 LCD controller

Remark: The LCD controller is available on parts LPC1788/87/86/85.

The LCD controller provides all of the necessary control signals to interface directly to a variety of color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512-byte color palette allows reducing bus utilization (i.e. memory size of the displayed data) while still supporting a large number of colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time needed to operate the display.

7.13.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized, for color STN and TFT.
- 24 bpp true-color non-palettized, for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.23 I²S-bus serial I/O controllers

The LPC178x/7x contain one I²S-bus interface. The I²S-bus provides a standard communication interface for digital audio applications.

The I²S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S connection has one master, which is always the master, and one slave. The I²S interface on the LPC178x/7x provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.23.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz (16, 22.05, 32, 44.1, 48) kHz.
- Configurable word select period in master mode (separately for I²S input and output).
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S input and I²S output.

7.24 CAN controller and acceptance filters

The LPC178x/7x contain one CAN controller with two channels.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.24.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.

- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

7.25 General purpose 32-bit timers/external event counters

The LPC178x/7x include four 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.25.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

7.26 Pulse Width Modulator (PWM)

The LPC178x/7x contain two standard PWMs.

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC178x/7x. The Timer is designed to count cycles of the system derived clock and optionally switch pins, generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is in addition to these features, and is based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the PWMMR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

7.26.1 Features

- LPC178x/7x has two PWM blocks with Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

7.27 Motor control PWM

The LPC178x/7x contain one motor control PWM.

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the

7.33.1.3 RTC oscillator

The RTC oscillator provides a 1 Hz clock to the RTC and a 32 kHz clock output that can be output on the CLKOUT pin in order to allow trimming the RTC oscillator without interference from a probe.

7.33.1.4 Watchdog oscillator

The Watchdog Timer has a dedicated watchdog oscillator that provides a 500 kHz clock to the Watchdog Timer. The watchdog oscillator is always running if the Watchdog Timer is enabled. The Watchdog oscillator clock can be output on the CLKOUT pin in order to allow observe its frequency.

In order to allow Watchdog Timer operation with minimum power consumption, which can be important in reduced power modes, the Watchdog oscillator frequency is not tightly controlled. The Watchdog oscillator frequency will vary over temperature and power supply within a particular part, and may vary by processing across different parts. This variation should be taken into account when determining Watchdog reload values.

Within a particular part, temperature and power supply variations can produce up to a ±17 % frequency variation. Frequency variation between devices under the same operating conditions can be up to ±30 %.

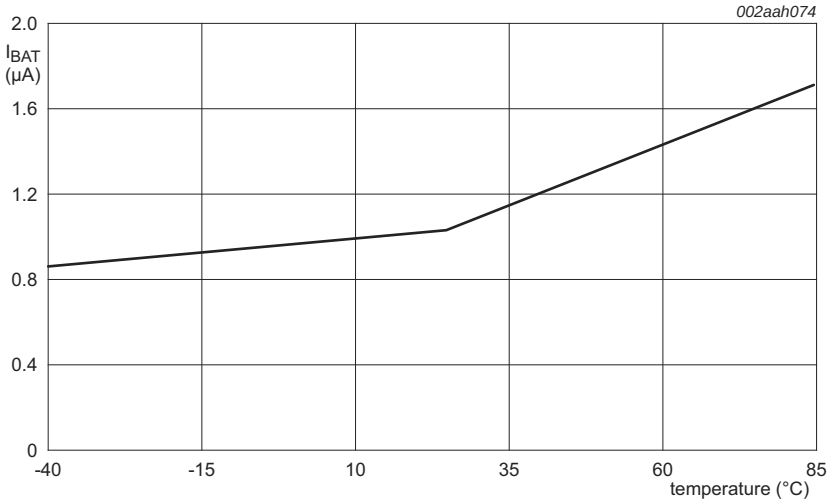
7.33.2 Main PLL (PLL0) and Alternate PLL (PLL1)

PLL0 (also called the Main PLL) and PLL1 (also called the Alternate PLL) are functionally identical but have somewhat different input possibilities and output connections. These possibilities are shown in Figure 7. The Main PLL can receive its input from either the IRC or the main oscillator and can potentially be used to provide the clocks to nearly everything on the device. The Alternate PLL receives its input only from the main oscillator and is intended to be used as an alternate source of clocking to the USB. The USB has timing needs that may not always be filled by the Main PLL.

Both PLLs are disabled and powered off on reset. If the Alternate PLL is left disabled, the USB clock can be supplied by PLL0 if everything is set up to provide 48 MHz to the USB clock through that route. The source for each clock must be selected via the CLKSEL registers and can be further reduced by clock dividers as needed.

PLL0 accepts an input clock frequency from either the IRC or the main oscillator. If only the Main PLL is used, then its output frequency must be an integer multiple of all other clocks needed in the system. PLL1 takes its input only from the main oscillator, requiring an external crystal in the range of 10 to 25 MHz. In each PLL, the Current Controlled Oscillator (CCO) operates in the range of 156 MHz to 320 MHz, so there are additional dividers to bring the output down to the desired frequencies. The minimum output divider value is 2, insuring that the output of the PLLs have a 50 % duty cycle.

If the USB is used, the possibilities for the CPU clock and other clocks will be limited by the requirements that the frequency be precise and very low jitter, and that the PLL0 output must be a multiple of 48 MHz. Even multiples of 48 MHz that are within the operating range of the PLL are 192 MHz and 288 MHz. Also, only the main oscillator in conjunction with the PLL can meet the precision and jitter specifications for USB. It is due to these limitations that the Alternate PLL is provided.



Conditions: $V_{DD(REG)(3V3)} = V_{DDA} = V_{DD(3V3)} = 0$; $V_{BAT} = 3.0$ V.

Fig 11. Part powered off: Typical battery supply current (I_{BAT}) versus temperature

11.2 External memory interface

Table 17. Dynamic characteristics: Static external memory interface

C_L = 30 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		2.7	3.5	4.7	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[3]	2.7 + $T_{cy(clk)}$ × WAITOEN	3.4 + $T_{cy(clk)}$ × WAITOEN	4.6 + $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[3]	2.8	3.8	5.1	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[3]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.26	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 2.83	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 3.7	ns
t_{am}	memory access time	RD_5	[3][4]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 8.6	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 11.9	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$ − 18.0	ns
$t_{h(D)}$	data input hold time	RD_6	[3][5]	−4.1	−5.8	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1		2.8	3.7	5.1	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[3]	2.7	3.5	4.6	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		[3]	0.1	0.1	0.16	ns
t_{deact}	deactivation time	RD_7	[3]	-	−3.4	−4.7	ns
Write cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		2.7	3.5	4.7	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		2.8	3.9	5.1	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[3]	2.7 + $T_{cy(clk)}$ × (1 + WAITWEN)	3.5 + $T_{cy(clk)}$ × (1 + WAITWEN)	4.6 + $T_{cy(clk)}$ × (1 + WAITWEN)	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[3]	2.8	3.9	5.1	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[3]	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 2.3	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 2.8	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$ − 3.8	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[3]	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 2.6	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 3.4	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 4.9	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[3]	2.5 + $T_{cy(clk)}$	3.3 + $T_{cy(clk)}$	4.3 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[3][6]	$T_{cy(clk)}$ − 2.7	$T_{cy(clk)}$ − 3.4	$T_{cy(clk)}$ − 4.6	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1		2.7	3.6	4.8	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	PB = 1	[3]	2.4 + $T_{cy(clk)}$	3.0 + $T_{cy(clk)}$	3.9 + $T_{cy(clk)}$	ns

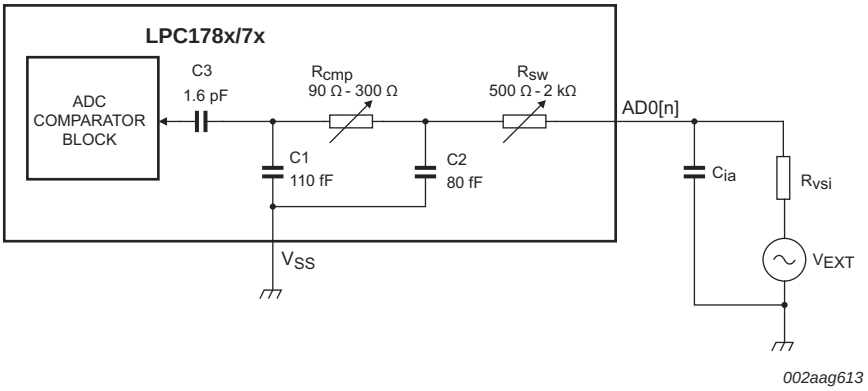
[6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 28.

[7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 28.

[8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 28.

[9] See Figure 29.

[10] 8-bit resolution is achieved by ignoring the lower four bits of the ADC conversion result.



The values of resistor components R_{cmp} and R_{sw} vary with temperature and input voltage and are process-dependent.

Fig 29. ADC interface to pins ADC0_IN[n]

Table 32. ADC interface components

Component	Range	Description
R_{cmp}	90 Ω to 300 Ω	Switch-on resistance for the comparator input switch. Varies with temperature, input voltage, and process.
R_{sw}	500 Ω to 2 kΩ	Switch-on resistance for channel selection switch. Varies with temperature, input voltage, and process.
C1	110 fF	Parasitic capacitance from the ADC block level.
C2	80 fF	Parasitic capacitance from the ADC block level.
C3	1.6 pF	Sampling capacitor.

13. DAC electrical characteristics

Table 33. 10-bit DAC electrical characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
E_D	differential linearity error	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity	-	±1.5	-	LSB
E_O	offset error	-	0.6	-	%
E_G	gain error	-	0.6	-	%
C_L	load capacitance	-	-	200	pF
R_L	load resistance	1	-	-	kΩ

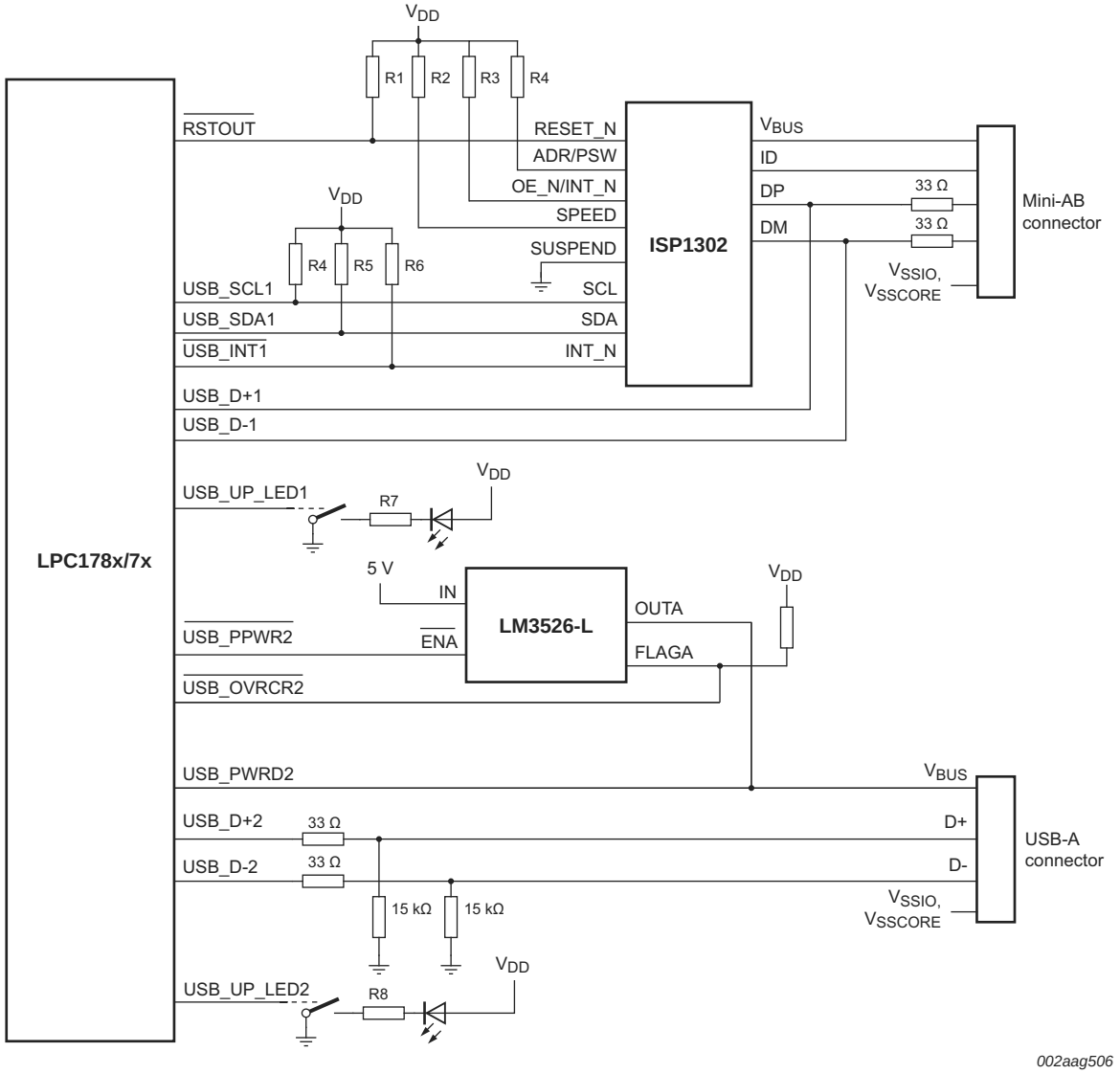


Fig 32. USB OTG port configuration: port 1 OTG dual-role device, port 2 host

To eliminate the loss of time counts in the RTC due to voltage swing or ramp rate of the $\overline{\text{RESET}}$ signal, connect an RC filter between the $\overline{\text{RESET}}$ pin and the external reset input.

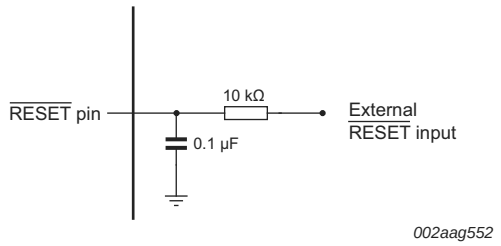


Fig 40. Reset input with RC filter

19. Revision history

Table 37. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC178X_7X v.5.5	20160426	Product data sheet	-	LPC178X_7X v.5.4
Modifications:	• Updated Table 29 “Dynamic characteristics: LCD”: $t_{d(QV)}$ max value is 9 ns for accuracy; was 12 ns.			
LPC178X_7X v.5.4	20160321	Product data sheet	CIN 201603016I	LPC178X_7X v.5.3
Modifications:	• Added Table 18 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00” for 10 pF load. • Updated Table 19 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00” for 30 pF load. • Added Table 20 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01” for 10 pF load. • Updated Table 21 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01” for 30 pF load. • Updated Table 22 “Dynamic characteristics: Dynamic external memory interface programmable clock delays (CMDDLY, FBCLKDLY, CLKOUT0DLY and CLKOUT1DLY)”. • Updated Figure 19 “Dynamic external memory interface signal timing”.			
LPC178X_7X v.5.3	20151015	Product data sheet	-	LPC178X_7X v.5.2
Modifications:	• Corrected max value of $t_{v(Q)}$ (data output valid time) in SPI mode to $3*T_{cy(PCLK)}$ + 6.3 ns. Was: $3*T_{cy(PCLK)}$ + 2.5 ns. See Table 26 “Dynamic characteristics: SSP pins in SPI mode”.			
LPC178X_7X v.5.2	20150814	Product data sheet	-	LPC178X_7X v.5.1
Modifications:	• Updated max value of $t_{v(Q)}$ (data output valid time) in SPI mode to $3*T_{cy(PCLK)}$ + 2.5 ns. See Table 24 “Dynamic characteristics: SSP pins in SPI mode”. • Added a column for GPIO pins and device order part number to the ordering options table. See Table 2 “LPC178x/7x ordering options”.			
LPC178X_7X v.5.1	20140501	Product data sheet	-	LPC178X_7X v.5
Modifications:	• Updated parameter $t_{su(D)}$ in Table 18 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00”: Minimum value changed to (FBCLKDLY + 1) × 0.25 + 0.3. Maximum value removed. • Removed max value from parameter $t_{h(D)}$ in Table 17. • Removed min value from parameter t_{deact} in Table 17. • Specified ADC conversion rate in burst mode in Table 29 “12-bit ADC characteristics”.			

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