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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 109 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 96K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 3.6V |
| Data Converters | A/D 8x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1778fbd144-551 |

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| P0[8] | 160 | A15 | C12 | 111 | [4] | I; IA | I/O | **P0[8] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2S_TX_WS —** $I^2S$ Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | | | | | | I/O | **SSP1_MISO —** Master In Slave Out for SSP1. |
| | | | | | | | O | **T2_MAT2 —** Match output for Timer 2, channel 2. |
| | | | | | | | I | **RTC_EV1 —** Event input 1 to Event Monitor/Recorder. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD[16] —** LCD data. |
| P0[9] | 158 | C14 | A13 | 109 | [4] | I; IA | I/O | **P0[9] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **I2S_TX_SDA —** $I^2S$ transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *$I^2S$-bus specification*. |
| | | | | | | | I/O | **SSP1_MOSI —** Master Out Slave In for SSP1. |
| | | | | | | | O | **T2_MAT3 —** Match output for Timer 2, channel 3. |
| | | | | | | | I | **RTC_EV2 —** Event input 2 to Event Monitor/Recorder. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD[17] —** LCD data. |
| P0[10] | 98 | T15 | L10 | 69 | [3] | I; PU | I/O | **P0[10] —** General purpose digital input/output pin. |
| | | | | | | | O | **U2_TXD —** Transmitter output for UART2. |
| | | | | | | | I/O | **I2C2_SDA —** $I^2C2$ data input/output (this pin does not use a specialized I2C pad). |
| | | | | | | | O | **T3_MAT0 —** Match output for Timer 3, channel 0. |
| P0[11] | 100 | R14 | P12 | 70 | [3] | I; PU | I/O | **P0[11] —** General purpose digital input/output pin. |
| | | | | | | | I | **U2_RXD —** Receiver input for UART2. |
| | | | | | | | I/O | **I2C2_SCL —** $I^2C2$ clock input/output (this pin does not use a specialized I2C pad). |
| | | | | | | | O | **T3_MAT1 —** Match output for Timer 3, channel 1. |
| P0[12] | 41 | R1 | J4 | 29 | [5] | I; PU | I/O | **P0[12] —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2. |
| | | | | | | | I/O | **SSP1_MISO —** Master In Slave Out for SSP1. |
| | | | | | | | I | **ADC0_IN[6] —** A/D converter 0, input 6. When configured as an ADC input, the digital function of the pin must be disabled. |

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| P1[8] | 190 | C7 | B6 | 132 | [3] | I; PU | I/O | **P1[8] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_CRS (ENET_CRS_DV) —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT1 —** Match output for Timer 3, channel 1. |
| | | | | | | | I/O | **SSP2_SSEL —** Slave Select for SSP2. |
| P1[9] | 188 | A6 | D7 | 131 | [3] | I; PU | I/O | **P1[9] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT0 —** Match output for Timer 3, channel 0. |
| P1[10] | 186 | C8 | A7 | 129 | [3] | I; PU | I/O | **P1[10] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T3_CAP0 —** Capture input for Timer 3, channel 0. |
| P1[11] | 163 | A14 | A12 | - | [3] | I; PU | I/O | **P1[11] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RXD2 —** Ethernet Receive Data 2 (MII interface). |
| | | | | | | | I/O | **SD_DAT[2] —** Data line 2 for SD card interface. |
| | | | | | | | O | **PWM0[6] —** Pulse Width Modulator 0, output 6. |
| P1[12] | 157 | A16 | A14 | - | [3] | I; PU | I/O | **P1[12] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RXD3 —** Ethernet Receive Data (MII interface). |
| | | | | | | | I/O | **SD_DAT[3] —** Data line 3 for SD card interface. |
| | | | | | | | I | **PWM0_CAP0 —** Capture input for PWM0, channel 0. |
| P1[13] | 147 | D16 | D14 | - | [3] | I; PU | I/O | **P1[13] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RX_DV —** Ethernet Receive Data Valid (MII interface). |
| P1[14] | 184 | A7 | D8 | 128 | [3] | I; PU | I/O | **P1[14] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RX_ER —** Ethernet receive error (RMII/MII interface). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T2_CAP0 —** Capture input for Timer 2, channel 0. |
| P1[15] | 182 | A8 | A8 | 126 | [3] | I; PU | I/O | **P1[15] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RX_CLK (ENET_REF_CLK) —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **I2C2_SDA —** $I^2C2$ data input/output (this pin does not use a specialized I2C pad). |

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| P1[16] | 180 | D10 | B8 | 125 | [3] | I; PU | I/O | **P1[16] —** General purpose digital input/output pin. |
| | | | | | | | O | **ENET_MDC —** Ethernet MIIM clock. |
| | | | | | | | O | **I2S_TX_MCLK —** I2S transmit master clock. |
| P1[17] | 178 | A9 | C9 | 123 | [3] | I; PU | I/O | **P1[17] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **ENET_MDIO —** Ethernet MIIM data input and output. |
| | | | | | | | O | **I2S_RX_MCLK —** I2S receive master clock. |
| P1[18] | 66 | P7 | L5 | 46 | [3] | I; PU | I/O | **P1[18] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB_UP_LED1 —** It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus. |
| | | | | | | | O | **PWM1[1] —** Pulse Width Modulator 1, channel 1 output. |
| | | | | | | | I | **T1_CAP0 —** Capture input for Timer 1, channel 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **SSP1_MISO —** Master In Slave Out for SSP1. |
| P1[19] | 68 | U6 | P5 | 47 | [3] | I; PU | I/O | **P1[19] —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{USB\_TX\_E1}}$ —** Transmit Enable signal for USB port 1 (OTG transceiver). |
| | | | | | | | O | **$\overline{\text{USB\_PPWR1}}$ —** Port Power enable signal for USB port 1. |
| | | | | | | | I | **T1_CAP1 —** Capture input for Timer 1, channel 1. |
| | | | | | | | O | **MC_0A —** Motor control PWM channel 0, output A. |
| | | | | | | | I/O | **SSP1_SCK —** Serial clock for SSP1. |
| | | | | | | | O | **U2_OE —** RS-485/EIA-485 output enable signal for UART2. |
| P1[20] | 70 | U7 | K6 | 49 | [3] | I; PU | I/O | **P1[20] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB_TX_DP1 —** D+ transmit data for USB port 1 (OTG transceiver). |
| | | | | | | | O | **PWM1[2] —** Pulse Width Modulator 1, channel 2 output. |
| | | | | | | | I | **QEI_PHA —** Quadrature Encoder Interface PHA input. |
| | | | | | | | I | **MC_FB0 —** Motor control PWM channel 0 feedback input. |
| | | | | | | | I/O | **SSP0_SCK —** Serial clock for SSP0. |
| | | | | | | | O | **LCD_VD[6] —** LCD data. |
| | | | | | | | O | **LCD_VD[10] —** LCD data. |

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| P2[5] | 140 | F16 | F12 | 97 | [3] | I; PU | I/O | **P2[5] —** General purpose digital input/output pin. |
| | | | | | | | O | **PWM1[6] —** Pulse Width Modulator 1, channel 6 output. |
| | | | | | | | O | **U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1. |
| | | | | | | | O | **T2_MAT0 —** Match output for Timer 2, channel 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **TRACEDATA[0] —** Trace data, bit 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT). |
| P2[6] | 138 | E17 | F13 | 96 | [3] | I; PU | I/O | **P2[6] —** General purpose digital input/output pin. |
| | | | | | | | I | **PWM1_CAP0 —** Capture input for PWM1, channel 0. |
| | | | | | | | I | **U1_RI —** Ring Indicator input for UART1. |
| | | | | | | | I | **T2_CAP0 —** Capture input for Timer 2, channel 0. |
| | | | | | | | O | **U2_OE —** RS-485/EIA-485 output enable signal for UART2. |
| | | | | | | | O | **TRACECLK —** Trace clock. |
| | | | | | | | O | **LCD_VD[0] —** LCD data. |
| | | | | | | | O | **LCD_VD[4] —** LCD data. |
| P2[7] | 136 | G16 | G11 | 95 | [3] | I; PU | I/O | **P2[7] —** General purpose digital input/output pin. |
| | | | | | | | I | **CAN_RD2 —** CAN2 receiver input. |
| | | | | | | | O | **U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD[1] —** LCD data. |
| | | | | | | | O | **LCD_VD[5] —** LCD data. |
| P2[8] | 134 | H15 | G14 | 93 | [3] | I; PU | I/O | **P2[8] —** General purpose digital input/output pin. |
| | | | | | | | O | **CAN_TD2 —** CAN2 transmitter output. |
| | | | | | | | O | **U2_TXD —** Transmitter output for UART2. |
| | | | | | | | I | **U1_CTS —** Clear to Send input for UART1. |
| | | | | | | | O | **ENET_MDC —** Ethernet MIIM clock. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD[2] —** LCD data. |
| | | | | | | | O | **LCD_VD[6] —** LCD data. |

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| P3[0] | 197 | B4 | D6 | 137 | [3] | I; PU | I/O | **P3[0] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[0] —** External memory data line 0. |
| P3[1] | 201 | B3 | E6 | 140 | [3] | I; PU | I/O | **P3[1] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[1] —** External memory data line 1. |
| P3[2] | 207 | B1 | A2 | 144 | [3] | I; PU | I/O | **P3[2] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[2] —** External memory data line 2. |
| P3[3] | 3 | E4 | G5 | 2 | [3] | I; PU | I/O | **P3[3] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[3] —** External memory data line 3. |
| P3[4] | 13 | F2 | D3 | 9 | [3] | I; PU | I/O | **P3[4] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[4] —** External memory data line 4. |
| P3[5] | 17 | G1 | E3 | 12 | [3] | I; PU | I/O | **P3[5] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[5] —** External memory data line 5. |
| P3[6] | 23 | J1 | F4 | 16 | [3] | I; PU | I/O | **P3[6] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[6] —** External memory data line 6. |
| P3[7] | 27 | L1 | G3 | 19 | [3] | I; PU | I/O | **P3[7] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[7] —** External memory data line 7. |
| P3[8] | 191 | D8 | A6 | - | [3] | I; PU | I/O | **P3[8] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[8] —** External memory data line 8. |
| P3[9] | 199 | C5 | A4 | - | [3] | I; PU | I/O | **P3[9] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[9] —** External memory data line 9. |
| P3[10] | 205 | B2 | B3 | - | [3] | I; PU | I/O | **P3[10] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[10] —** External memory data line 10. |
| P3[11] | 208 | D5 | B2 | - | [3] | I; PU | I/O | **P3[11] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[11] —** External memory data line 11. |
| P3[12] | 1 | D4 | A1 | - | [3] | I; PU | I/O | **P3[12] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[12] —** External memory data line 12. |
| P3[13] | 7 | C1 | C1 | - | [3] | I; PU | I/O | **P3[13] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[13] —** External memory data line 13. |
| P3[14] | 21 | H2 | F1 | - | [3] | I; PU | I/O | **P3[14] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[14] —** External memory data line 14. |
| P3[15] | 28 | M1 | G4 | - | [3] | I; PU | I/O | **P3[15] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[15] —** External memory data line 15. |
| P3[16] | 137 | F17 | - | - | [3] | I; PU | I/O | **P3[16] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[16] —** External memory data line 16. |
| | | | | | | | O | **PWM0[1] —** Pulse Width Modulator 0, output 1. |
| | | | | | | | O | **U1_TXD —** Transmitter output for UART1. |

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| P4[1] | 79 | U10 | M7 | 55 | [3] | I; PU | I/O | **P4[1] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[1] —** External memory address line 1. |
| P4[2] | 83 | T11 | M8 | 58 | [3] | I; PU | I/O | **P4[2] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[2] —** External memory address line 2. |
| P4[3] | 97 | U16 | K9 | 68 | [3] | I; PU | I/O | **P4[3] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[3] —** External memory address line 3. |
| P4[4] | 103 | R15 | P13 | 72 | [3] | I; PU | I/O | **P4[4] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[4] —** External memory address line 4. |
| P4[5] | 107 | R16 | H10 | 74 | [3] | I; PU | I/O | **P4[5] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[5] —** External memory address line 5. |
| P4[6] | 113 | M14 | K10 | 78 | [3] | I; PU | I/O | **P4[6] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[6] —** External memory address line 6. |
| P4[7] | 121 | L16 | K12 | 84 | [3] | I; PU | I/O | **P4[7] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[7] —** External memory address line 7. |
| P4[8] | 127 | J17 | J11 | 88 | [3] | I; PU | I/O | **P4[8] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[8] —** External memory address line 8. |
| P4[9] | 131 | H17 | H12 | 91 | [3] | I; PU | I/O | **P4[9] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[9] —** External memory address line 9. |
| P4[10] | 135 | G17 | G12 | 94 | [3] | I; PU | I/O | **P4[10] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[10] —** External memory address line 10. |
| P4[11] | 145 | F14 | F11 | 101 | [3] | I; PU | I/O | **P4[11] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[11] —** External memory address line 11. |
| P4[12] | 149 | C16 | F10 | 104 | [3] | I; PU | I/O | **P4[12] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[12] —** External memory address line 12. |
| P4[13] | 155 | B16 | B14 | 108 | [3] | I; PU | I/O | **P4[13] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[13] —** External memory address line 13. |
| P4[14] | 159 | B15 | E8 | 110 | [3] | I; PU | I/O | **P4[14] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[14] —** External memory address line 14. |
| P4[15] | 173 | A11 | C10 | 120 | [3] | I; PU | I/O | **P4[15] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[15] —** External memory address line 15. |
| P4[16] | 101 | U17 | N12 | - | [3] | I; PU | I/O | **P4[16] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[16] —** External memory address line 16. |
| P4[17] | 104 | P14 | N13 | - | [3] | I; PU | I/O | **P4[17] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[17] —** External memory address line 17. |
| P4[18] | 105 | P15 | P14 | - | [3] | I; PU | I/O | **P4[18] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[18] —** External memory address line 18. |

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| P4[19] | 111 | P16 | M14 | - | [3] | I; PU | I/O | **P4[19] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[19] —** External memory address line 19. |
| P4[20] | 109 | R17 | - | - | [3] | I; PU | I/O | **P4[20] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[20] —** External memory address line 20. |
| | | | | | | | I/O | **I2C2_SDA —** $I^2C2$ data input/output (this pin does not use a specialized I2C pad). |
| | | | | | | | I/O | **SSP1_SCK —** Serial Clock for SSP1. |
| P4[21] | 115 | M15 | - | - | [3] | I; PU | I/O | **P4[21] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[21] —** External memory address line 21. |
| | | | | | | | I/O | **I2C2_SCL —** $I^2C2$ clock input/output (this pin does not use a specialized I2C pad). |
| | | | | | | | I/O | **SSP1_SSEL —** Slave Select for SSP1. |
| P4[22] | 123 | K14 | - | - | [3] | I; PU | I/O | **P4[22] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[22] —** External memory address line 22. |
| | | | | | | | O | **U2_TXD —** Transmitter output for UART2. |
| | | | | | | | I/O | **SSP1_MISO —** Master In Slave Out for SSP1. |
| P4[23] | 129 | J15 | - | - | [3] | I; PU | I/O | **P4[23] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_A[23] —** External memory address line 23. |
| | | | | | | | I | **U2_RXD —** Receiver input for UART2. |
| | | | | | | | I/O | **SSP1_MOSI —** Master Out Slave In for SSP1. |
| P4[24] | 183 | B8 | C8 | 127 | [3] | I; PU | I/O | **P4[24] —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{EMC\_OE}}$ —** LOW active Output Enable signal. |
| P4[25] | 179 | B9 | D9 | 124 | [3] | I; PU | I/O | **P4[25] —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{EMC\_WE}}$ —** LOW active Write Enable signal. |
| P4[26] | 119 | L15 | K13 | - | [3] | I; PU | I/O | **P4[26] —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{EMC\_BLS0}}$ —** LOW active Byte Lane select signal 0. |
| P4[27] | 139 | G15 | F14 | - | [3] | I; PU | I/O | **P4[27] —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{EMC\_BLS1}}$ —** LOW active Byte Lane select signal 1. |
| P4[28] | 170 | C11 | D10 | 118 | [3] | I; PU | I/O | **P4[28] —** General purpose digital input/output pin. |
| | | | | | | | O | **$\overline{\text{EMC\_BLS2}}$ —** LOW active Byte Lane select signal 2. |
| | | | | | | | O | **U3_TXD —** Transmitter output for UART3. |
| | | | | | | | O | **T2_MAT0 —** Match output for Timer 2, channel 0. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD[6] —** LCD data. |
| | | | | | | | O | **LCD_VD[10] —** LCD data. |
| | | | | | | | O | **LCD_VD[2] —** LCD data. |

**Table 4. Pin allocation table TFBGA208**

*Not all functions are available on all parts. See Table 2 and Table 7 (EMC pins).*

| Ball | Symbol | Ball | Symbol | Ball | Symbol | Ball | Symbol |
|---|---|---|---|---|---|---|---|
| 1 | P3[13] | 2 | JTAG_TDI | 3 | P5[4] | 4 | P0[2] |
| 5 | P3[9] | 6 | P3[22] | 7 | P1[8] | 8 | P1[10] |
| 9 | $V_{DD(3V3)}$ | 10 | P3[21] | 11 | P4[28] | 12 | P0[5] |
| 13 | P0[7] | 14 | P0[9] | 15 | P3[18] | 16 | P4[12] |
| 17 | $V_{DD(3V3)}$) | | - | | - | | - |
| **Row D** | | | | | | | |
| 1 | JTAG_TRST | 2 | P3[28] | 3 | JTAG_TDO (SWO) | 4 | P3[12] |
| 5 | P3[11] | 6 | P0[3] | 7 | $V_{DD(3V3)}$ | 8 | P3[8] |
| 9 | P1[2] | 10 | P1[16] | 11 | $V_{DD(REG)(3V3)}$ | 12 | VSSREG |
| 13 | P0[6] | 14 | P1[7] | 15 | P2[2] | 16 | P1[13] |
| 17 | P2[4] | | - | | - | | - |
| **Row E** | | | | | | | |
| 1 | P0[26] | 2 | JTAG_TCK (SWDCLK) | 3 | JTAG_TMS (SWDIO) | 4 | P3[3] |
| 5 | - | 6 | - | 7 | - | 8 | - |
| 9 | - | 10 | - | 11 | - | 12 | - |
| 13 | - | 14 | P2[1] | 15 | $V_{SS}$ | 16 | P2[3] |
| 17 | P2[6] | | - | | - | | - |
| **Row F** | | | | | | | |
| 1 | P0[25] | 2 | P3[4] | 3 | P3[29] | 4 | P5[0] |
| 5 | - | 6 | - | 7 | - | 8 | - |
| 9 | - | 10 | - | 11 | - | 12 | - |
| 13 | - | 14 | P4[11] | 15 | P3[17] | 16 | P2[5] |
| 17 | P3[16] | | - | | - | | - |
| **Row G** | | | | | | | |
| 1 | P3[5] | 2 | P0[24] | 3 | $V_{DD(3V3)}$ | 4 | $V_{DDA}$ |
| 5 | - | 6 | - | 7 | - | 8 | - |
| 9 | - | 10 | - | 11 | - | 12 | - |
| 13 | - | 14 | P5[3] | 15 | P4[27] | 16 | P2[7] |
| 17 | P4[10] | | - | | - | | - |
| **Row H** | | | | | | | |
| 1 | P0[23] | 2 | P3[14] | 3 | P3[30] | 4 | $V_{DD(REG)(3V3)}$ |
| 5 | - | 6 | - | 7 | - | 8 | - |
| 9 | - | 10 | - | 11 | - | 12 | - |
| 13 | - | 14 | $V_{SS}$ | 15 | P2[8] | 16 | P2[9] |
| 17 | P4[9] | | - | | - | | - |
| **Row J** | | | | | | | |
| 1 | P3[6] | 2 | $V_{SSA}$ | 3 | P3[31] | 4 | P5[1] |
| 5 | - | 6 | - | 7 | - | 8 | - |
| 9 | - | 10 | - | 11 | - | 12 | - |

**Table 5. Pin allocation table TFBGA180**

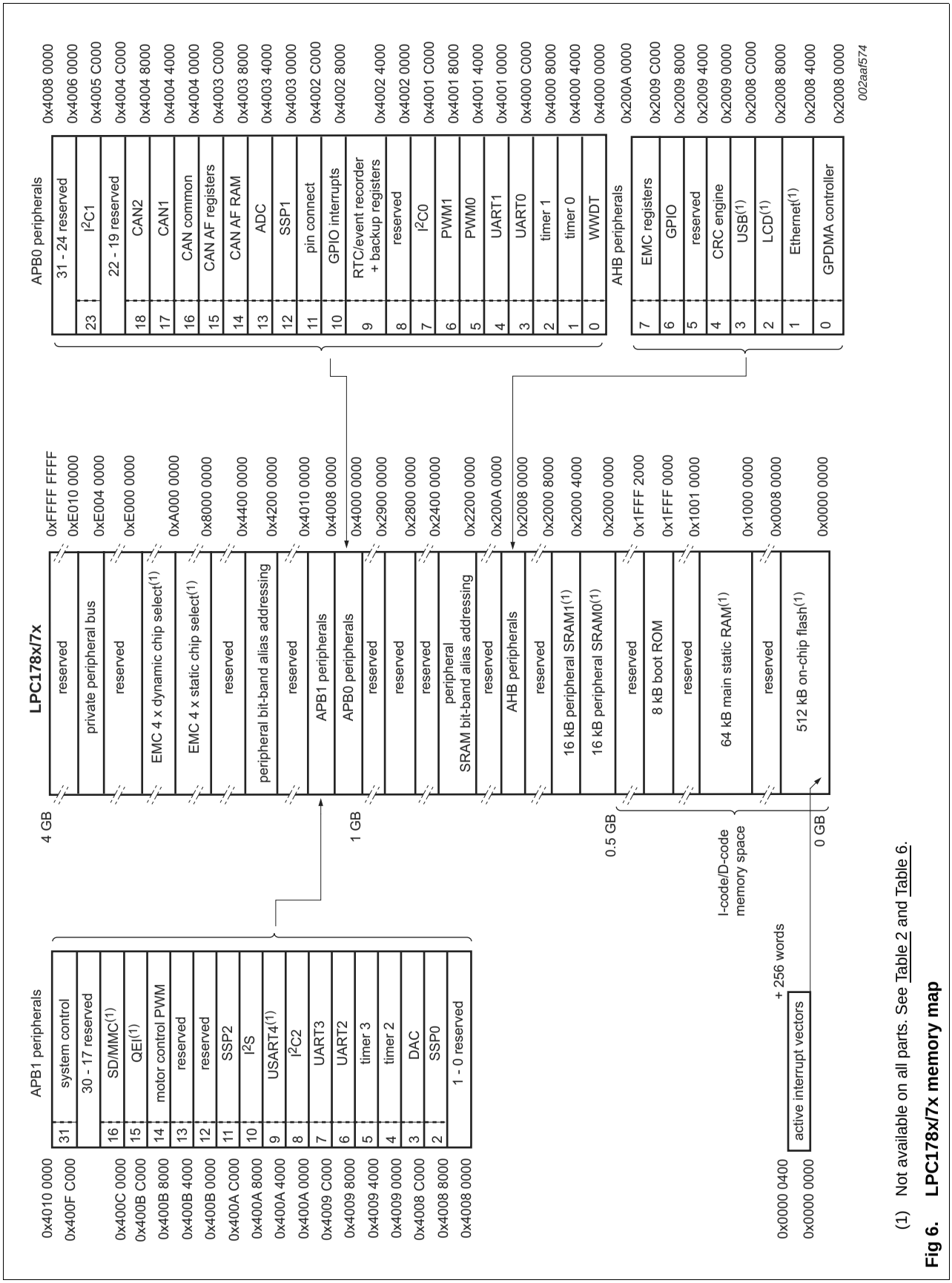
*Not all functions are available on all parts. See Table 2 and Table 7 (EMC pins).*

| Ball | Symbol | Ball | Symbol | Ball | Symbol | Ball | Symbol |
|---|---|---|---|---|---|---|---|
| **Row J** | | | | | | | |
| 1 | $\overline{\text{RESET}}$ | 2 | RTCX1 | 3 | RTCX2 | 4 | P0[12] |
| 5 | P0[13] | 6 | - | 7 | - | 8 | - |
| 9 | - | 10 | P0[19] | 11 | P4[8] | 12 | P0[17] |
| 13 | P0[18] | 14 | $V_{DD(3V3)}$ | | - | | - |
| **Row K** | | | | | | | |
| 1 | VBAT | 2 | P1[31] | 3 | P1[30] | 4 | XTAL2 |
| 5 | P0[29] | 6 | P1[20] | 7 | P3[26] | 8 | $V_{DD(3V3)}$ |
| 9 | P4[3] | 10 | P4[6] | 11 | P0[21] | 12 | P4[7] |
| 13 | P4[26] | 14 | P0[20] | | - | | - |
| **Row L** | | | | | | | |
| 1 | P2[29] | 2 | XTAL1 | 3 | P0[27] | 4 | $V_{DD(3V3)}$ |
| 5 | P1[18] | 6 | P4[0] | 7 | P1[25] | 8 | $V_{SSREG}$ |
| 9 | $V_{SS}$ | 10 | P0[10] | 11 | $V_{DD(3V3)}$ | 12 | P5[2] |
| 13 | $V_{SS}$ | 14 | P0[22] | | - | | - |
| **Row M** | | | | | | | |
| 1 | P0[28] | 2 | P2[28] | 3 | P3[25] | 4 | P3[23] |
| 5 | P0[14] | 6 | P1[22] | 7 | P4[1] | 8 | P4[2] |
| 9 | P1[27] | 10 | P0[0] | 11 | P2[13] | 12 | P2[11] |
| 13 | P2[10] | 14 | P4[19] | | - | | - |
| **Row N** | | | | | | | |
| 1 | P0[31] | 2 | USB_D-2 | 3 | P3[24] | 4 | P0[30] |
| 5 | P2[19] | 6 | P1[21] | 7 | P1[23] | 8 | P2[21] |
| 9 | $V_{DD(REG)(3V3)}$ | 10 | P1[29] | 11 | P0[1] | 12 | P4[16] |
| 13 | P4[17] | 14 | P2[12] | | - | | - |
| **Row P** | | | | | | | |
| 1 | P2[24] | 2 | P2[25] | 3 | P2[18] | 4 | $V_{SS}$ |
| 5 | P1[19] | 6 | P2[20] | 7 | P1[24] | 8 | P1[26] |
| 9 | P2[16] | 10 | P1[28] | 11 | P2[17] | 12 | P0[11] |
| 13 | P4[4] | 14 | P4[18] | | - | | - |

# 7. Functional description

## 7.1 Architectural overview

The ARM Cortex-M3 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses are faster than the system bus and are used similarly to Tightly Coupled Memory (TCM) interfaces: one bus dedicated for instruction fetch (I-code) and one bus for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.




(1) Not available on all parts. See Table 2 and Table 6.

**Fig 6. LPC178x/7x memory map**

- Physical interface:
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

## 7.15 USB interface

**Remark:** The USB Device/Host/OTG controller is available on parts LPC1788/87/86/85 and LPC1778/77/76. The USB Device-only controller is available on parts LPC1774.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

Details on typical USB interfacing solutions can be found in Section 14.1.

### 7.15.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the USB RAM.

#### 7.15.1.1 Features

- Fully compliant with *USB 2.0 Specification* (full speed).
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the LPC178x/7x can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

### 7.15.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

#### 7.15.2.1 Features

- OHCI compliant.

## 7.23 I²S-bus serial I/O controllers

The LPC178x/7x contain one I²S-bus interface. The I²S-bus provides a standard communication interface for digital audio applications.

The I²S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S connection has one master, which is always the master, and one slave. The I²S interface on the LPC178x/7x provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

### 7.23.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz (16, 22.05, 32, 44.1, 48) kHz.
- Configurable word select period in master mode (separately for I²S input and output).
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S input and I²S output.

## 7.24 CAN controller and acceptance filters

The LPC178x/7x contain one CAN controller with two channels.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

### 7.24.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.

- Global Acceptance Filter recognizes 11-bit and 29-bit receive identifiers for all CAN buses.
- Acceptance Filter can provide FullCAN-style automatic reception for selected Standard Identifiers.
- FullCAN messages can generate interrupts.

## 7.25 General purpose 32-bit timers/external event counters

The LPC178x/7x include four 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

### 7.25.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Two 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- Up to two match registers can be used to generate timed DMA requests.

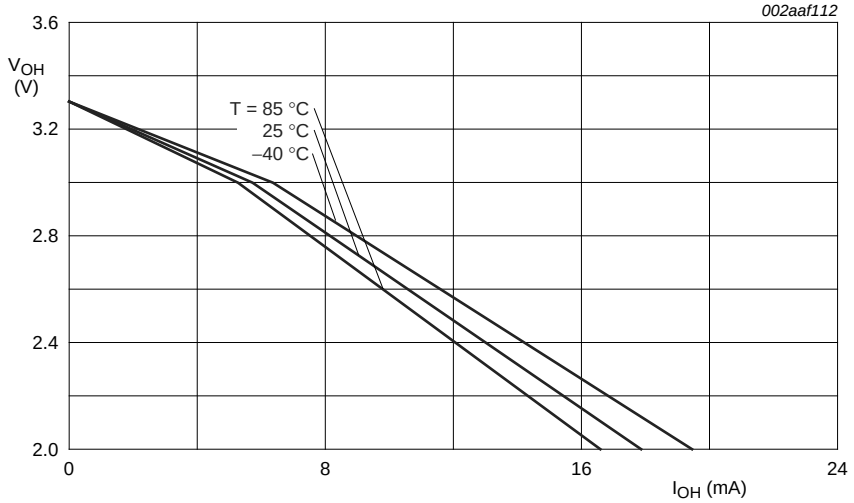
## 7.26 Pulse Width Modulator (PWM)

The LPC178x/7x contain two standard PWMs.

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC178x/7x. The Timer is designed to count cycles of the system derived clock and optionally switch pins, generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is in addition to these features, and is based on match register events.

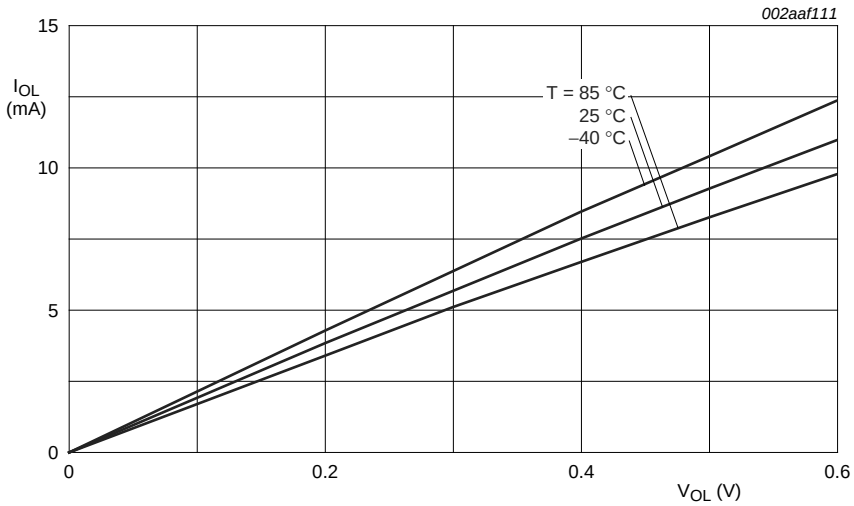
The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

## 10.3 Electrical pin characteristics



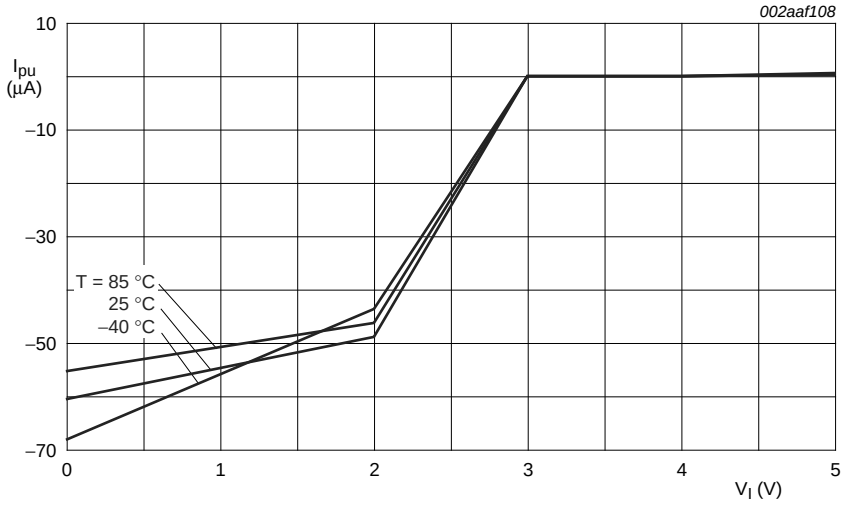

Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

**Fig 12. Typical HIGH-level output voltage $V_{OH}$ versus HIGH-level output source current $I_{OH}$**



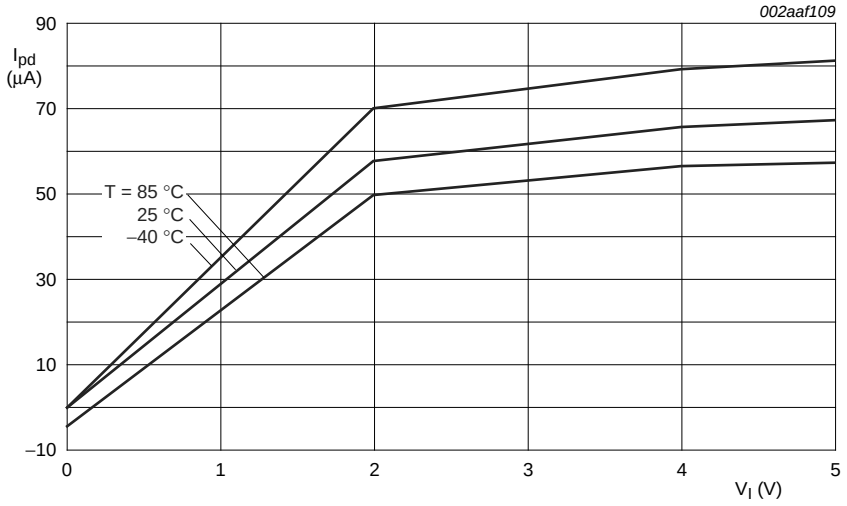

Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

**Fig 13. Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**




Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

**Fig 14. Typical pull-up current $I_{pu}$ versus input voltage $V_I$**




Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

**Fig 15. Typical pull-down current $I_{pd}$ versus input voltage $V_I$**

**Table 22. Dynamic characteristics: Dynamic external memory interface programmable clock delays (CMDDLY, FBCLKDLY, CLKOUT0DLY and CLKOUT1DLY)**

*$T_{amb}$ = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V.Values guaranteed by design. $t_{cmddly}$ is programmable delay value for EMC command outputs in command delayed mode; $t_{fbdly}$ is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.*

| Symbols | Parameter | Five bit value for each delay in EMCDLYCTL[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{cmddly}$, $t_{fbdly}$, $t_{clk0dly}$, $t_{clk1dly}$ | delay time | b00000 | 0.0 | 0.0 | 0.0 | ns |
| | | b00001 | 0.1 | 0.1 | 0.2 | ns |
| | | b00010 | 0.2 | 0.3 | 0.5 | ns |
| | | b00011 | 0.3 | 0.4 | 0.7 | ns |
| | | b00100 | 0.5 | 0.8 | 1.3 | ns |
| | | b00101 | 0.6 | 0.9 | 1.5 | ns |
| | | b00110 | 0.7 | 1.1 | 1.8 | ns |
| | | b00111 | 0.8 | 1.2 | 2.0 | ns |
| | | b01000 | 1.2 | 1.8 | 2.9 | ns |
| | | b01001 | 1.3 | 1.9 | 3.1 | ns |
| | | b01010 | 1.4 | 2.0 | 3.4 | ns |
| | | b01011 | 1.5 | 2.1 | 3.6 | ns |
| | | b01100 | 1.7 | 2.6 | 4.2 | ns |
| | | b01101 | 1.8 | 2.7 | 4.4 | ns |
| | | b01110 | 1.9 | 2.9 | 4.7 | ns |
| | | b01111 | 2.0 | 3.0 | 4.9 | ns |
| | | b10000 | 2.4 | 3.7 | 6.0 | ns |
| | | b10001 | 2.5 | 3.8 | 6.2 | ns |
| | | b10010 | 2.6 | 4.0 | 6.5 | ns |
| | | b10011 | 2.7 | 4.1 | 6.7 | ns |
| | | b10100 | 2.9 | 4.5 | 7.3 | ns |
| | | b10101 | 3.0 | 4.6 | 7.5 | ns |
| | | b10110 | 3.1 | 4.8 | 7.8 | ns |
| | | b10111 | 3.2 | 4.9 | 8.0 | ns |
| | | b11000 | 3.6 | 5.4 | 8.9 | ns |
| | | b11001 | 3.7 | 5.5 | 9.1 | ns |
| | | b11010 | 3.8 | 5.7 | 9.4 | ns |
| | | b11011 | 3.9 | 5.8 | 9.6 | ns |
| | | b11100 | 4.1 | 6.2 | 10.2 | ns |
| | | b11101 | 4.2 | 6.3 | 10.4 | ns |
| | | b11110 | 4.3 | 6.6 | 10.7 | ns |
| | | b11111 | 4.4 | 6.7 | 10.9 | ns |

[1] The programmable delay blocks are controlled by the EMCDLYCTL register in the EMC register block. All delay times are incremental delays for each element starting from delay block 0. See the *LPC178x/7x user manual* for details.

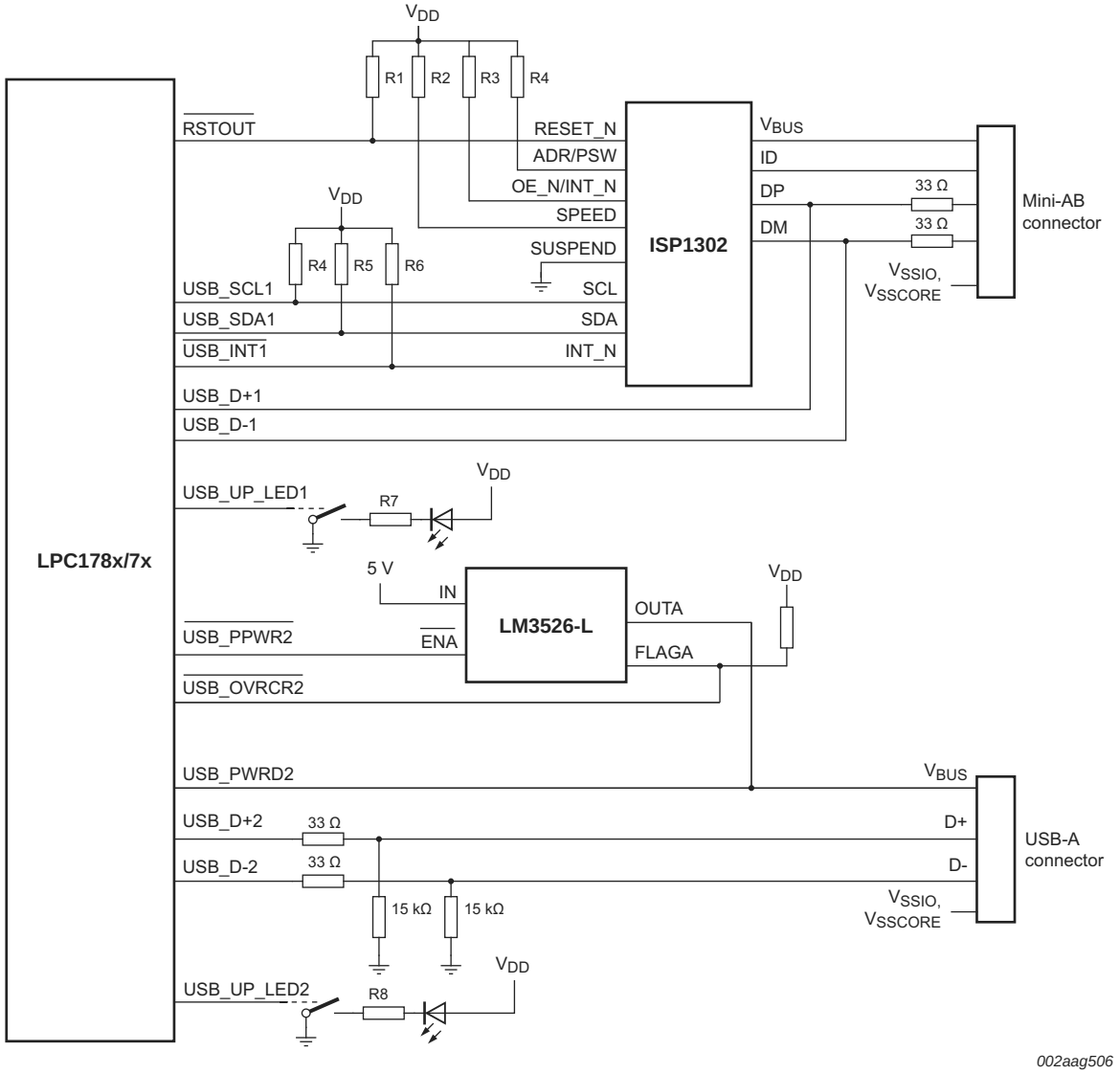
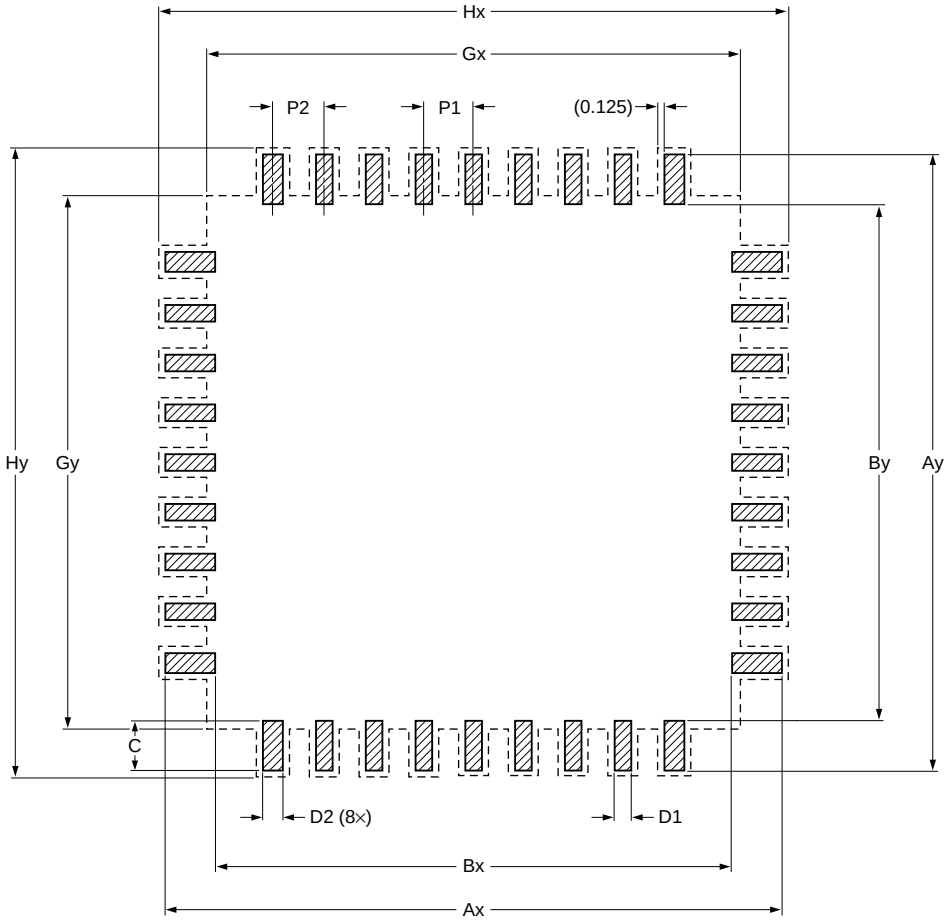



**Fig 32. USB OTG port configuration: port 1 OTG dual-role device, port 2 host**

**Footprint information for reflow soldering of LQFP144 package** **SOT486-1**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

| P1 | P2 | Ax | Ay | Bx | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.500 | 0.560 | 23.300 | 23.300 | 20.300 | 20.300 | 1.500 | 0.280 | 0.400 | 20.500 | 20.500 | 23.550 | 23.550 |

*sot486-1_fr*

**Fig 47. Reflow soldering of the LQFP144 package**

## 18. References

[1] LPC178x/7x User manual UM10470:
http://www.nxp.com/documents/user_manual/UM10470.pdf

[2] LPC177x/8x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC177X_8X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

**Table 37. Revision history** *…continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC178X_7X v.3 | 20111220 | Objective data sheet | - | LPC178X_7X v.2 |
| Modifications: | • Removed BOOT function from pin P3[14].<br>• $I_{BAT}$ and $I_{DD(REG)(3V3)}$ updated for Deep power-down mode in Table 13.<br>• Maximum SDRAM clock of 80 MHz specified in Section 2, Table 18, and Table 19.<br>• Power consumption data added (Figure 9 and Figure 10).<br>• Removed parameter $Z_{DRV}$ in Table 13.<br>• Specified maximum value for parameter $C_L$ in Table 33 and remove typical value.<br>• Specified setting of boost bits in Table 14, Table note 5 and in Table 13, Table note 6 .<br>• USB connection diagrams updated (Figure 33 to Figure 36).<br>• Current drain condition on battery supply specified in Section 7.33.6.<br>• Table note 10 in Table 13 updated.<br>• ADC characteristics updated (Table 31).<br>• Section 14.6 “Reset pin configuration for RTC operation” added.<br>• EEPROM size for parts LPC1774 corrected in Table 2 and Figure 1.<br>• Changed function LCD_VD[5] on pin P0[10] to Reserved.<br>• Changed function LCD_VD[10] on pin P0[11] to Reserved.<br>• Changed function LCD_VD[13] on pin P0[19] to Reserved.<br>• Changed function LCD_VD[14] on pin P0[20] to Reserved.<br>• ADC interface model updated (see Table 32 and Figure 30). | | | |
| LPC178X_7X v.2 | 20110527 | Objective data sheet | - | LPC178X_7X v.1 |
| Modifications: | • Symbol names in Table 3 to Table 5 abbreviated.<br>• Reserved functions added in Table 3.<br>• Added function LCD_VD[5] to pin P0[10].<br>• Added function LCD_VD[10] to pin P0[11].<br>• Added function LCD_VD[13] to pin P0[19].<br>• Added function LCD_VD[14] to pin P0[20].<br>• Added function U4_SCLK to pin P0[21].<br>• Added function<br>• Added function MOSI to pin P5[0].<br>• Added function SSP2_MISO to pin P5[1].<br>• Added EMC dynamic characteristics. | | | |
| LPC178X_7X v.1 | 20110524 | Objective data sheet | - | - |