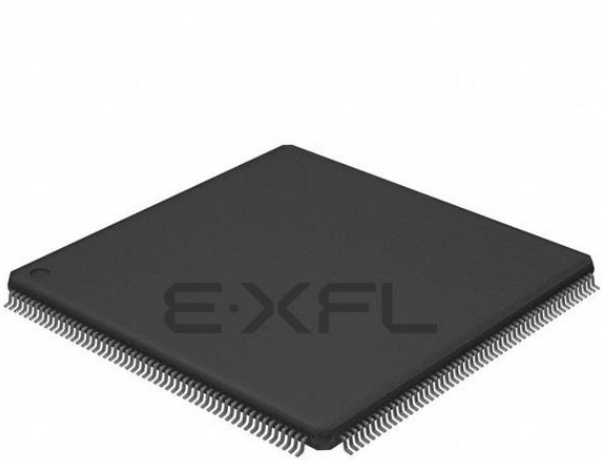

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	165
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1778fbd208-551

6. Pinning information

6.1 Pinning

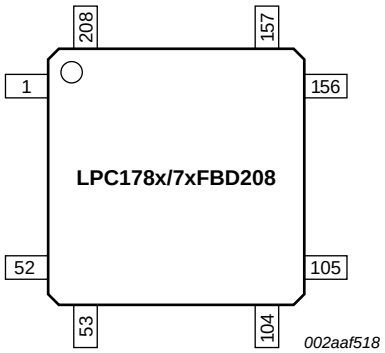


Fig 2. Pin configuration (LQFP208)

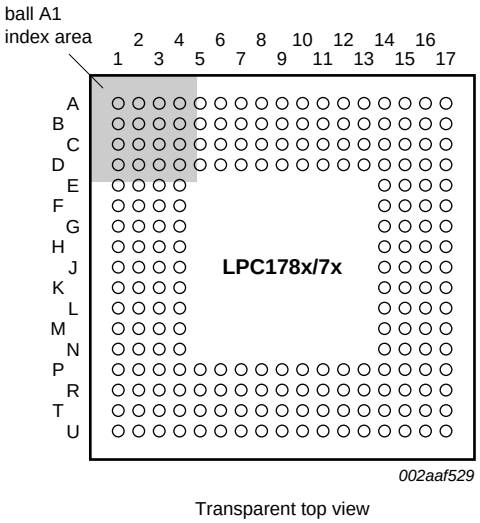


Fig 3. Pin configuration (TFBGA208)

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[8]	160	A15	C12	111	[4]	I; IA	I/O	**P0[8] —** General purpose digital input/output pin.
							I/O	**I2S_TX_WS —** I^2S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
							I	**RTC_EV1 —** Event input 1 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[16] —** LCD data.
P0[9]	158	C14	A13	109	[4]	I; IA	I/O	**P0[9] —** General purpose digital input/output pin.
							I/O	**I2S_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
							I	**RTC_EV2 —** Event input 2 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[17] —** LCD data.
P0[10]	98	T15	L10	69	[3]	I; PU	I/O	**P0[10] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for UART2.
							I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P0[11]	100	R14	P12	70	[3]	I; PU	I/O	**P0[11] —** General purpose digital input/output pin.
							I	**U2_RXD —** Receiver input for UART2.
							I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT1 —** Match output for Timer 3, channel 1.
P0[12]	41	R1	J4	29	[5]	I; PU	I/O	**P0[12] —** General purpose digital input/output pin.
							O	**$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							I	**ADC0_IN[6] —** A/D converter 0, input 6. When configured as an ADC input, the digital function of the pin must be disabled.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[1]	194	B5	A5	135	[3]	I; PU	I/O	**P1[1] —** General purpose digital input/output pin.
							O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output for Timer 3, channel 3.
							I/O	**SSP2_MOSI —** Master Out Slave In for SSP2.
P1[2]	185	D9	B7	-	[3]	I; PU	I/O	**P1[2] —** General purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							O	**SD_CLK —** Clock output line for SD card interface.
							O	**PWM0[1] —** Pulse Width Modulator 0, output 1.
P1[3]	177	A10	A9	-	[3]	I; PU	I/O	**P1[3] —** General purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**SD_CMD —** Command line for SD card interface.
							O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
P1[4]	192	A5	C6	133	[3]	I; PU	I/O	**P1[4] —** General purpose digital input/output pin.
							O	**ENET_TX_EN —** Ethernet transmit data enable (RMII/MII interface).
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output for Timer 3, channel 2.
							I/O	**SSP2_MISO —** Master In Slave Out for SSP2.
P1[5]	156	A17	B13	-	[3]	I; PU	I/O	**P1[5] —** General purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							O	**SD_PWR —** Power Supply Enable for external SD card power supply.
							O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
P1[6]	171	B11	B10	-	[3]	I; PU	I/O	**P1[6] —** General purpose digital input/output pin.
							I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
							I/O	**SD_DAT[0] —** Data line 0 for SD card interface.
							O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
P1[7]	153	D14	C13	-	[3]	I; PU	I/O	**P1[7] —** General purpose digital input/output pin.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							I/O	**SD_DAT[1] —** Data line 1 for SD card interface.
							O	**PWM0[5] —** Pulse Width Modulator 0, output 5.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[21]	72	R8	N6	50	[3]	I; PU	I/O	**P1[21] —** General purpose digital input/output pin.
							O	**USB_TX_DM1 —** D− transmit data for USB port 1 (OTG transceiver).
							O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I	**$\overline{\text{MC\_ABORT}}$ —** Motor control PWM, active low fast abort.
							-	**R —** Function reserved.
							O	**LCD_VD[7] —** LCD data.
							O	**LCD_VD[11] —** LCD data.
P1[22]	74	U8	M6	51	[3]	I; PU	I/O	**P1[22] —** General purpose digital input/output pin.
							I	**USB_RCV1 —** Differential receive data for USB port 1 (OTG transceiver).
							I	**USB_PWRD1 —** Power Status for USB port 1 (host power switch).
							O	**T1_MAT0 —** Match output for Timer 1, channel 0.
							O	**MC_0B —** Motor control PWM channel 0, output B.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							O	**LCD_VD[8] —** LCD data.
							O	**LCD_VD[12] —** LCD data.
P1[23]	76	P9	N7	53	[3]	I; PU	I/O	**P1[23] —** General purpose digital input/output pin.
							I	**USB_RX_DP1 —** D+ receive data for USB port 1 (OTG transceiver).
							O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
							I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
							I	**MC_FB1 —** Motor control PWM channel 1 feedback input.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							O	**LCD_VD[9] —** LCD data.
							O	**LCD_VD[13] —** LCD data.
P1[24]	78	T9	P7	54	[3]	I; PU	I/O	**P1[24] —** General purpose digital input/output pin.
							I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).
							O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
							I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
							I	**MC_FB2 —** Motor control PWM channel 2 feedback input.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							O	**LCD_VD[10] —** LCD data.
							O	**LCD_VD[14] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P4[1]	79	U10	M7	55	[3]	I; PU	I/O	**P4[1] —** General purpose digital input/output pin.
							I/O	**EMC_A[1] —** External memory address line 1.
P4[2]	83	T11	M8	58	[3]	I; PU	I/O	**P4[2] —** General purpose digital input/output pin.
							I/O	**EMC_A[2] —** External memory address line 2.
P4[3]	97	U16	K9	68	[3]	I; PU	I/O	**P4[3] —** General purpose digital input/output pin.
							I/O	**EMC_A[3] —** External memory address line 3.
P4[4]	103	R15	P13	72	[3]	I; PU	I/O	**P4[4] —** General purpose digital input/output pin.
							I/O	**EMC_A[4] —** External memory address line 4.
P4[5]	107	R16	H10	74	[3]	I; PU	I/O	**P4[5] —** General purpose digital input/output pin.
							I/O	**EMC_A[5] —** External memory address line 5.
P4[6]	113	M14	K10	78	[3]	I; PU	I/O	**P4[6] —** General purpose digital input/output pin.
							I/O	**EMC_A[6] —** External memory address line 6.
P4[7]	121	L16	K12	84	[3]	I; PU	I/O	**P4[7] —** General purpose digital input/output pin.
							I/O	**EMC_A[7] —** External memory address line 7.
P4[8]	127	J17	J11	88	[3]	I; PU	I/O	**P4[8] —** General purpose digital input/output pin.
							I/O	**EMC_A[8] —** External memory address line 8.
P4[9]	131	H17	H12	91	[3]	I; PU	I/O	**P4[9] —** General purpose digital input/output pin.
							I/O	**EMC_A[9] —** External memory address line 9.
P4[10]	135	G17	G12	94	[3]	I; PU	I/O	**P4[10] —** General purpose digital input/output pin.
							I/O	**EMC_A[10] —** External memory address line 10.
P4[11]	145	F14	F11	101	[3]	I; PU	I/O	**P4[11] —** General purpose digital input/output pin.
							I/O	**EMC_A[11] —** External memory address line 11.
P4[12]	149	C16	F10	104	[3]	I; PU	I/O	**P4[12] —** General purpose digital input/output pin.
							I/O	**EMC_A[12] —** External memory address line 12.
P4[13]	155	B16	B14	108	[3]	I; PU	I/O	**P4[13] —** General purpose digital input/output pin.
							I/O	**EMC_A[13] —** External memory address line 13.
P4[14]	159	B15	E8	110	[3]	I; PU	I/O	**P4[14] —** General purpose digital input/output pin.
							I/O	**EMC_A[14] —** External memory address line 14.
P4[15]	173	A11	C10	120	[3]	I; PU	I/O	**P4[15] —** General purpose digital input/output pin.
							I/O	**EMC_A[15] —** External memory address line 15.
P4[16]	101	U17	N12	-	[3]	I; PU	I/O	**P4[16] —** General purpose digital input/output pin.
							I/O	**EMC_A[16] —** External memory address line 16.
P4[17]	104	P14	N13	-	[3]	I; PU	I/O	**P4[17] —** General purpose digital input/output pin.
							I/O	**EMC_A[17] —** External memory address line 17.
P4[18]	105	P15	P14	-	[3]	I; PU	I/O	**P4[18] —** General purpose digital input/output pin.
							I/O	**EMC_A[18] —** External memory address line 18.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P5[3]	141	G14	G10	98	[11]	I	I/O	**P5[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**U4_RXD —** Receiver input for USART4.
							I/O	**I2C0_SCL —** I^2C0 clock input/output (this pin uses a specialized I^2C pad that supports I^2C Fast Mode Plus).
P5[4]	206	C3	C4	143	[3]	I; PU	I/O	**P5[4] —** General purpose digital input/output pin.
							O	**U0_OE —** RS-485/EIA-485 output enable signal for UART0.
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output for Timer 3, channel 3.
							O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
JTAG_TDO (SWO)	2	D3	B1	1	[3]	O	O	Test Data Out for JTAG interface. Also used as Serial wire trace output.
JTAG_TDI	4	C2	C3	3	[3]	I; PU	I	Test Data In for JTAG interface.
JTAG_TMS (SWDIO)	6	E3	C2	4	[3]	I; PU	I	Test Mode Select for JTAG interface. Also used as Serial wire debug data input/output.
JTAG_$\overline{\text{TRST}}$	8	D1	D4	5	[3]	I; PU	I	Test Reset for JTAG interface.
JTAG_TCK (SWDCLK)	10	E2	D2	7	[3]	i	I	Test Clock for JTAG interface. This clock must be slower than 1/6 of the CPU clock (CCLK) for the JTAG interface to operate. Also used as serial wire clock.
$\overline{\text{RESET}}$	35	M2	J1	24	[12]	I; PU	I	External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
$\overline{\text{RSTOUT}}$	29	K3	H2	20	[3]	OH	O	Reset status output. A LOW output on this pin indicates that the device is in the reset state for any reason. This reflects the $\overline{\text{RESET}}$ input pin and all internal reset sources.
RTC_ALARM	37	N1	H5	26	[13]	OL	O	RTC controlled output. This pin has a low drive strength and is powered by VBAT. It is driven HIGH when an RTC alarm is generated.
RTCX1	34	K2	J2	23	[14] [15]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	36	L2	J3	25	[14] [15]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
USB_D−2	52	U1	N2	37	[9]	-	I/O	USB port 2 bidirectional D− line.

Table 4. Pin allocation table TFBGA208

Not all functions are available on all parts. See Table 2 and Table 7 (EMC pins).

Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol
13	P1[28]	14	P0[1]	15	P0[10]	16	P2[13]
17	P2[11]		-		-		-
Row U							
1	USB_D-2	2	P3[25]	3	P2[18]	4	P0[29]
5	P2[23]	6	P1[19]	7	P1[20]	8	P1[22]
9	P4[0]	10	P4[1]	11	P2[21]	12	P2[22]
13	$V_{DD(3V3)}$	14	P1[29]	15	P0[0]	16	P4[3]
17	P4[16]		-		-		-

Table 5. Pin allocation table TFBGA180

Not all functions are available on all parts. See Table 2 and Table 7 (EMC pins).

Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol
Row A							
5	P1[1]	6	P3[8]	7	P1[10]	8	P1[15]
9	P1[3]	10	V_{SSREG}	11	P0[4]	12	P1[11]
13	P0[9]	14	P1[12]		-		-
Row B							
1	JTAG_TDO (SWO)	2	P3[11]	3	P3[10]	4	V_{SS}
5	P1[0]	6	P1[8]	7	P1[2]	8	P1[16]
9	P4[29]	10	P1[6]	11	P0[5]	12	P0[7]
13	P1[5]	14	P4[13]		-		-
Row C							
1	P3[13]	2	JTAG_TMS (SWDIO)	3	JTAG_TDI	4	P5[4]
5	$V_{DD(3V3)}$	6	P1[4]	7	P4[30]	8	P4[24]
9	P1[17]	10	P4[15]	11	V_{SS}	12	P0[8]
13	P1[7]	14	P2[1]		-		-
Row D							
1	P0[26]	2	JTAG_TCK (SWDCLK)	3	P3[4]	4	$\overline{\text{JTAG\_TRST}}$
5	P0[2]	6	P3[0]	7	P1[9]	8	P1[14]
9	P4[25]	10	P4[28]	11	P0[6]	12	P2[0]
13	V_{SS}	14	P1[13]		-		-
Row E							
1	P0[24]	2	$V_{DD(3V3)}$	3	P3[5]	4	P0[25]
5	P5[0]	6	P3[1]	7	P4[31]	8	P4[14]
9	$V_{DD(REG)(3V3)}$	10	$V_{DD(3V3)}$	11	P2[2]	12	$V_{DD(3V3)}$
13	P2[3]	14	P2[4]		-		-
Row F							
1	P3[14]	2	V_{DDA}	3	V_{SSA}	4	P3[6]
5	P0[23]	6	-	7	-	8	-
9	-	10	P4[12]	11	P4[11]	12	P2[5]

- Physical interface:
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

7.15 USB interface

Remark: The USB Device/Host/OTG controller is available on parts LPC1788/87/86/85 and LPC1778/77/76. The USB Device-only controller is available on parts LPC1774.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

Details on typical USB interfacing solutions can be found in Section 14.1.

7.15.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the USB RAM.

7.15.1.1 Features

- Fully compliant with *USB 2.0 Specification* (full speed).
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the LPC178x/7x can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

7.15.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

7.15.2.1 Features

- OHCI compliant.

7.23 I²S-bus serial I/O controllers

The LPC178x/7x contain one I²S-bus interface. The I²S-bus provides a standard communication interface for digital audio applications.

The I²S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S connection has one master, which is always the master, and one slave. The I²S interface on the LPC178x/7x provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.23.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz (16, 22.05, 32, 44.1, 48) kHz.
- Configurable word select period in master mode (separately for I²S input and output).
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S input and I²S output.

7.24 CAN controller and acceptance filters

The LPC178x/7x contain one CAN controller with two channels.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.24.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.

7.34 System control

7.34.1 Reset

Reset has four sources on the LPC178x/7x: the $\overline{\text{RESET}}$ pin, the Watchdog reset, Power-On Reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip Reset by any source, once the operating voltage attains a usable level, starts the Wake-up timer (see description in Section 7.33.3), causing reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.34.2 Brownout detection

The LPC178x/7x include 2-stage monitoring of the voltage on the $V_{DD(REG)(3V3)}$ pins. If this voltage falls below 2.2 V (typical), the BOD asserts an interrupt signal to the Vectored Interrupt Controller. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register.

The second stage of low-voltage detection asserts a reset to inactivate the LPC178x/7x when the voltage on the $V_{DD(REG)(3V3)}$ pins falls below 1.85 V (typical). This reset prevents alteration of the flash as operation of the various elements of the chip would otherwise become unreliable due to low voltage. The BOD circuit maintains this reset down below 1 V, at which point the power-on reset circuitry maintains the overall reset.

Both the 2.2 V and 1.85 V thresholds include some hysteresis. In normal operation, this hysteresis allows the 2.2 V detection to reliably interrupt, or a regularly executed event loop to sense the condition.

7.34.3 Code security (Code Read Protection - CRP)

This feature of the LPC178x/7x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection.

CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.

CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P2[10] pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

8. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail		2.4	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			2.4	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			−0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		−0.5	+4.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP			−0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins		−0.5	+5.1	V
V_I	input voltage	5 V tolerant digital I/O pins; $V_{DD(3V3)} \geq 2.4V$	[2]	−0.5	+5.5	V
		$V_{DD(3V3)} = 0$ V		−0.5	+3.6	V
		other I/O pins	[2][3]	−0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[4]	−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[5]	-	4000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on the required shelf lifetime. Please refer to the JEDEC spec for further details.

[5] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

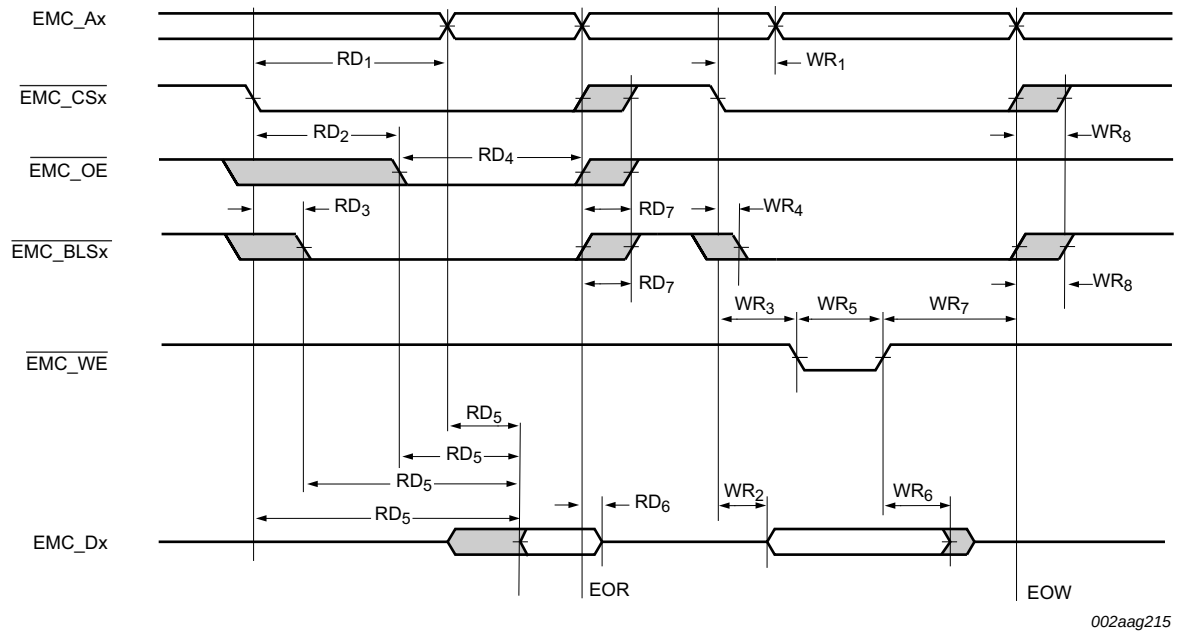


Fig 17. External static memory read/write access (PB =1)

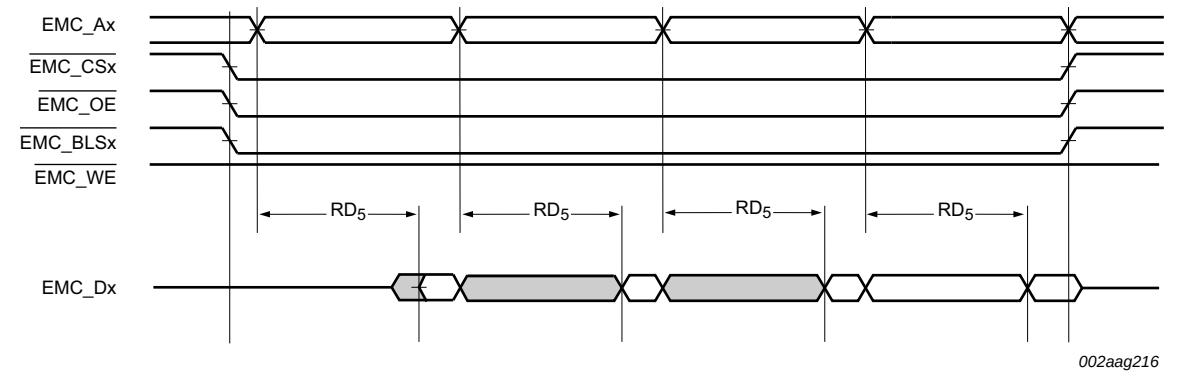


Fig 18. External static memory burst read cycle

11.6 SSP interface

Table 26. Dynamic characteristics: SSP pins in SPI mode

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions		Min	Max	Unit
SSP master						
$T_{cy(clk)}$	clock cycle time	full-duplex mode	[1]	30	-	ns
		when only transmitting		30	-	ns
t_{DS}	data set-up time	in SPI mode	[2]	14.8	-	ns
t_{DH}	data hold time	in SPI mode	[2]	2	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2]	-	6.3	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2]	−2.4	-	ns
SSP slave						
$T_{cy(clk)}$	clock cycle time		[3]	100	-	ns
t_{DS}	data set-up time	in SPI mode	[3][4]	14.8	-	ns
t_{DH}	data hold time	in SPI mode	[3][4]	2	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[3][4]	-	$3*T_{cy(PCLK)} + 6.3$	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[3][4]	−2.4	-	ns

[1] The minimum clock cycle time, and therefore the maximum frequency of the SSP in master mode, is limited by the pin electronics to the value given. The SSP block should not be configured to generate a clock faster than that. At and below the maximum frequency, $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. 5The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency f_{main}, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] T_{amb} = −40 °C to 85 °C; $V_{DD(3V3)}$ = 3.0 V to 3.6 V.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$. The maximum clock rate in slave mode is 1/12th of the PCLK rate.

[4] T_{amb} = 25 °C; $V_{DD(3V3)}$ = 3.3 V.

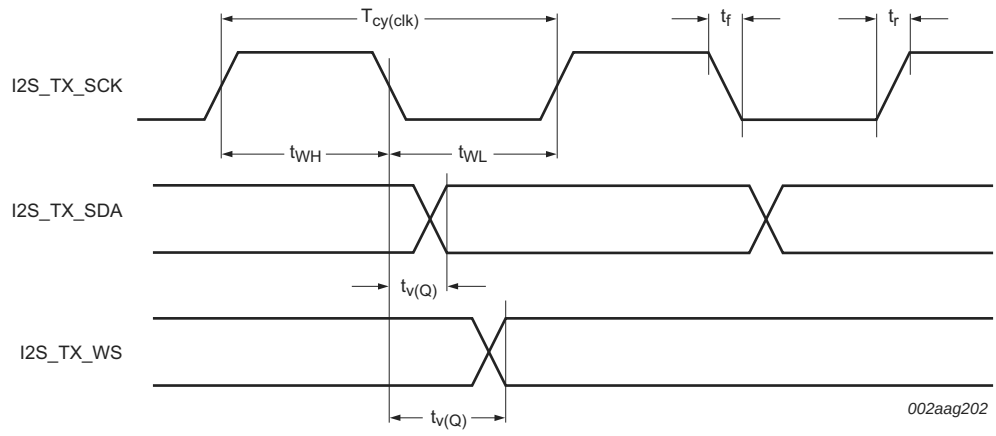


Fig 24. I²S-bus timing (transmit)

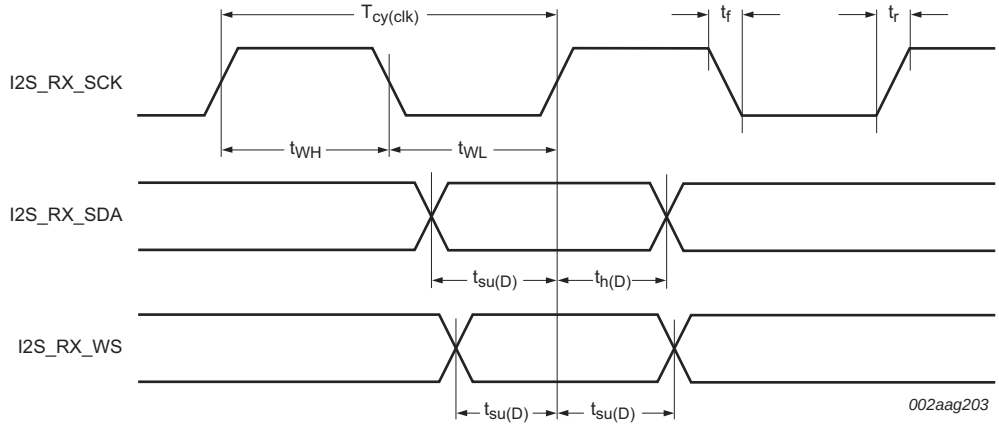


Fig 25. I²S-bus timing (receive)

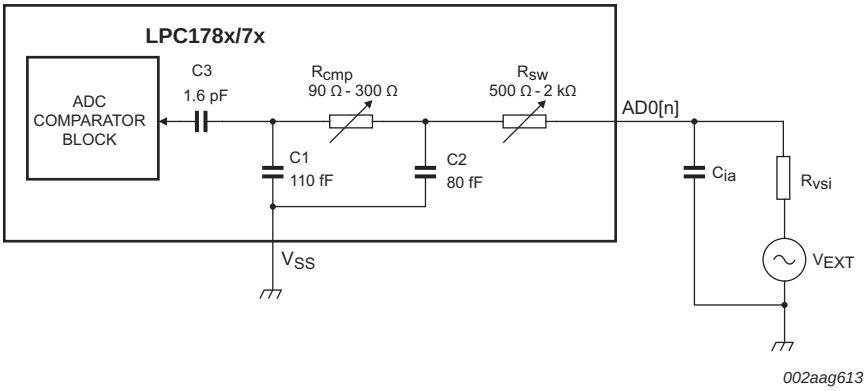
11.9 LCD

Remark: The LCD controller is available on parts LPC1788/87/86/85.

Table 29. Dynamic characteristics: LCD

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin LCD_DCLK	-	50	MHz
$t_{d(QV)}$	data output valid delay time		-	9	ns
$t_{h(Q)}$	data output hold time		−0.5	-	ns



The values of resistor components R_{cmp} and R_{sw} vary with temperature and input voltage and are process-dependent.

Fig 29. ADC interface to pins ADC0_IN[n]

Table 32. ADC interface components

Component	Range	Description
R_{cmp}	90 Ω to 300 Ω	Switch-on resistance for the comparator input switch. Varies with temperature, input voltage, and process.
R_{sw}	500 Ω to 2 kΩ	Switch-on resistance for channel selection switch. Varies with temperature, input voltage, and process.
C1	110 fF	Parasitic capacitance from the ADC block level.
C2	80 fF	Parasitic capacitance from the ADC block level.
C3	1.6 pF	Sampling capacitor.

13. DAC electrical characteristics

Table 33. 10-bit DAC electrical characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
E_D	differential linearity error	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity	-	±1.5	-	LSB
E_O	offset error	-	0.6	-	%
E_G	gain error	-	0.6	-	%
C_L	load capacitance	-	-	200	pF
R_L	load resistance	1	-	-	kΩ

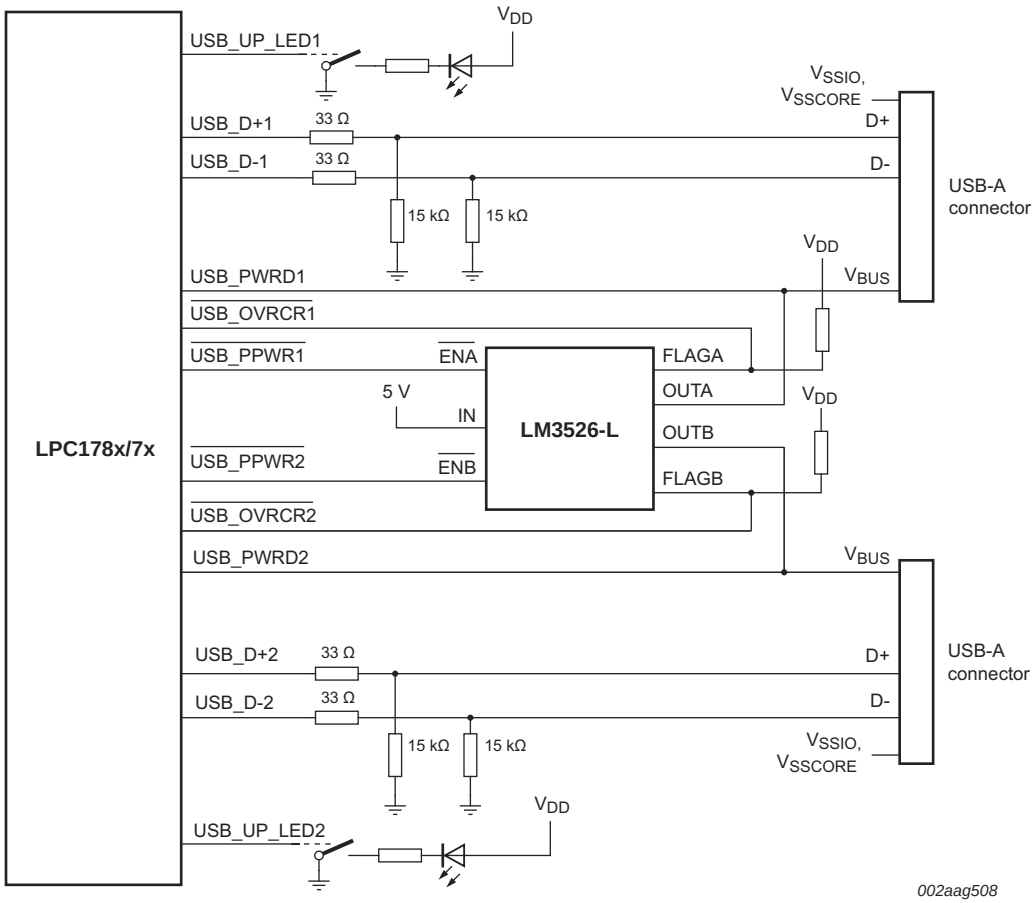
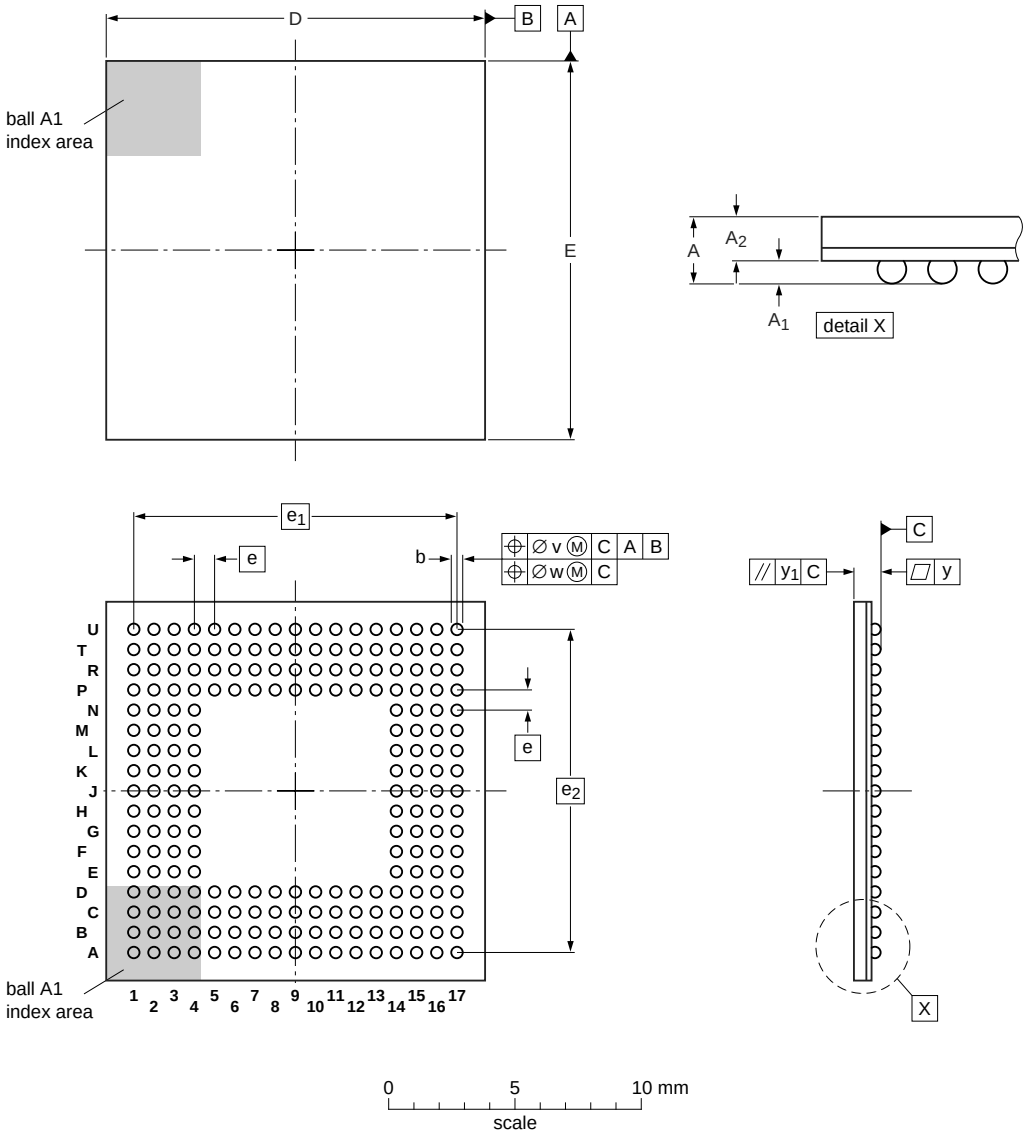


Fig 34. USB host port configuration: port 1 and port 2 as hosts

TFBGA208: plastic thin fine-pitch ball grid array package; 208 balls; body 15 x 15 x 0.7 mm **SOT950-1**



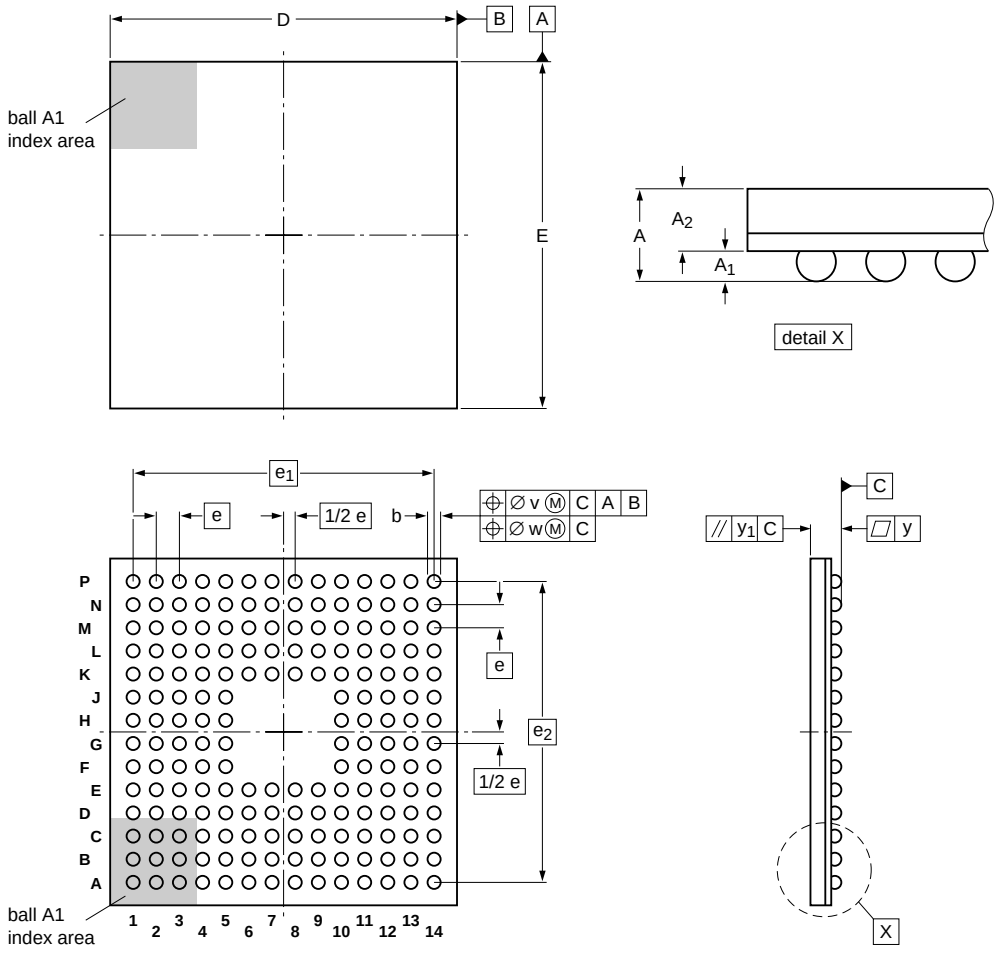
DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.6	0.5 0.4	15.1 14.9	15.1 14.9	0.8	12.8	12.8	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT950-1		- - -				~~06-06-01~~ 06-06-14

Fig 42. TFBGA208 package

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



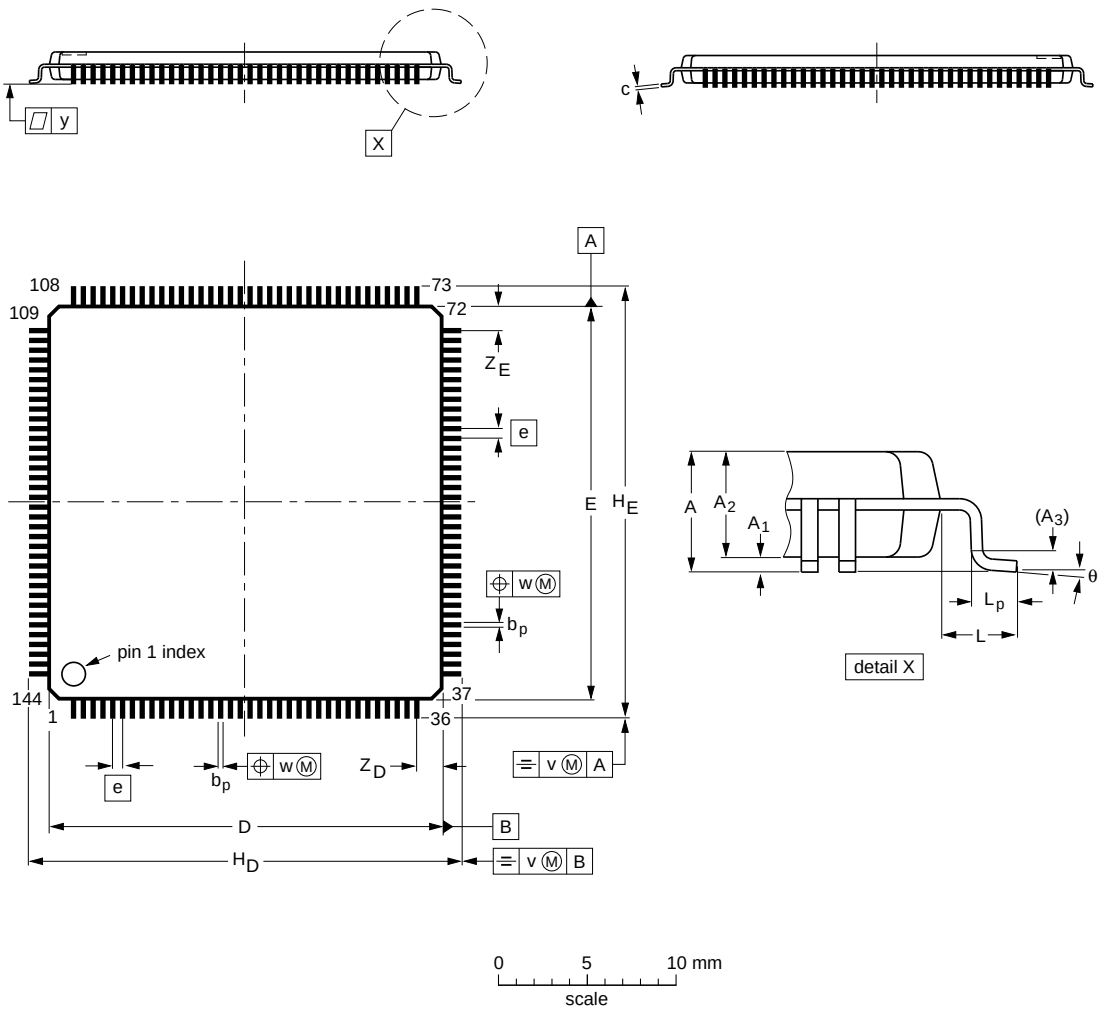
DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 43. TFBGA180 package

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 44. LQFP144 package

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC178X_7X v.3	20111220	Objective data sheet	-	LPC178X_7X v.2
Modifications:	• Removed BOOT function from pin P3[14]. • I_{BAT} and $I_{DD(REG)(3V3)}$ updated for Deep power-down mode in Table 13. • Maximum SDRAM clock of 80 MHz specified in Section 2, Table 18, and Table 19. • Power consumption data added (Figure 9 and Figure 10). • Removed parameter Z_{DRV} in Table 13. • Specified maximum value for parameter C_L in Table 33 and remove typical value. • Specified setting of boost bits in Table 14, Table note 5 and in Table 13, Table note 6 . • USB connection diagrams updated (Figure 33 to Figure 36). • Current drain condition on battery supply specified in Section 7.33.6. • Table note 10 in Table 13 updated. • ADC characteristics updated (Table 31). • Section 14.6 “Reset pin configuration for RTC operation” added. • EEPROM size for parts LPC1774 corrected in Table 2 and Figure 1. • Changed function LCD_VD[5] on pin P0[10] to Reserved. • Changed function LCD_VD[10] on pin P0[11] to Reserved. • Changed function LCD_VD[13] on pin P0[19] to Reserved. • Changed function LCD_VD[14] on pin P0[20] to Reserved. • ADC interface model updated (see Table 32 and Figure 30).			
LPC178X_7X v.2	20110527	Objective data sheet	-	LPC178X_7X v.1
Modifications:	• Symbol names in Table 3 to Table 5 abbreviated. • Reserved functions added in Table 3. • Added function LCD_VD[5] to pin P0[10]. • Added function LCD_VD[10] to pin P0[11]. • Added function LCD_VD[13] to pin P0[19]. • Added function LCD_VD[14] to pin P0[20]. • Added function U4_SCLK to pin P0[21]. • Added function • Added function MOSI to pin P5[0]. • Added function SSP2_MISO to pin P5[1]. • Added EMC dynamic characteristics.			
LPC178X_7X v.1	20110524	Objective data sheet	-	-