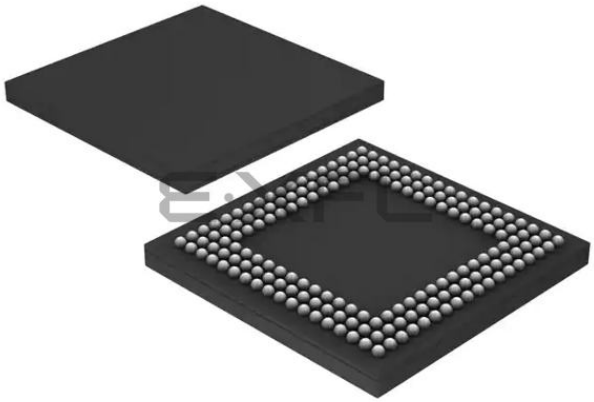

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 141 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 96K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 3.6V |
| Data Converters | A/D 8x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 180-TFBGA |
| Supplier Device Package | 180-TFBGA (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1778fet180-551 |

- Multilayer AHB matrix interconnect provides a separate bus for each AHB master. AHB masters include the CPU, USB, Ethernet, and the General Purpose DMA controller. This interconnect provides communication with no arbitration delays unless two masters attempt to access the same slave at the same time.
- Split APB bus allows for higher throughput with fewer stalls between the CPU and DMA. A single level of write buffering allows the CPU to continue without waiting for completion of APB writes if the APB was not already busy.
- Cortex-M3 system tick timer, including an external clock input option.
- Standard JTAG test/debug interface as well as Serial Wire Debug and Serial WireTrace Port options.
- Embedded Trace Macrocell (ETM) module supports real-time trace.
- Boundary scan for simplified board testing.
- Non-maskable Interrupt (NMI) input.

- Memory:
  - Up to 512 kB on-chip flash program memory with In-System Programming (ISP) and In-Application Programming (IAP) capabilities. The combination of an enhanced flash memory accelerator and location of the flash memory on the CPU local code/data bus provides high code performance from flash.
  - Up to 96 kB on-chip SRAM includes:

    64 kB of main SRAM on the CPU with local code/data bus for high-performance CPU access.

    Two 16 kB peripheral SRAM blocks with separate access paths for higher throughput. These SRAM blocks may be used for DMA memory as well as for general purpose instruction and data storage.
  - Up to 4032 byte on-chip EEPROM.
- LCD controller, supporting both Super-Twisted Nematic (STN) and Thin-Film Transistors (TFT) displays.
  - Dedicated DMA controller.
  - Selectable display resolution (up to 1024 $\times$ 768 pixels).
  - Supports up to 24-bit true-color mode.
- External Memory Controller (EMC) provides support for asynchronous static memory devices such as RAM, ROM and flash, as well as dynamic memories such as single data rate SDRAM with an SDRAM clock of up to 80 MHz.
- Eight channel General Purpose DMA controller (GPDMA) on the AHB multilayer matrix that can be used with the SSP, I2S, UART, CRC engine, Analog-to-Digital and Digital-to-Analog converter peripherals, timer match signals, GPIO, and for memory-to-memory transfers.
- Serial interfaces:
  - Ethernet MAC with MII/RMII interface and associated DMA controller. These functions reside on an independent AHB.
  - USB 2.0 full-speed dual-port device/host/OTG controller with on-chip PHY and associated DMA controller.
  - Five UARTs with fractional baud rate generation, internal FIFO, DMA support, and RS-485/EIA-485 support. One UART (UART1) has full modem control I/O, and one UART (USART4) supports IrDA, synchronous mode, and a smart card mode conforming to ISO7816-3.
  - Three SSP controllers with FIFO and multi-protocol capabilities. The SSP controllers can be used with the GPDMA.

- The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, PORT0/2 pin interrupt, and NMI).
- Brownout detect with separate threshold for interrupt and forced reset.
- On-chip Power-On Reset (POR).

- Clock generation:
  - Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, USB clock, or the watchdog timer clock.
  - On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC oscillator (IRC) trimmed to 1% accuracy that can optionally be used as a system clock.
  - An on-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator or the internal RC oscillator.
  - A second, dedicated PLL may be used for USB interface in order to allow added flexibility for the Main PLL settings.
- Versatile pin function selection feature allows many possibilities for using on-chip peripheral functions.
- Unique device serial number for identification purposes.
- Single 3.3 V power supply (2.4 V to 3.6 V). Temperature range of −40 °C to 85 °C.
- Available as LQFP208, TFBGA208, TFBGA180, and LQFP144 package.

## 3. Applications

- Communications:
  - Point-of-sale terminals, web servers, multi-protocol bridges
- Industrial/Medical:
  - Automation controllers, application control, robotics control, HVAC, PLC, inverters, circuit breakers, medical scanning, security monitoring, motor drive, video intercom
- Consumer/Appliance:
  - Audio, MP3 decoders, alarm systems, displays, printers, scanners, small appliances, fitness equipment
- Automotive:
  - After-market, car alarms, GPS/fleet monitors

**Table 2. LPC178x/7x ordering options**

*All parts include two CAN channels, three SSP interfaces, three $I^2C$ interfaces, one $I^2S$ interface, DAC, and an 8-channel 12-bit ADC.*

| Type number | Device order part number | Flash (kB) | Main SRAM (kB) | Peripheral SRAM (kB) | Total SRAM (kB) | EEPROM (byte) | Ethernet | USB | UART | EMC bus width (bit) [1] | GPIO | LCD | QEI | SD/ MMC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **LPC178x** | | | | | | | | | | | | | | |
| LPC1788FBD208 | LPC1788FBD208/CP3E | 512 | 64 | 16 × 2 | 96 | 4032 | Y | H/O/D | 5 | 32 | 165 | Y | Y | Y |
| LPC1788FET208 | LPC1788FET208,551 | 512 | 64 | 16 × 2 | 96 | 4032 | Y | H/O/D | 5 | 32 | 165 | Y | Y | Y |
| LPC1788FET180 | LPC1788FET180,551 | 512 | 64 | 16 × 2 | 96 | 4032 | Y | H/O/D | 5 | 16 | 141 | Y | Y | Y |
| LPC1788FBD144 | LPC1788FBD144,551 | 512 | 64 | 16 × 2 | 96 | 4032 | Y | H/O/D | 5 | 8 | 109 | Y | Y | Y |
| LPC1787FBD208 | LPC1787FBD208,551 | 512 | 64 | 16 × 2 | 96 | 4032 | N | H/O/D | 5 | 32 | 165 | Y | Y | Y |
| LPC1786FBD208 | LPC1786FBD208,551 | 256 | 64 | 16 | 80 | 4032 | Y | H/O/D | 5 | 32 | 165 | Y | Y | Y |
| LPC1785FBD208 | LPC1785FBD208K | 256 | 64 | 16 | 80 | 4032 | N | H/O/D | 5 | 32 | 165 | Y | N | Y |
| **LPC177x** | | | | | | | | | | | | | | |
| LPC1778FBD208 | LPC1778FBD208,551 | 512 | 64 | 16 × 2 | 96 | 4032 | Y | H/O/D | 5 | 32 | 165 | N | Y | Y |
| LPC1778FET208 | LPC1778FET208,551 | 512 | 64 | 16 × 2 | 96 | 4032 | Y | H/O/D | 5 | 32 | 165 | N | Y | Y |
| LPC1778FET180 | LPC1778FET180,551 | 512 | 64 | 16 × 2 | 96 | 4032 | Y | H/O/D | 5 | 16 | 141 | N | Y | Y |
| LPC1778FBD144 | LPC1778FBD144,551 | 512 | 64 | 16 × 2 | 96 | 4032 | Y | H/O/D | 5 | 8 | 109 | N | Y | Y |
| LPC1777FBD208 | LPC1777FBD208,551 | 512 | 64 | 16 × 2 | 96 | 4032 | N | H/O/D | 5 | 32 | 165 | N | Y | Y |
| LPC1776FBD208 | LPC1776FBD208,551 | 256 | 64 | 16 | 80 | 4032 | Y | H/O/D | 5 | 32 | 165 | N | Y | Y |
| LPC1776FET180 | LPC1776FET180,551 | 256 | 64 | 16 | 80 | 4032 | Y | H/O/D | 5 | 16 | 141 | N | Y | Y |
| LPC1774FBD208 | LPC1774FBD208,551 | 128 | 32 | 8 | 40 | 2048 | N | D | 5 | 32 | 165 | N | N | N |
| LPC1774FBD144 | LPC1774FBD144,551 | 128 | 32 | 8 | 40 | 2048 | N | D | 4[2] | 8 | 109 | N | N | N |

[1] Maximum data bus width of the External Memory Controller (EMC) depends on package size. Smaller widths may be used.

[2] USART4 not available.

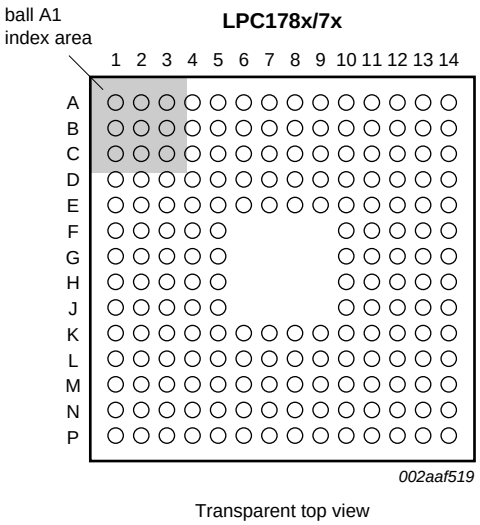



**Fig 4. Pin configuration (TFBGA180)**

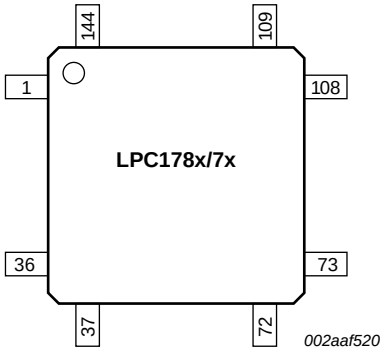



**Fig 5. Pin configuration (LQFP144)**

## 6.2 Pin description

I/O pins on the LPC178x/7x are 5 V tolerant and have input hysteresis unless otherwise indicated in the table below. Crystal pins, power pins, and reference voltage pins are not 5 V tolerant. In addition, when pins are selected to be ADC inputs, they are no longer 5 V tolerant and the input voltage must be limited to the voltage at the ADC positive reference pin (VREFP).

All port pins Pn[m] are multiplexed, and the multiplexed functions appear in Table 3 in the order defined by the FUNC bits of the corresponding IOCON register up to the highest used function number. Each port pin can support up to eight multiplexed functions. IOCON register FUNC values which are reserved are noted as ‘R’ in the pin configuration table.

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| P1[8] | 190 | C7 | B6 | 132 | [3] | I; PU | I/O | **P1[8] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_CRS (ENET_CRS_DV) —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT1 —** Match output for Timer 3, channel 1. |
| | | | | | | | I/O | **SSP2_SSEL —** Slave Select for SSP2. |
| P1[9] | 188 | A6 | D7 | 131 | [3] | I; PU | I/O | **P1[9] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **T3_MAT0 —** Match output for Timer 3, channel 0. |
| P1[10] | 186 | C8 | A7 | 129 | [3] | I; PU | I/O | **P1[10] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T3_CAP0 —** Capture input for Timer 3, channel 0. |
| P1[11] | 163 | A14 | A12 | - | [3] | I; PU | I/O | **P1[11] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RXD2 —** Ethernet Receive Data 2 (MII interface). |
| | | | | | | | I/O | **SD_DAT[2] —** Data line 2 for SD card interface. |
| | | | | | | | O | **PWM0[6] —** Pulse Width Modulator 0, output 6. |
| P1[12] | 157 | A16 | A14 | - | [3] | I; PU | I/O | **P1[12] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RXD3 —** Ethernet Receive Data (MII interface). |
| | | | | | | | I/O | **SD_DAT[3] —** Data line 3 for SD card interface. |
| | | | | | | | I | **PWM0_CAP0 —** Capture input for PWM0, channel 0. |
| P1[13] | 147 | D16 | D14 | - | [3] | I; PU | I/O | **P1[13] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RX_DV —** Ethernet Receive Data Valid (MII interface). |
| P1[14] | 184 | A7 | D8 | 128 | [3] | I; PU | I/O | **P1[14] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RX_ER —** Ethernet receive error (RMII/MII interface). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **T2_CAP0 —** Capture input for Timer 2, channel 0. |
| P1[15] | 182 | A8 | A8 | 126 | [3] | I; PU | I/O | **P1[15] —** General purpose digital input/output pin. |
| | | | | | | | I | **ENET_RX_CLK (ENET_REF_CLK) —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface). |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I/O | **I2C2_SDA —** $I^2C2$ data input/output (this pin does not use a specialized I2C pad). |

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| P1[25] | 80 | T10 | L7 | 56 | [3] | I; PU | I/O | **P1[25] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB_LS1 —** Low Speed status for USB port 1 (OTG transceiver). |
| | | | | | | | O | **USB_HSTEN1 —** Host Enabled status for USB port 1. |
| | | | | | | | O | **T1_MAT1 —** Match output for Timer 1, channel 1. |
| | | | | | | | O | **MC_1A —** Motor control PWM channel 1, output A. |
| | | | | | | | O | **CLKOUT —** Selectable clock output. |
| | | | | | | | O | **LCD_VD[11] —** LCD data. |
| | | | | | | | O | **LCD_VD[15] —** LCD data. |
| P1[26] | 82 | R10 | P8 | 57 | [3] | I; PU | I/O | **P1[26] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB_SSPND1 —** USB port 1 Bus Suspend status (OTG transceiver). |
| | | | | | | | O | **PWM1[6] —** Pulse Width Modulator 1, channel 6 output. |
| | | | | | | | I | **T0_CAP0 —** Capture input for Timer 0, channel 0. |
| | | | | | | | O | **MC_1B —** Motor control PWM channel 1, output B. |
| | | | | | | | I/O | **SSP1_SSEL —** Slave Select for SSP1. |
| | | | | | | | O | **LCD_VD[12] —** LCD data. |
| | | | | | | | O | **LCD_VD[20] —** LCD data. |
| P1[27] | 88 | T12 | M9 | 61 | [3] | I; PU | I/O | **P1[27] —** General purpose digital input/output pin. |
| | | | | | | | I | **USB_INT1 —** USB port 1 OTG transceiver interrupt (OTG transceiver). |
| | | | | | | | I | **USB_OVRCR1 —** USB port 1 Over-Current status. |
| | | | | | | | I | **T0_CAP1 —** Capture input for Timer 0, channel 1. |
| | | | | | | | O | **CLKOUT —** Selectable clock output. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_VD[13] —** LCD data. |
| | | | | | | | O | **LCD_VD[21] —** LCD data. |
| P1[28] | 90 | T13 | P10 | 63 | [3] | I; PU | I/O | **P1[28] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **USB_SCL1 —** USB port 1 $I^2C$ serial clock (OTG transceiver). |
| | | | | | | | I | **PWM1_CAP0 —** Capture input for PWM1, channel 0. |
| | | | | | | | O | **T0_MAT0 —** Match output for Timer 0, channel 0. |
| | | | | | | | O | **MC_2A —** Motor control PWM channel 2, output A. |
| | | | | | | | I/O | **SSP0_SSEL —** Slave Select for SSP0. |
| | | | | | | | O | **LCD_VD[14] —** LCD data. |
| | | | | | | | O | **LCD_VD[22] —** LCD data. |

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| P2[9] | 132 | H16 | H11 | 92 | [3] | I; PU | I/O | **P2[9] —** General purpose digital input/output pin. |
| | | | | | | | O | **USB_CONNECT1 —** USB1 SoftConnect control. Signal used to switch an external 1.5 kΩ resistor under the software control. Used with the SoftConnect USB feature. |
| | | | | | | | I | **U2_RXD —** Receiver input for UART2. |
| | | | | | | | I | **U4_RXD —** Receiver input for USART4. |
| | | | | | | | I/O | **ENET_MDIO —** Ethernet MIIM data input and output. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | I | **LCD_VD[3] —** LCD data. |
| | | | | | | | I | **LCD_VD[7] —** LCD data. |
| P2[10] | 110 | N15 | M13 | 76 | [10] | I; PU | I/O | **P2[10] —** General purpose digital input/output pin. This pin includes a 10 ns input .<br>A LOW on this pin while $\overline{\text{RESET}}$ is LOW forces the on-chip boot loader to take over control of the part after a reset and go into ISP mode. |
| | | | | | | | I | **$\overline{\text{EINT0}}$ —** External interrupt 0 input. |
| | | | | | | | I | **NMI —** Non-maskable interrupt input. |
| P2[11] | 108 | T17 | M12 | 75 | [10] | I; PU | I/O | **P2[11] —** General purpose digital input/output pin. This pin includes a 10 ns input glitch filter. |
| | | | | | | | I | **$\overline{\text{EINT1}}$ —** External interrupt 1 input. |
| | | | | | | | I/O | **SD_DAT[1] —** Data line 1 for SD card interface. |
| | | | | | | | I/O | **I2S_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *$I^2S$-bus specification*. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | - | **R —** Function reserved. |
| | | | | | | | O | **LCD_CLKIN —** LCD clock. |
| P2[12] | 106 | N14 | N14 | 73 | [10] | I; PU | I/O | **P2[12] —** General purpose digital input/output pin. This pin includes a 10 ns input glitch filter. |
| | | | | | | | I | **$\overline{\text{EINT2}}$ —** External interrupt 2 input. |
| | | | | | | | I/O | **SD_DAT[2] —** Data line 2 for SD card interface. |
| | | | | | | | I/O | **I2S_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *$I^2S$-bus specification*. |
| | | | | | | | O | **LCD_VD[4] —** LCD data. |
| | | | | | | | O | **LCD_VD[3] —** LCD data. |
| | | | | | | | O | **LCD_VD[8] —** LCD data. |
| | | | | | | | O | **LCD_VD[18] —** LCD data. |

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| P3[17] | 143 | F15 | - | - | [3] | I; PU | I/O | **P3[17] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[17] —** External memory data line 17. |
| | | | | | | | O | **PWM0[2] —** Pulse Width Modulator 0, output 2. |
| | | | | | | | I | **U1_RXD —** Receiver input for UART1. |
| P3[18] | 151 | C15 | - | - | [3] | I; PU | I/O | **P3[18] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[18] —** External memory data line 18. |
| | | | | | | | O | **PWM0[3] —** Pulse Width Modulator 0, output 3. |
| | | | | | | | I | **U1_CTS —** Clear to Send input for UART1. |
| P3[19] | 161 | B14 | - | - | [3] | I; PU | I/O | **P3[19] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[19] —** External memory data line 19. |
| | | | | | | | O | **PWM0[4] —** Pulse Width Modulator 0, output 4. |
| | | | | | | | I | **U1_DCD —** Data Carrier Detect input for UART1. |
| P3[20] | 167 | A13 | - | - | [3] | I; PU | I/O | **P3[20] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[20] —** External memory data line 20. |
| | | | | | | | O | **PWM0[5] —** Pulse Width Modulator 0, output 5. |
| | | | | | | | I | **U1_DSR —** Data Set Ready input for UART1. |
| P3[21] | 175 | C10 | - | - | [3] | I; PU | I/O | **P3[21] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[21] —** External memory data line 21. |
| | | | | | | | O | **PWM0[6] —** Pulse Width Modulator 0, output 6. |
| | | | | | | | O | **U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1. |
| P3[22] | 195 | C6 | - | - | [3] | I; PU | I/O | **P3[22] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[22] —** External memory data line 22. |
| | | | | | | | I | **PWM0_CAP0 —** Capture input for PWM0, channel 0. |
| | | | | | | | I | **U1_RI —** Ring Indicator input for UART1. |
| P3[23] | 65 | T6 | M4 | 45 | [3] | I; PU | I/O | **P3[23] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[23] —** External memory data line 23. |
| | | | | | | | I | **PWM1_CAP0 —** Capture input for PWM1, channel 0. |
| | | | | | | | I | **T0_CAP0 —** Capture input for Timer 0, channel 0. |
| P3[24] | 58 | R5 | N3 | 40 | [3] | I; PU | I/O | **P3[24] —** General purpose digital input/output pin. |
| | | | | | | | I/O | **EMC_D[24] —** External memory data line 24. |
| | | | | | | | O | **PWM1[1] —** Pulse Width Modulator 1, output 1. |
| | | | | | | | I | **T0_CAP1 —** Capture input for Timer 0, channel 1. |

**Table 3. Pin description** *…continued*

*Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).*

| Symbol | Pin LQFP208 | Ball TFBGA208 | Ball TFBGA180 | Pin LQFP144 | | Reset state[1] | Type[2] | Description |
|---|---|---|---|---|---|---|---|---|
| VBAT | 38 | M3 | K1 | 27 | | - | I | RTC power supply: 3.0 V on this pin supplies power to the RTC. |
| $V_{DD(REG)(3V3)}$ | 26, 86, 174 | H4, P11, D11 | G1, N9, E9 | 18, 60, 121 | | - | S | 3.3 V regulator supply voltage: This is the power supply for the on-chip voltage regulator that supplies internal logic. |
| $V_{DDA}$ | 20 | G4 | F2 | 14 | | - | S | Analog 3.3 V pad supply voltage: This can be connected to the same supply as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC. **Note: This pin should be tied to 3.3 V if the ADC and DAC are not used.** |
| $V_{DD(3V3)}$ | 15, 60, 71, 89, 112, 125, 146, 165, 181, 198 | G3, P6, P8, U13, P17, K16, C17, B13, C9, D7 | E2, L4, K8, L11, J14, E12, E10, C5 | 41, 62, 77, 102, 114, 138 | | - | S | 3.3 V supply voltage: This is the power supply voltage for I/O other than pins in the VBAT domain. |
| VREFP | 24 | K1 | G2 | 17 | | - | S | ADC positive reference voltage: This should be the same voltage as $V_{DDA}$, but should be isolated to minimize noise and error. The voltage level on this pin is used as a reference for ADC and DAC. **Note: This pin should be tied to 3.3 V if the ADC and DAC are not used.** |
| $V_{SS}$ | 33, 63, 77, 93, 114, 133, 148, 169, 189, 200 | L3, T5, R9, P12, N16, H14, E15, A12, B6, A2 | H4, P4, L9, L13, G13, D13, C11, B4 | 44, 65, 79, 103, 117, 139 | | - | G | Ground: 0 V reference for digital IO pins. |
| $V_{SSREG}$ | 32, 84, 172 | D12, K4, P10 | H3, L8, A10 | 22, 59, 119 | | - | G | Ground: 0 V reference for internal logic. |
| $V_{SSA}$ | 22 | J2 | F3 | 15 | | - | G | Analog ground: 0 V power supply and reference for the ADC and DAC. This should be the same voltage as $V_{SS}$, but should be isolated to minimize noise and error. |
| XTAL1 | 44 | M4 | L2 | 31 | [14] [16] | - | I | Input to the oscillator circuit and internal clock generator circuits. |
| XTAL2 | 46 | N4 | K4 | 33 | [14] [16] | - | O | Output from the oscillator amplifier. |

during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

### 7.21.1 Features

- Maximum SSP speed of 33 Mbit/s (master) or 10 Mbit/s (slave).
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- 4-bit to 16-bit frame.
- DMA transfers supported by GPDMA.

## 7.22 $I^2C$-bus serial I/O controllers

The LPC178x/7x contain three $I^2C$-bus controllers.

The $I^2C$-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial Data Line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The $I^2C$ is a multi-master bus and can be controlled by more than one bus master connected to it.

### 7.22.1 Features

- All $I^2C$-bus controllers can use standard GPIO pins with bit rates of up to 400 kbit/s (Fast $I^2C$-bus). The $I^2C0$-bus interface uses special open-drain pins with bit rates of up to 400 kbit/s.
- The $I^2C$-bus interface supports Fast-mode Plus with bit rates up to 1 Mbit/s for I2C0 using pins P5[2] and P5[3].
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The $I^2C$-bus can be used for test and diagnostic purposes.
- Both $I^2C$-bus controllers support multiple address recognition and a bus monitor mode.

The alternate PLL accepts an input clock frequency from the main oscillator in the range of 10 MHz to 25 MHz only. When used as the USB clock, the input frequency is multiplied up to a multiple of 48 MHz (192 MHz or 288 MHz as described above).

### 7.33.3 Wake-up timer

The LPC178x/7x begin operation at power-up and when awakened from Power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up Timer.

The wake-up timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

### 7.33.4 Power control

The LPC178x/7x support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, the peripheral power control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.

The LPC178x/7x also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

#### 7.33.4.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(REG)(3V3)}$). Having the on-chip voltage regulator powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly” while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC domain. The RTC operates at very low power, which can be supplied by an external battery. The device core power ($V_{DD(REG)(3V3)}$) is used to operate the RTC whenever $V_{DD(REG)(3V3)}$ is present. There is no power drain from the RTC battery when $V_{DD(REG)(3V3)}$ is at nominal levels and $V_{DD(REG)(3V3)} > V_{BAT}$.

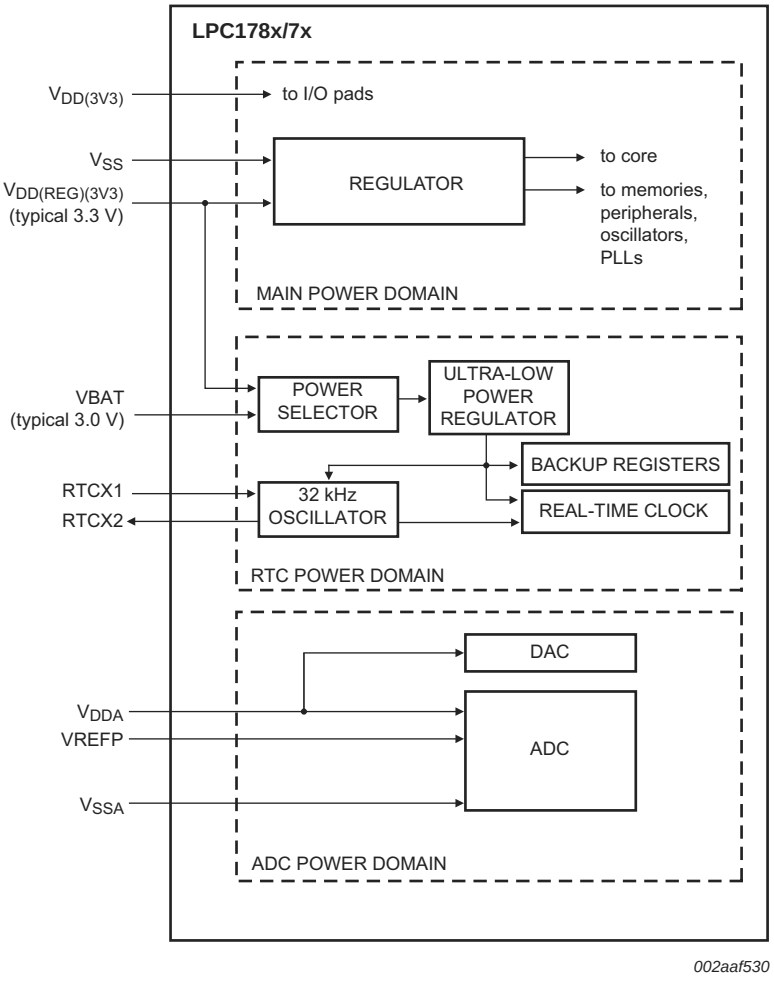
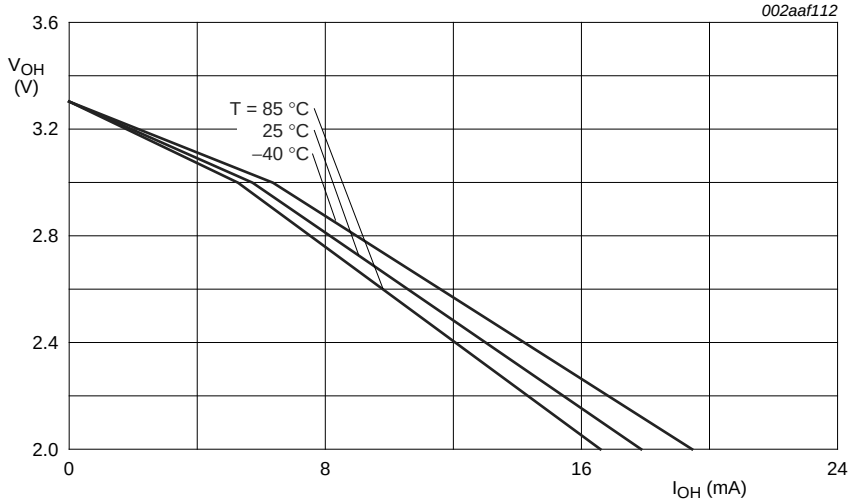


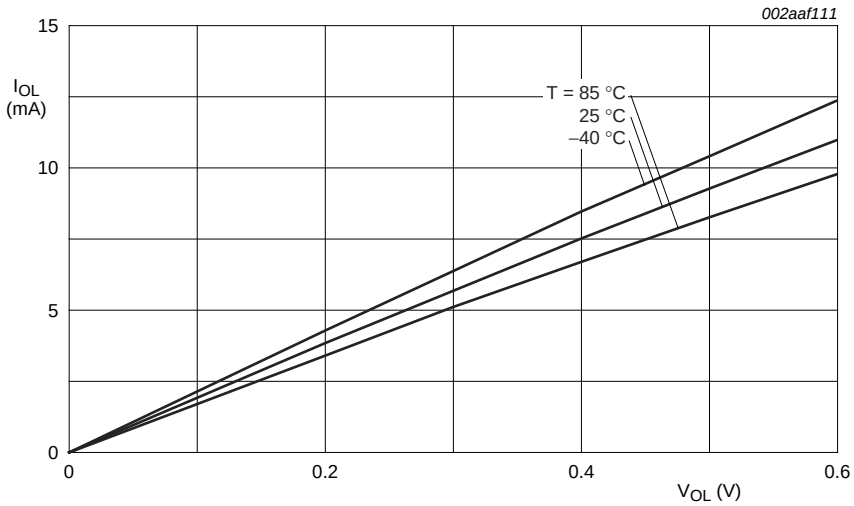

**Fig 8. Power distribution**

## 10.3 Electrical pin characteristics




Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

**Fig 12. Typical HIGH-level output voltage $V_{OH}$ versus HIGH-level output source current $I_{OH}$**




Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

**Fig 13. Typical LOW-level output current $I_{OL}$ versus LOW-level output voltage $V_{OL}$**

## 11.3 External clock

**Table 23. Dynamic characteristic: external clock (see Figure 36)**
*$T_{amb}$ = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{osc}$ | oscillator frequency | 1 | 12 | 25 | MHz |
| $T_{cy(clk)}$ | clock cycle time | 40 | 83.3 | 1000 | ns |
| $t_{CHCX}$ | clock HIGH time | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCX}$ | clock LOW time | $T_{cy(clk)} \times 0.4$ | - | - | ns |
| $t_{CLCH}$ | clock rise time | - | - | 5 | ns |
| $t_{CHCL}$ | clock fall time | - | - | 5 | ns |

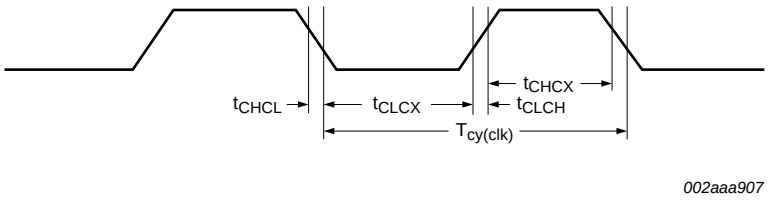



**Fig 20. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)**

## 11.4 Internal oscillators

**Table 24. Dynamic characteristic: internal oscillators**
*$T_{amb}$ = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.*[1]

| Symbol | Parameter | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|
| $f_{osc(RC)}$ | internal RC oscillator frequency | 11.88 | 12 | 12.12 | MHz |
| $f_{i(RTC)}$ | RTC input frequency | - | 32.768 | - | kHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

## 11.5 I/O pins

**Table 25. Dynamic characteristic: I/O pins[1]**
*$C_L$ = 10 pF; $T_{amb}$ = −40 °C to +85 °C; $V_{DD(3V3)}$ = 3.0 V to 3.6 V.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_r$ | rise time | pin configured as output | 3.0 | - | 5.0 | ns |
| $t_f$ | fall time | pin configured as output | 2.5 | - | 5.0 | ns |

[1] Applies to standard port pins.

## 11.6 SSP interface

**Table 26. Dynamic characteristics: SSP pins in SPI mode**

*$C_L$ = 10 pF; $T_{amb}$ = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **SSP master** | | | | | | |
| $T_{cy(clk)}$ | clock cycle time | full-duplex mode | [1] | 30 | - | ns |
| | | when only transmitting | | 30 | - | ns |
| $t_{DS}$ | data set-up time | in SPI mode | [2] | 14.8 | - | ns |
| $t_{DH}$ | data hold time | in SPI mode | [2] | 2 | - | ns |
| $t_{v(Q)}$ | data output valid time | in SPI mode | [2] | - | 6.3 | ns |
| $t_{h(Q)}$ | data output hold time | in SPI mode | [2] | −2.4 | - | ns |
| **SSP slave** | | | | | | |
| $T_{cy(clk)}$ | clock cycle time | | [3] | 100 | - | ns |
| $t_{DS}$ | data set-up time | in SPI mode | [3][4] | 14.8 | - | ns |
| $t_{DH}$ | data hold time | in SPI mode | [3][4] | 2 | - | ns |
| $t_{v(Q)}$ | data output valid time | in SPI mode | [3][4] | - | $3*T_{cy(PCLK)} + 6.3$ | ns |
| $t_{h(Q)}$ | data output hold time | in SPI mode | [3][4] | −2.4 | - | ns |

[1] The minimum clock cycle time, and therefore the maximum frequency of the SSP in master mode, is limited by the pin electronics to the value given. The SSP block should not be configured to generate a clock faster than that. At and below the maximum frequency, $T_{cy(clk)} = (SSPCLKDIV \times (1 + SCR) \times CPSDVSR) / f_{main}$. 5The clock cycle time derived from the SPI bit rate $T_{cy(clk)}$ is a function of the main clock frequency $f_{main}$, the SSP peripheral clock divider (SSPCLKDIV), the SSP SCR parameter (specified in the SSP0CR0 register), and the SSP CPSDVSR parameter (specified in the SSP clock prescale register).

[2] $T_{amb}$ = −40 °C to 85 °C; $V_{DD(3V3)}$ = 3.0 V to 3.6 V.

[3] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$. The maximum clock rate in slave mode is 1/12th of the PCLK rate.

[4] $T_{amb}$ = 25 °C; $V_{DD(3V3)}$ = 3.3 V.

## 11.7 I²C-bus

**Table 27. Dynamic characteristic: I²C-bus pins[1]**
*$T_{amb}$ = −40 °C to +85 °C.[2]*

| Symbol | Parameter | | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | Standard-mode | 0 | 100 | kHz |
| | | | Fast-mode | 0 | 400 | kHz |
| | | | Fast-mode Plus | 0 | 1 | MHz |
| $t_f$ | fall time | [4][5][6][7] | of both SDA and SCL signals<br>Standard-mode | - | 300 | ns |
| | | | Fast-mode | $20 + 0.1 \times C_b$ | 300 | ns |
| | | | Fast-mode Plus | - | 120 | ns |
| $t_{LOW}$ | LOW period of the SCL clock | | Standard-mode | 4.7 | - | µs |
| | | | Fast-mode | 1.3 | - | µs |
| | | | Fast-mode Plus | 0.5 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | Standard-mode | 4.0 | - | µs |
| | | | Fast-mode | 0.6 | - | µs |
| | | | Fast-mode Plus | 0.26 | - | µs |
| $t_{HD;DAT}$ | data hold time | [3][4][8] | Standard-mode | 0 | - | µs |
| | | | Fast-mode | 0 | - | µs |
| | | | Fast-mode Plus | 0 | - | µs |
| $t_{SU;DAT}$ | data set-up time | [9][10] | Standard-mode | 250 | - | ns |
| | | | Fast-mode | 100 | - | ns |
| | | | Fast-mode Plus | 50 | - | ns |

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH}$(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] $C_b$ = total capacitance of one bus line in pF.

[6] The maximum $t_f$ for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage $t_f$ is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified $t_f$.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

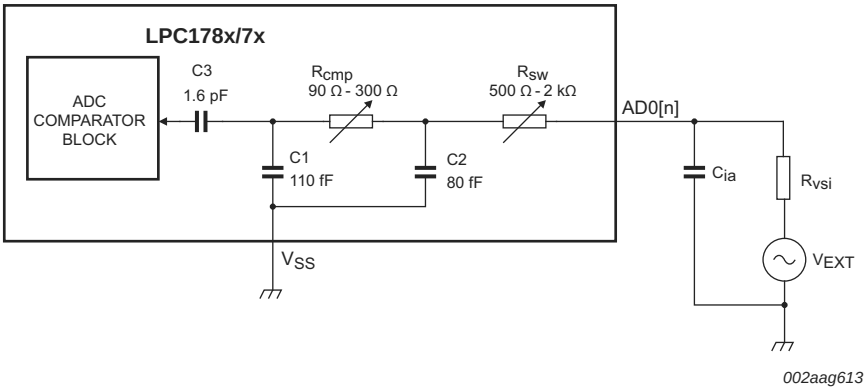
[6] The offset error ($E_O$) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 28.

[7] The gain error ($E_G$) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 28.

[8] The absolute error ($E_T$) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 28.

[9] See Figure 29.

[10] 8-bit resolution is achieved by ignoring the lower four bits of the ADC conversion result.




The values of resistor components $R_{cmp}$ and $R_{sw}$ vary with temperature and input voltage and are process-dependent.

**Fig 29. ADC interface to pins ADC0_IN[n]**

**Table 32. ADC interface components**

| Component | Range | Description |
|---|---|---|
| $R_{cmp}$ | 90 Ω to 300 Ω | Switch-on resistance for the comparator input switch. Varies with temperature, input voltage, and process. |
| $R_{sw}$ | 500 Ω to 2 kΩ | Switch-on resistance for channel selection switch. Varies with temperature, input voltage, and process. |
| C1 | 110 fF | Parasitic capacitance from the ADC block level. |
| C2 | 80 fF | Parasitic capacitance from the ADC block level. |
| C3 | 1.6 pF | Sampling capacitor. |

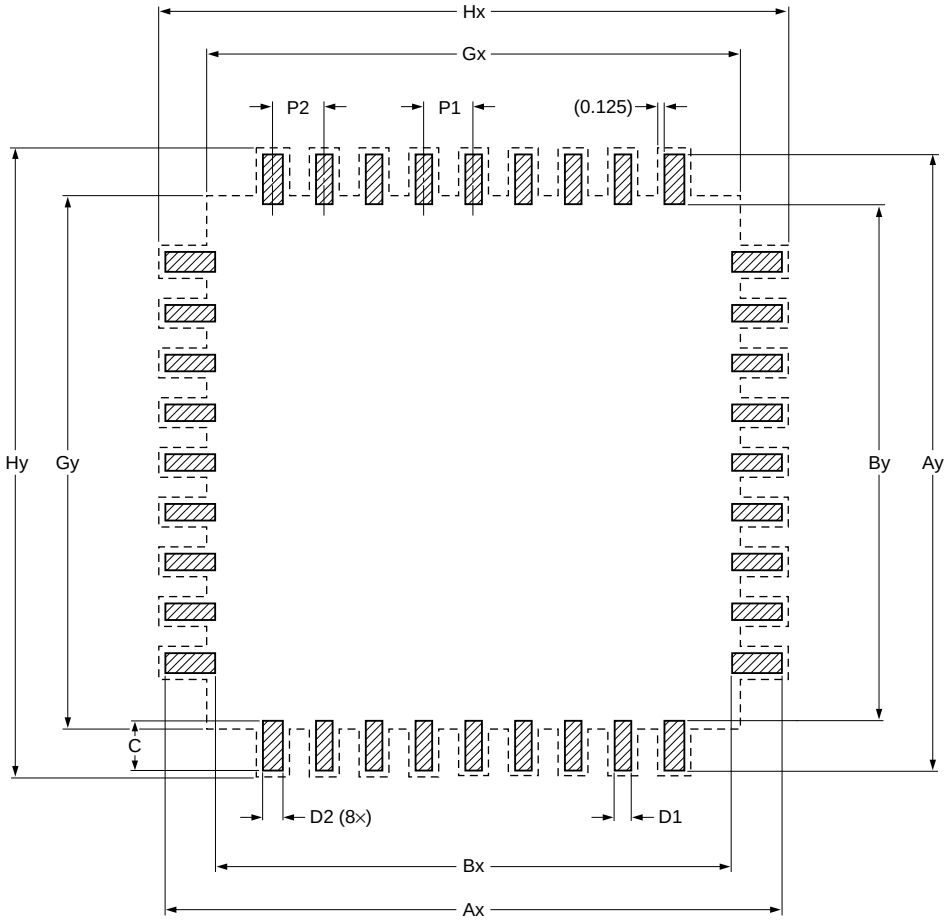
# 13. DAC electrical characteristics

**Table 33. 10-bit DAC electrical characteristics**

*$V_{DDA}$ = 2.7 V to 3.6 V; $T_{amb}$ = −40 °C to +85 °C unless otherwise specified*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $E_D$ | differential linearity error | - | ±1 | - | LSB |
| $E_{L(adj)}$ | integral non-linearity | - | ±1.5 | - | LSB |
| $E_O$ | offset error | - | 0.6 | - | % |
| $E_G$ | gain error | - | 0.6 | - | % |
| $C_L$ | load capacitance | - | - | 200 | pF |
| $R_L$ | load resistance | 1 | - | - | kΩ |

**Footprint information for reflow soldering of LQFP144 package** **SOT486-1**




Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

| P1 | P2 | Ax | Ay | Bx | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.500 | 0.560 | 23.300 | 23.300 | 20.300 | 20.300 | 1.500 | 0.280 | 0.400 | 20.500 | 20.500 | 23.550 | 23.550 |

*sot486-1_fr*

**Fig 47. Reflow soldering of the LQFP144 package**

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