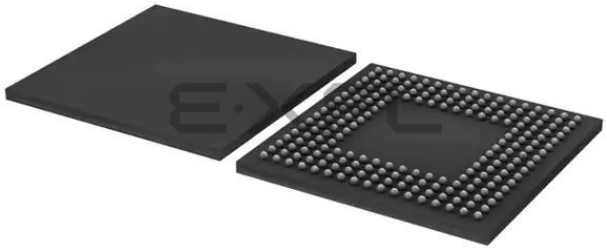

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	165
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-TFBGA
Supplier Device Package	208-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1778fet208-551

- Multilayer AHB matrix interconnect provides a separate bus for each AHB master. AHB masters include the CPU, USB, Ethernet, and the General Purpose DMA controller. This interconnect provides communication with no arbitration delays unless two masters attempt to access the same slave at the same time.
- Split APB bus allows for higher throughput with fewer stalls between the CPU and DMA. A single level of write buffering allows the CPU to continue without waiting for completion of APB writes if the APB was not already busy.
- Cortex-M3 system tick timer, including an external clock input option.
- Standard JTAG test/debug interface as well as Serial Wire Debug and Serial WireTrace Port options.
- Embedded Trace Macrocell (ETM) module supports real-time trace.
- Boundary scan for simplified board testing.
- Non-maskable Interrupt (NMI) input.

- Memory:
  - Up to 512 kB on-chip flash program memory with In-System Programming (ISP) and In-Application Programming (IAP) capabilities. The combination of an enhanced flash memory accelerator and location of the flash memory on the CPU local code/data bus provides high code performance from flash.
  - Up to 96 kB on-chip SRAM includes:

    64 kB of main SRAM on the CPU with local code/data bus for high-performance CPU access.

    Two 16 kB peripheral SRAM blocks with separate access paths for higher throughput. These SRAM blocks may be used for DMA memory as well as for general purpose instruction and data storage.
  - Up to 4032 byte on-chip EEPROM.
- LCD controller, supporting both Super-Twisted Nematic (STN) and Thin-Film Transistors (TFT) displays.
  - Dedicated DMA controller.
  - Selectable display resolution (up to 1024 $\times$ 768 pixels).
  - Supports up to 24-bit true-color mode.
- External Memory Controller (EMC) provides support for asynchronous static memory devices such as RAM, ROM and flash, as well as dynamic memories such as single data rate SDRAM with an SDRAM clock of up to 80 MHz.
- Eight channel General Purpose DMA controller (GPDMA) on the AHB multilayer matrix that can be used with the SSP, I2S, UART, CRC engine, Analog-to-Digital and Digital-to-Analog converter peripherals, timer match signals, GPIO, and for memory-to-memory transfers.
- Serial interfaces:
  - Ethernet MAC with MII/RMII interface and associated DMA controller. These functions reside on an independent AHB.
  - USB 2.0 full-speed dual-port device/host/OTG controller with on-chip PHY and associated DMA controller.
  - Five UARTs with fractional baud rate generation, internal FIFO, DMA support, and RS-485/EIA-485 support. One UART (UART1) has full modem control I/O, and one UART (USART4) supports IrDA, synchronous mode, and a smart card mode conforming to ISO7816-3.
  - Three SSP controllers with FIFO and multi-protocol capabilities. The SSP controllers can be used with the GPDMA.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1788			
LPC1788FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1788FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 ´ 15 ´ 0.7 mm	SOT950-1
LPC1788FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1788FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1787			
LPC1787FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1786			
LPC1786FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1785			
LPC1785FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1778			
LPC1778FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1778FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 ´ 15 ´ 0.7 mm	SOT950-1
LPC1778FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1778FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1777			
LPC1777FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1776			
LPC1776FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1776FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1774			
LPC1774FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1774FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

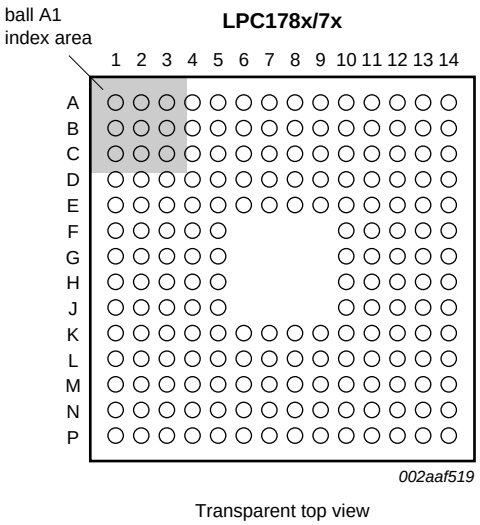


Fig 4. Pin configuration (TFBGA180)

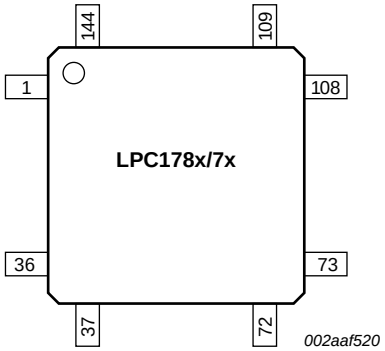


Fig 5. Pin configuration (LQFP144)

6.2 Pin description

I/O pins on the LPC178x/7x are 5 V tolerant and have input hysteresis unless otherwise indicated in the table below. Crystal pins, power pins, and reference voltage pins are not 5 V tolerant. In addition, when pins are selected to be ADC inputs, they are no longer 5 V tolerant and the input voltage must be limited to the voltage at the ADC positive reference pin (VREFP).

All port pins Pn[m] are multiplexed, and the multiplexed functions appear in Table 3 in the order defined by the FUNC bits of the corresponding IOCON register up to the highest used function number. Each port pin can support up to eight multiplexed functions. IOCON register FUNC values which are reserved are noted as ‘R’ in the pin configuration table.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[8]	160	A15	C12	111	[4]	I; IA	I/O	**P0[8] —** General purpose digital input/output pin.
							I/O	**I2S_TX_WS —** I^2S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
							I	**RTC_EV1 —** Event input 1 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[16] —** LCD data.
P0[9]	158	C14	A13	109	[4]	I; IA	I/O	**P0[9] —** General purpose digital input/output pin.
							I/O	**I2S_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
							I	**RTC_EV2 —** Event input 2 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[17] —** LCD data.
P0[10]	98	T15	L10	69	[3]	I; PU	I/O	**P0[10] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for UART2.
							I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P0[11]	100	R14	P12	70	[3]	I; PU	I/O	**P0[11] —** General purpose digital input/output pin.
							I	**U2_RXD —** Receiver input for UART2.
							I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT1 —** Match output for Timer 3, channel 1.
P0[12]	41	R1	J4	29	[5]	I; PU	I/O	**P0[12] —** General purpose digital input/output pin.
							O	**$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							I	**ADC0_IN[6] —** A/D converter 0, input 6. When configured as an ADC input, the digital function of the pin must be disabled.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[13]	45	R2	J5	32	[5]	I; PU	I/O	**P0[13] —** General purpose digital input/output pin.
							O	**USB_UP_LED2 —** USB port 2 GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							I	**ADC0_IN[7] —** A/D converter 0, input 7. When configured as an ADC input, the digital function of the pin must be disabled.
P0[14]	69	T7	M5	48	[3]	I; PU	I/O	**P0[14] —** General purpose digital input/output pin.
							O	**$\overline{\text{USB\_HSTEN2}}$ —** Host Enabled status for USB port 2.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							O	**USB_CONNECT2 —** SoftConnect control for USB port 2. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
P0[15]	128	J16	H13	89	[3]	I; PU	I/O	**P0[15] —** General purpose digital input/output pin.
							O	**U1_TXD —** Transmitter output for UART1.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
P0[16]	130	J14	H14	90	[3]	I; PU	I/O	**P0[16] —** General purpose digital input/output pin.
							I	**U1_RXD —** Receiver input for UART1.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
P0[17]	126	K17	J12	87	[3]	I; PU	I/O	**P0[17] —** General purpose digital input/output pin.
							I	**U1_CTS —** Clear to Send input for UART1.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
P0[18]	124	K15	J13	86	[3]	I; PU	I/O	**P0[18] —** General purpose digital input/output pin.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							I/O	**SSP0_MOSI —** Master Out Slave In for SSP0.
P0[19]	122	L17	J10	85	[3]	I; PU	I/O	**P0[19] —** General purpose digital input/output pin.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**SD_CLK —** Clock output line for SD card interface.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[1]	194	B5	A5	135	[3]	I; PU	I/O	**P1[1] —** General purpose digital input/output pin.
							O	**ENET_TXD1 —** Ethernet transmit data 1 (RMII/MII interface).
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output for Timer 3, channel 3.
							I/O	**SSP2_MOSI —** Master Out Slave In for SSP2.
P1[2]	185	D9	B7	-	[3]	I; PU	I/O	**P1[2] —** General purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							O	**SD_CLK —** Clock output line for SD card interface.
							O	**PWM0[1] —** Pulse Width Modulator 0, output 1.
P1[3]	177	A10	A9	-	[3]	I; PU	I/O	**P1[3] —** General purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**SD_CMD —** Command line for SD card interface.
							O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
P1[4]	192	A5	C6	133	[3]	I; PU	I/O	**P1[4] —** General purpose digital input/output pin.
							O	**ENET_TX_EN —** Ethernet transmit data enable (RMII/MII interface).
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output for Timer 3, channel 2.
							I/O	**SSP2_MISO —** Master In Slave Out for SSP2.
P1[5]	156	A17	B13	-	[3]	I; PU	I/O	**P1[5] —** General purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							O	**SD_PWR —** Power Supply Enable for external SD card power supply.
							O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
P1[6]	171	B11	B10	-	[3]	I; PU	I/O	**P1[6] —** General purpose digital input/output pin.
							I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
							I/O	**SD_DAT[0] —** Data line 0 for SD card interface.
							O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
P1[7]	153	D14	C13	-	[3]	I; PU	I/O	**P1[7] —** General purpose digital input/output pin.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							I/O	**SD_DAT[1] —** Data line 1 for SD card interface.
							O	**PWM0[5] —** Pulse Width Modulator 0, output 5.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[21]	72	R8	N6	50	[3]	I; PU	I/O	**P1[21] —** General purpose digital input/output pin.
							O	**USB_TX_DM1 —** D− transmit data for USB port 1 (OTG transceiver).
							O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I	**$\overline{\text{MC\_ABORT}}$ —** Motor control PWM, active low fast abort.
							-	**R —** Function reserved.
							O	**LCD_VD[7] —** LCD data.
							O	**LCD_VD[11] —** LCD data.
P1[22]	74	U8	M6	51	[3]	I; PU	I/O	**P1[22] —** General purpose digital input/output pin.
							I	**USB_RCV1 —** Differential receive data for USB port 1 (OTG transceiver).
							I	**USB_PWRD1 —** Power Status for USB port 1 (host power switch).
							O	**T1_MAT0 —** Match output for Timer 1, channel 0.
							O	**MC_0B —** Motor control PWM channel 0, output B.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							O	**LCD_VD[8] —** LCD data.
							O	**LCD_VD[12] —** LCD data.
P1[23]	76	P9	N7	53	[3]	I; PU	I/O	**P1[23] —** General purpose digital input/output pin.
							I	**USB_RX_DP1 —** D+ receive data for USB port 1 (OTG transceiver).
							O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
							I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
							I	**MC_FB1 —** Motor control PWM channel 1 feedback input.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							O	**LCD_VD[9] —** LCD data.
							O	**LCD_VD[13] —** LCD data.
P1[24]	78	T9	P7	54	[3]	I; PU	I/O	**P1[24] —** General purpose digital input/output pin.
							I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).
							O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
							I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
							I	**MC_FB2 —** Motor control PWM channel 2 feedback input.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							O	**LCD_VD[10] —** LCD data.
							O	**LCD_VD[14] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P2[1]	152	E14	C14	106	[3]	I; PU	I/O	**P2[1] —** General purpose digital input/output pin.
							O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
							I	**U1_RXD —** Receiver input for UART1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_LE —** Line end signal.
P2[2]	150	D15	E11	105	[3]	I; PU	I/O	**P2[2] —** General purpose digital input/output pin.
							O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
							-	**R —** Function reserved.
							O	**TRACEDATA[3] —** Trace data, bit 3.
							-	**R —** Function reserved.
							O	**LCD_DCLK —** LCD panel clock.
P2[3]	144	E16	E13	100	[3]	I; PU	I/O	**P2[3] —** General purpose digital input/output pin.
							O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
							-	**R —** Function reserved.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							-	**R —** Function reserved.
							O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
P2[4]	142	D17	E14	99	[3]	I; PU	I/O	**P2[4] —** General purpose digital input/output pin.
							O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**T2_MAT1 —** Match output for Timer 2, channel 1.
							-	**R —** Function reserved.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							-	**R —** Function reserved.
							O	**LCD_ENAB_M —** STN AC bias drive or TFT data enable output.

The LPC178x/7x EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

See Table 6 for EMC memory access.

7.10.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.11 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral and can be accessed through the AHB master. The GPDMA controller allows data transfers between the various on-chip SRAM areas and supports the SD/MMC card interface, all SSPs, the I^2S, all UARTs, the A/D Converter, and the D/A Converter peripherals. DMA can also be triggered by selected timer match conditions. Memory-to-memory transfers and transfers to or from GPIO are supported.

7.14 Ethernet

Remark: The Ethernet block is available on parts LPC1788/86 and LPC1778/76.

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share the ARM Cortex-M3 D-code and system bus through the AHB-multilayer matrix to access the various on-chip SRAM blocks for Ethernet data, control, and status information.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Media Independent Interface (MII) or Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.14.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame suppor
  - .
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching.
  - Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.

7.33.1.3 RTC oscillator

The RTC oscillator provides a 1 Hz clock to the RTC and a 32 kHz clock output that can be output on the CLKOUT pin in order to allow trimming the RTC oscillator without interference from a probe.

7.33.1.4 Watchdog oscillator

The Watchdog Timer has a dedicated watchdog oscillator that provides a 500 kHz clock to the Watchdog Timer. The watchdog oscillator is always running if the Watchdog Timer is enabled. The Watchdog oscillator clock can be output on the CLKOUT pin in order to allow observe its frequency.

In order to allow Watchdog Timer operation with minimum power consumption, which can be important in reduced power modes, the Watchdog oscillator frequency is not tightly controlled. The Watchdog oscillator frequency will vary over temperature and power supply within a particular part, and may vary by processing across different parts. This variation should be taken into account when determining Watchdog reload values.

Within a particular part, temperature and power supply variations can produce up to a ±17 % frequency variation. Frequency variation between devices under the same operating conditions can be up to ±30 %.

7.33.2 Main PLL (PLL0) and Alternate PLL (PLL1)

PLL0 (also called the Main PLL) and PLL1 (also called the Alternate PLL) are functionally identical but have somewhat different input possibilities and output connections. These possibilities are shown in Figure 7. The Main PLL can receive its input from either the IRC or the main oscillator and can potentially be used to provide the clocks to nearly everything on the device. The Alternate PLL receives its input only from the main oscillator and is intended to be used as an alternate source of clocking to the USB. The USB has timing needs that may not always be filled by the Main PLL.

Both PLLs are disabled and powered off on reset. If the Alternate PLL is left disabled, the USB clock can be supplied by PLL0 if everything is set up to provide 48 MHz to the USB clock through that route. The source for each clock must be selected via the CLKSEL registers and can be further reduced by clock dividers as needed.

PLL0 accepts an input clock frequency from either the IRC or the main oscillator. If only the Main PLL is used, then its output frequency must be an integer multiple of all other clocks needed in the system. PLL1 takes its input only from the main oscillator, requiring an external crystal in the range of 10 to 25 MHz. In each PLL, the Current Controlled Oscillator (CCO) operates in the range of 156 MHz to 320 MHz, so there are additional dividers to bring the output down to the desired frequencies. The minimum output divider value is 2, insuring that the output of the PLLs have a 50 % duty cycle.

If the USB is used, the possibilities for the CPU clock and other clocks will be limited by the requirements that the frequency be precise and very low jitter, and that the PLL0 output must be a multiple of 48 MHz. Even multiples of 48 MHz that are within the operating range of the PLL are 192 MHz and 288 MHz. Also, only the main oscillator in conjunction with the PLL can meet the precision and jitter specifications for USB. It is due to these limitations that the Alternate PLL is provided.

10.2 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the PCONP register. All other blocks are disabled and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. The peripheral clock was set to PCLK = CCLK/4 with CCLK = 12 MHz, 48 MHz, and 120 MHz.

The combined current of several peripherals running at the same time can be less than the sum of each individual peripheral current measured separately.

Table 14. Power consumption for individual analog and digital blocks

T_{amb} = 25 °C; $V_{DD(REG)(3V3)} = V_{DD(3V3)} = V_{DDA}$ = 3.3 V; PCLK = CCLK/4.

Peripheral	Conditions	Typical supply current in mA		
		12 MHz[1]	48 MHz[1]	120 MHz[2]
Timer0	-	0.01	0.06	0.15
Timer1	-	0.02	0.07	0.16
Timer2	-	0.02	0.07	0.17
Timer3	-	0.01	0.07	0.16
Timer0 + Timer1 + Timer2 + Timer3	-	0.07	0.28	0.67
UART0	-	0.05	0.19	0.45
UART1	-	0.06	0.24	0.56
UART2	-	0.05	0.2	0.47
UART3	-	0.06	0.23	0.56
USART4	-	0.07	0.27	0.66
UART0 + UART1 + UART2 + UART3 + USART4	-	0.29	1.13	2.74
PWM0 + PWM1	-	0.08	0.31	0.75
Motor control PWM	-	0.04	0.15	0.36
I2C0	-	0.01	0.03	0.08
I2C1	-	0.01	0.03	0.1
I2C2	-	0.01	0.03	0.08
I2C0 + I2C1 + I2C2	-	0.02	0.1	0.26
SSP0	-	0.03	0.1	0.26
SSP1	-	0.02	0.11	0.27
DAC	-	0.3	0.31	0.33
ADC (12 MHz clock)	-	1.51	1.61	1.7
CAN1	-	0.11	0.44	1.08
CAN2	-	0.1	0.4	0.98
CAN1 + CAN2	-	0.15	0.59	1.44
DMA	PCLK = CCLK	1.1	4.27	10.27
QEI	-	0.02	0.11	0.28
GPIO	-	0.4	1.72	4.16
LCD	-	0.99	3.84	9.25
I2S	-	0.04	0.18	0.46

Table 14. Power consumption for individual analog and digital blocks *…continued*
T_{amb} = 25 °C; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 3.3 V; PCLK = CCLK/4.

Peripheral	Conditions	Typical supply current in mA		
		12 MHz[1]	48 MHz[1]	120 MHz[2]
EMC	-	0.82	3.17	7.63
RTC	-	0.01	0.01	0.05
USB + PLL1	-	0.62	0.97	1.67
Ethernet	PCENET bit set to 1 in the PCONP register	0.54	2.08	5.03

[1] Boost control bits in the PBOOST register set to 0x0 (see *LPC178x/7x User manual UM10470*).

[2] Boost control bits in the PBOOST register set to 0x3 (see *LPC178x/7x User manual UM10470*).

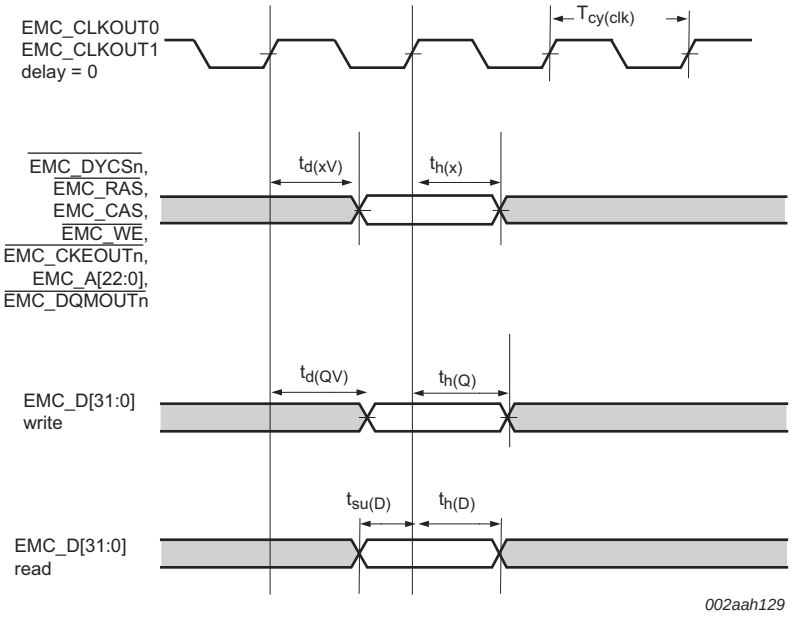


Fig 19. Dynamic external memory interface signal timing

Table 22. Dynamic characteristics: Dynamic external memory interface programmable clock delays (CMDDLY, FBCLKDLY, CLKOUT0DLY and CLKOUT1DLY)

T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V.Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbols	Parameter	Five bit value for each delay in EMCDLYCTL[1]	Min	Typ	Max	Unit
t_{cmddly}, t_{fbdly}, $t_{clk0dly}$, $t_{clk1dly}$	delay time	b00000	0.0	0.0	0.0	ns
		b00001	0.1	0.1	0.2	ns
		b00010	0.2	0.3	0.5	ns
		b00011	0.3	0.4	0.7	ns
		b00100	0.5	0.8	1.3	ns
		b00101	0.6	0.9	1.5	ns
		b00110	0.7	1.1	1.8	ns
		b00111	0.8	1.2	2.0	ns
		b01000	1.2	1.8	2.9	ns
		b01001	1.3	1.9	3.1	ns
		b01010	1.4	2.0	3.4	ns
		b01011	1.5	2.1	3.6	ns
		b01100	1.7	2.6	4.2	ns
		b01101	1.8	2.7	4.4	ns
		b01110	1.9	2.9	4.7	ns
		b01111	2.0	3.0	4.9	ns
		b10000	2.4	3.7	6.0	ns
		b10001	2.5	3.8	6.2	ns
		b10010	2.6	4.0	6.5	ns
		b10011	2.7	4.1	6.7	ns
		b10100	2.9	4.5	7.3	ns
		b10101	3.0	4.6	7.5	ns
		b10110	3.1	4.8	7.8	ns
		b10111	3.2	4.9	8.0	ns
		b11000	3.6	5.4	8.9	ns
		b11001	3.7	5.5	9.1	ns
		b11010	3.8	5.7	9.4	ns
		b11011	3.9	5.8	9.6	ns
		b11100	4.1	6.2	10.2	ns
		b11101	4.2	6.3	10.4	ns
		b11110	4.3	6.6	10.7	ns
		b11111	4.4	6.7	10.9	ns

[1] The programmable delay blocks are controlled by the EMCDLYCTL register in the EMC register block. All delay times are incremental delays for each element starting from delay block 0. See the *LPC178x/7x user manual* for details.

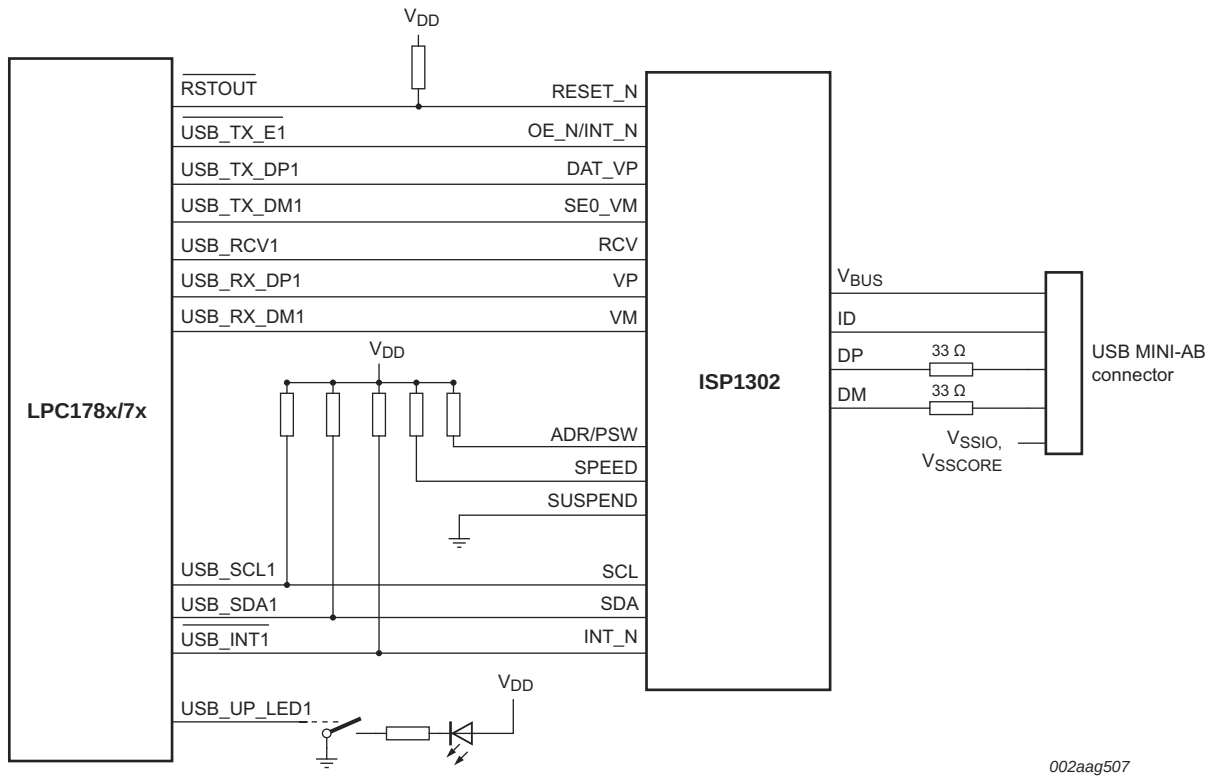
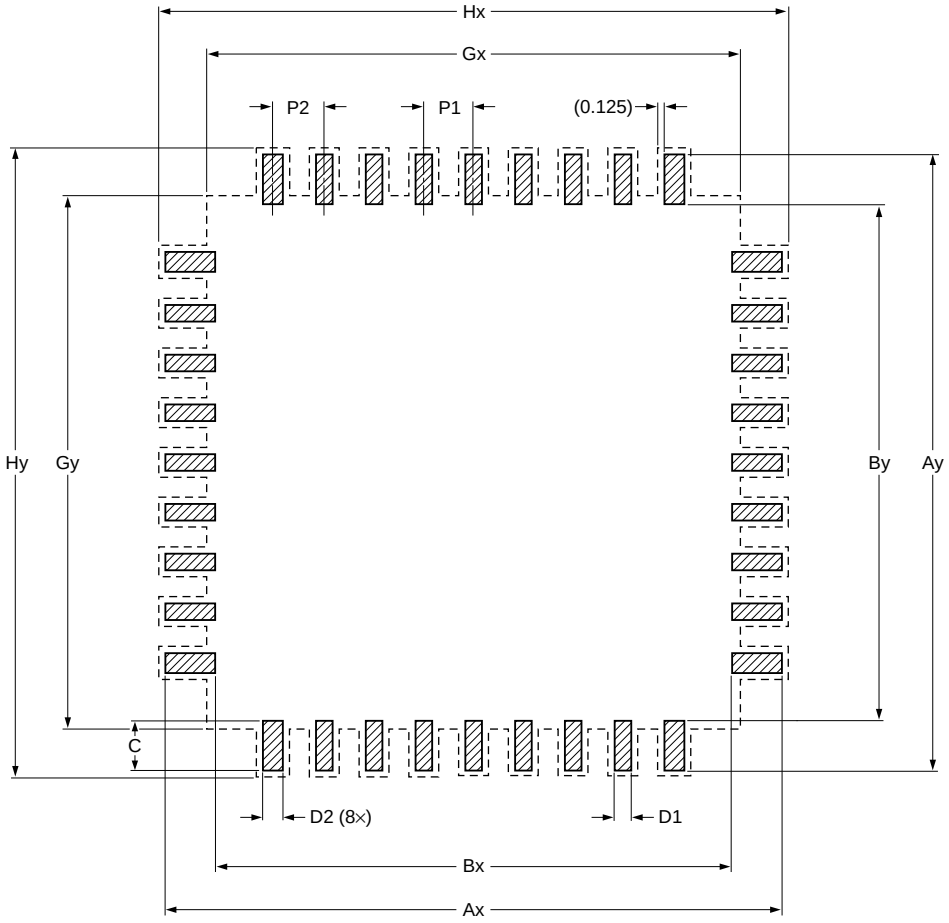


Fig 33. USB OTG port configuration: VP_VM mode

Footprint information for reflow soldering of LQFP144 package **SOT486-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	23.300	23.300	20.300	20.300	1.500	0.280	0.400	20.500	20.500	23.550	23.550

sot486-1_fr

Fig 47. Reflow soldering of the LQFP144 package

18. References

[1] LPC178x/7x User manual UM10470:
http://www.nxp.com/documents/user_manual/UM10470.pdf

[2] LPC177x/8x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC177X_8X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC178X_7X v.3	20111220	Objective data sheet	-	LPC178X_7X v.2
Modifications:	• Removed BOOT function from pin P3[14]. • I_{BAT} and $I_{DD(REG)(3V3)}$ updated for Deep power-down mode in Table 13. • Maximum SDRAM clock of 80 MHz specified in Section 2, Table 18, and Table 19. • Power consumption data added (Figure 9 and Figure 10). • Removed parameter Z_{DRV} in Table 13. • Specified maximum value for parameter C_L in Table 33 and remove typical value. • Specified setting of boost bits in Table 14, Table note 5 and in Table 13, Table note 6 . • USB connection diagrams updated (Figure 33 to Figure 36). • Current drain condition on battery supply specified in Section 7.33.6. • Table note 10 in Table 13 updated. • ADC characteristics updated (Table 31). • Section 14.6 “Reset pin configuration for RTC operation” added. • EEPROM size for parts LPC1774 corrected in Table 2 and Figure 1. • Changed function LCD_VD[5] on pin P0[10] to Reserved. • Changed function LCD_VD[10] on pin P0[11] to Reserved. • Changed function LCD_VD[13] on pin P0[19] to Reserved. • Changed function LCD_VD[14] on pin P0[20] to Reserved. • ADC interface model updated (see Table 32 and Figure 30).			
LPC178X_7X v.2	20110527	Objective data sheet	-	LPC178X_7X v.1
Modifications:	• Symbol names in Table 3 to Table 5 abbreviated. • Reserved functions added in Table 3. • Added function LCD_VD[5] to pin P0[10]. • Added function LCD_VD[10] to pin P0[11]. • Added function LCD_VD[13] to pin P0[19]. • Added function LCD_VD[14] to pin P0[20]. • Added function U4_SCLK to pin P0[21]. • Added function • Added function MOSI to pin P5[0]. • Added function SSP2_MISO to pin P5[1]. • Added EMC dynamic characteristics.			
LPC178X_7X v.1	20110524	Objective data sheet	-	-

For more information, please visit: http://www.nxp.com
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