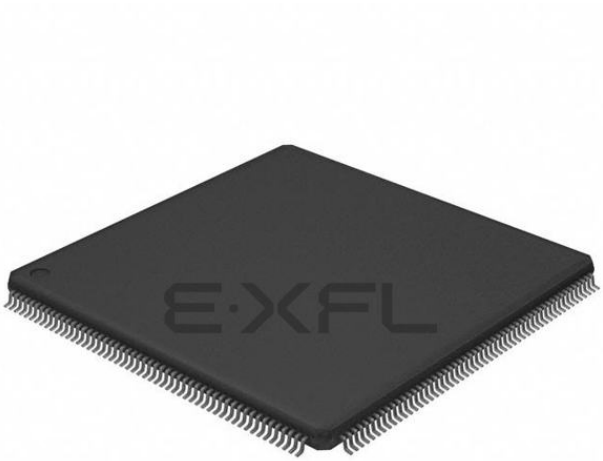

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, Motor Control PWM, POR, PWM, WDT
Number of I/O	165
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1785fbd208-551

Table 3. Pin description

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[0] to P0[31]							I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block.
P0[0]	94	U15	M10	66	[3]	I; PU	I/O	**P0[0] —** General purpose digital input/output pin.
							I	**CAN_RD1 —** CAN1 receiver input.
							O	**U3_TXD —** Transmitter output for UART3.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
							O	**U0_TXD —** Transmitter output for UART0.
P0[1]	96	T14	N11	67	[3]	I; PU	I/O	**P0[1] —** General purpose digital input/output pin.
							O	**CAN_TD1 —** CAN1 transmitter output.
							I	**U3_RXD —** Receiver input for UART3.
							I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
							I	**U0_RXD —** Receiver input for UART0.
P0[2]	202	C4	D5	141	[3]	I; PU	I/O	**P0[2] —** General purpose digital input/output pin.
							O	**U0_TXD —** Transmitter output for UART0.
							O	**U3_TXD —** Transmitter output for UART3.
P0[3]	204	D6	A3	142	[3]	I; PU	I/O	**P0[3] —** General purpose digital input/output pin.
							I	**U0_RXD —** Receiver input for UART0.
							I	**U3_RXD —** Receiver input for UART3.
P0[4]	168	B12	A11	116	[3]	I; PU	I/O	**P0[4] —** General purpose digital input/output pin.
							I/O	**I2S_RX_SCK —** I^2S Receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							I	**CAN_RD2 —** CAN2 receiver input.
							I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[0] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[5]	166	C12	B11	115	[3]	I; PU	I/O	**P0[5] —** General purpose digital input/output pin.
							I/O	**I2S_RX_WS —** I^2S Receive word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							O	**CAN_TD2 —** CAN2 transmitter output.
							I	**T2_CAP1 —** Capture input for Timer 2, channel 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[1] —** LCD data.
P0[6]	164	D13	D11	113	[3]	I; PU	I/O	**P0[6] —** General purpose digital input/output pin.
							I/O	**I2S_RX_SDA —** I^2S Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							O	**T2_MAT0 —** Match output for Timer 2, channel 0.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[8] —** LCD data.
P0[7]	162	C13	B12	112	[4]	I; IA	I/O	**P0[7] —** General purpose digital input/output pin.
							I/O	**I2S_TX_SCK —** I^2S transmit clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							I/O	**SSP1_SCK —** Serial Clock for SSP1.
							O	**T2_MAT1 —** Match output for Timer 2, channel 1.
							I	**RTC_EV0 —** Event input 0 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[9] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[25]	80	T10	L7	56	[3]	I; PU	I/O	**P1[25] —** General purpose digital input/output pin.
							O	**USB_LS1 —** Low Speed status for USB port 1 (OTG transceiver).
							O	**USB_HSTEN1 —** Host Enabled status for USB port 1.
							O	**T1_MAT1 —** Match output for Timer 1, channel 1.
							O	**MC_1A —** Motor control PWM channel 1, output A.
							O	**CLKOUT —** Selectable clock output.
							O	**LCD_VD[11] —** LCD data.
							O	**LCD_VD[15] —** LCD data.
P1[26]	82	R10	P8	57	[3]	I; PU	I/O	**P1[26] —** General purpose digital input/output pin.
							O	**USB_SSPND1 —** USB port 1 Bus Suspend status (OTG transceiver).
							O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
							I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
							O	**MC_1B —** Motor control PWM channel 1, output B.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							O	**LCD_VD[12] —** LCD data.
							O	**LCD_VD[20] —** LCD data.
P1[27]	88	T12	M9	61	[3]	I; PU	I/O	**P1[27] —** General purpose digital input/output pin.
							I	**USB_INT1 —** USB port 1 OTG transceiver interrupt (OTG transceiver).
							I	**USB_OVRCR1 —** USB port 1 Over-Current status.
							I	**T0_CAP1 —** Capture input for Timer 0, channel 1.
							O	**CLKOUT —** Selectable clock output.
							-	**R —** Function reserved.
							O	**LCD_VD[13] —** LCD data.
							O	**LCD_VD[21] —** LCD data.
P1[28]	90	T13	P10	63	[3]	I; PU	I/O	**P1[28] —** General purpose digital input/output pin.
							I/O	**USB_SCL1 —** USB port 1 I^2C serial clock (OTG transceiver).
							I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
							O	**T0_MAT0 —** Match output for Timer 0, channel 0.
							O	**MC_2A —** Motor control PWM channel 2, output A.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							O	**LCD_VD[14] —** LCD data.
							O	**LCD_VD[22] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P5[3]	141	G14	G10	98	[11]	I	I/O	**P5[3] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**U4_RXD —** Receiver input for USART4.
							I/O	**I2C0_SCL —** I^2C0 clock input/output (this pin uses a specialized I^2C pad that supports I^2C Fast Mode Plus).
P5[4]	206	C3	C4	143	[3]	I; PU	I/O	**P5[4] —** General purpose digital input/output pin.
							O	**U0_OE —** RS-485/EIA-485 output enable signal for UART0.
							-	**R —** Function reserved.
							O	**T3_MAT3 —** Match output for Timer 3, channel 3.
							O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
JTAG_TDO (SWO)	2	D3	B1	1	[3]	O	O	Test Data Out for JTAG interface. Also used as Serial wire trace output.
JTAG_TDI	4	C2	C3	3	[3]	I; PU	I	Test Data In for JTAG interface.
JTAG_TMS (SWDIO)	6	E3	C2	4	[3]	I; PU	I	Test Mode Select for JTAG interface. Also used as Serial wire debug data input/output.
JTAG_$\overline{\text{TRST}}$	8	D1	D4	5	[3]	I; PU	I	Test Reset for JTAG interface.
JTAG_TCK (SWDCLK)	10	E2	D2	7	[3]	i	I	Test Clock for JTAG interface. This clock must be slower than 1/6 of the CPU clock (CCLK) for the JTAG interface to operate. Also used as serial wire clock.
$\overline{\text{RESET}}$	35	M2	J1	24	[12]	I; PU	I	External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. This pin also serves as the debug select input. LOW level selects the JTAG boundary scan. HIGH level selects the ARM SWD debug mode.
$\overline{\text{RSTOUT}}$	29	K3	H2	20	[3]	OH	O	Reset status output. A LOW output on this pin indicates that the device is in the reset state for any reason. This reflects the $\overline{\text{RESET}}$ input pin and all internal reset sources.
RTC_ALARM	37	N1	H5	26	[13]	OL	O	RTC controlled output. This pin has a low drive strength and is powered by VBAT. It is driven HIGH when an RTC alarm is generated.
RTCX1	34	K2	J2	23	[14] [15]	-	I	Input to the RTC 32 kHz ultra-low power oscillator circuit.
RTCX2	36	L2	J3	25	[14] [15]	-	O	Output from the RTC 32 kHz ultra-low power oscillator circuit.
USB_D−2	52	U1	N2	37	[9]	-	I/O	USB port 2 bidirectional D− line.

Table 5. Pin allocation table TFBGA180

Not all functions are available on all parts. See Table 2 and Table 7 (EMC pins).

Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol
13	P2[6]	14	P4[27]		-		-
Row G							
1	$V_{DD(REG)(3V3)}$	2	VREFP	3	P3[7]	4	P3[15]
5	P3[3]	6	-	7	-	8	-
9	-	10	P5[3]	11	P2[7]	12	P4[10]
13	V_{SS}	14	P2[8]		-		-
Row H							
1	P5[1]	2	$\overline{\text{RSTOUT}}$	3	V_{SSREG}	4	V_{SS}
5	RTC_ALARM	6	-	7	-	8	-
9	-	10	P4[5]	11	P2[9]	12	P4[9]
13	P0[15]	14	P0[16]		-		-

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

7.7 Memory map

Table 6. LPC178x/177x memory usage and details

Address range	General Use	Address range details and description	
0x0000 0000 to 0x1FFF FFFF	On-chip non-volatile memory	0x0000 0000 - 0x0007 FFFF	For devices with 512 kB of flash memory.
		0x0000 0000 - 0x0003 FFFF	For devices with 256 kB of flash memory.
		0x0000 0000 - 0x0001 FFFF	For devices with 128 kB of flash memory.
		0x0000 0000 - 0x0000 FFFF	For devices with 64 kB of flash memory.
	On-chip main SRAM	0x1000 0000 - 0x1000 FFFF	For devices with 64 kB of main SRAM.
		0x1000 0000 - 0x1000 7FFF	For devices with 32 kB of main SRAM.
		0x1000 0000 - 0x1000 3FFF	For devices with 16 kB of main SRAM.
	Boot ROM	0x1FFF 0000 - 0x1FFF 1FFF	8 kB Boot ROM with flash services.
0x2000 0000 to 0x3FFF FFFF	On-chip SRAM (typically used for peripheral data)	0x2000 0000 - 0x2000 1FFF	Peripheral RAM - bank 0 (first 8 kB)
		0x2000 2000 - 0x2000 3FFF	Peripheral RAM - bank 0 (second 8 kB)
		0x2000 4000 - 0x2000 7FFF	Peripheral RAM - bank 1 (16 kB)
	AHB peripherals	0x2008 0000 - 0x200B FFFF	See Figure 6 for details
0x4000 0000 to 0x7FFF FFFF	APB Peripherals	0x4000 0000 - 0x4007 FFFF	APB0 Peripherals, up to 32 peripheral blocks of 16 kB each.
		0x4008 0000 - 0x400F FFFF	APB1 Peripherals, up to 32 peripheral blocks of 16 kB each.
0x8000 0000 to 0xDFFF FFFF	Off-chip Memory via the External Memory Controller	Four static memory chip selects:	
		0x8000 0000 - 0x83FF FFFF	Static memory chip select 0 (up to 64 MB)
		0x9000 0000 - 0x93FF FFFF	Static memory chip select 1 (up to 64 MB)
		0x9800 0000 - 0x9BFF FFFF	Static memory chip select 2 (up to 64 MB)
		0x9C00 0000 - 0x9FFF FFFF	Static memory chip select 3 (up to 64 MB)
		Four dynamic memory chip selects:	
		0xA000 0000 - 0xAFFF FFFF	Dynamic memory chip select 0 (up to 256MB)
		0xB000 0000 - 0xBFFF FFFF	Dynamic memory chip select 1 (up to 256MB)
		0xC000 0000 - 0xCFFF FFFF	Dynamic memory chip select 2 (up to 256MB)
		0xD000 0000 - 0xDFFF FFFF	Dynamic memory chip select 3 (up to 256MB)
0xE000 0000 to 0xE00F FFFF	Cortex-M3 Private Peripheral Bus	0xE000 0000 - 0xE00F FFFF	Cortex-M3 related functions, includes the NVIC and System Tick Timer.

The LPC178x/7x incorporate several distinct memory regions, shown in the following figures. Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 1 MB in size and is divided to allow for up to 64 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the PWMMR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

7.26.1 Features

- LPC178x/7x has two PWM blocks with Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

7.27 Motor control PWM

The LPC178x/7x contain one motor control PWM.

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

The DMA controller can continue to work in Sleep mode and has access to the peripheral RAMs and all peripheral registers. The flash memory and the main SRAM are not available in Sleep mode, they are disabled in order to save power.

Wake-up from Sleep mode will occur whenever any enabled interrupt occurs.

7.33.4.2 Deep-sleep mode

In Deep-sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep-sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down to allow fast wake-up. The RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The clock divider registers are automatically reset to zero.

The Deep-sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Deep-sleep mode reduces chip power consumption to a very low value. Power to the flash memory is left on in Deep-sleep mode, allowing a very quick wake-up.

Wake-up from Deep-sleep mode can initiated by the NMI, External Interrupts $\overline{\text{EINT0}}$ through $\overline{\text{EINT3}}$, GPIO interrupts, the Ethernet Wake-on-LAN interrupt, Brownout Detect, an RTC Alarm interrupt, a USB input pin transition (USB activity interrupt), a CAN input pin transition, or a Watchdog Timer time-out, when the related interrupt is enabled. Wake-up will occur whenever any enabled interrupt occurs.

On wake-up from Deep-sleep mode, the code execution and peripherals activities will resume after four cycles expire if the IRC was used before entering Deep-sleep mode. If the main external oscillator was used, the code execution will resume when 4096 cycles expire. PLL and clock dividers need to be reconfigured accordingly.

7.33.4.3 Power-down mode

Power-down mode does everything that Deep-sleep mode does but also turns off the power to the IRC oscillator and the flash memory. This saves more power but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

When the chip enters Power-down mode, the IRC, the main oscillator, and all clocks are stopped. The RTC remains running if it has been enabled and RTC interrupts may be used to wake up the CPU. The flash is forced into Power-down mode. The PLLs are automatically turned off and the clock selection multiplexers are set to use the system clock sysclk (the reset state). The clock divider control registers are automatically reset to zero. If the Watchdog timer is running, it will continue running in Power-down mode.

Table 13. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[15][16][17]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[18]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[18]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	µA
		$V_{DD(3V3)} < V_I < 5$ V		0	0	0	µA
I^2C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05 \times V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[19]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[20]	-	-	±10	µA
V_{BUS}	bus supply voltage		[20]	-	-	5.25	V

Table 14. Power consumption for individual analog and digital blocks *…continued*
T_{amb} = 25 °C; $V_{DD(REG)(3V3)}$ = $V_{DD(3V3)}$ = V_{DDA} = 3.3 V; PCLK = CCLK/4.

Peripheral	Conditions	Typical supply current in mA		
		12 MHz[1]	48 MHz[1]	120 MHz[2]
EMC	-	0.82	3.17	7.63
RTC	-	0.01	0.01	0.05
USB + PLL1	-	0.62	0.97	1.67
Ethernet	PCENET bit set to 1 in the PCONP register	0.54	2.08	5.03

[1] Boost control bits in the PBOOST register set to 0x0 (see *LPC178x/7x User manual UM10470*).

[2] Boost control bits in the PBOOST register set to 0x3 (see *LPC178x/7x User manual UM10470*).

Table 17. Dynamic characteristics: Static external memory interface *…continued*

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
t_{deact}	deactivation time	WR_8; PB = 0; PB = 1	[3]	−2.7	−3.4	−4.7	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	WR_9; PB = 0	[3]	2.8 + $T_{cy(clk)}$ × (1 + WAITWEN)	3.7 + $T_{cy(clk)}$ × (1 + WAITWEN)	5.1 + $T_{cy(clk)}$ × (1 + WAITWEN)	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	WR_{10}; PB = 0	[3]	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 2.6	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 3.4	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 4.9	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	WR_{11}; PB = 0	[3][6]	2.6 + $T_{cy(clk)}$	3.3 + $T_{cy(clk)}$	4.4 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	WR12; PB = 0	[3]	2.7 + $T_{cy(clk)}$	3.6 + $T_{cy(clk)}$	4.8 + $T_{cy(clk)}$	ns

[1] Parameters are shown as RD_n or WD_n in Figure 16 as indicated in the Conditions column.

[2] Parameters specified for 40 % of $V_{DD(3V3)}$ for rising edges and 60 % of $V_{DD(3V3)}$ for falling edges.

[3] $T_{cy(clk)}$ = 1/EMC_CLK (see *LPC178x/7x User manual UM10470*).

[4] Latest of address valid, $\overline{EMC\_CSx}$ LOW, $\overline{EMC\_OE}$ LOW, $\overline{EMC\_BLSx}$ LOW (PB = 1).

[5] After End Of Read (EOR): Earliest of $\overline{EMC\_CSx}$ HIGH, $\overline{EMC\_OE}$ HIGH, $\overline{EMC\_BLSx}$ HIGH (PB = 1), address invalid.

[6] End Of Write (EOW): Earliest of address invalid, $\overline{EMC\_CSx}$ HIGH, $\overline{EMC\_BLSx}$ HIGH (PB = 1).

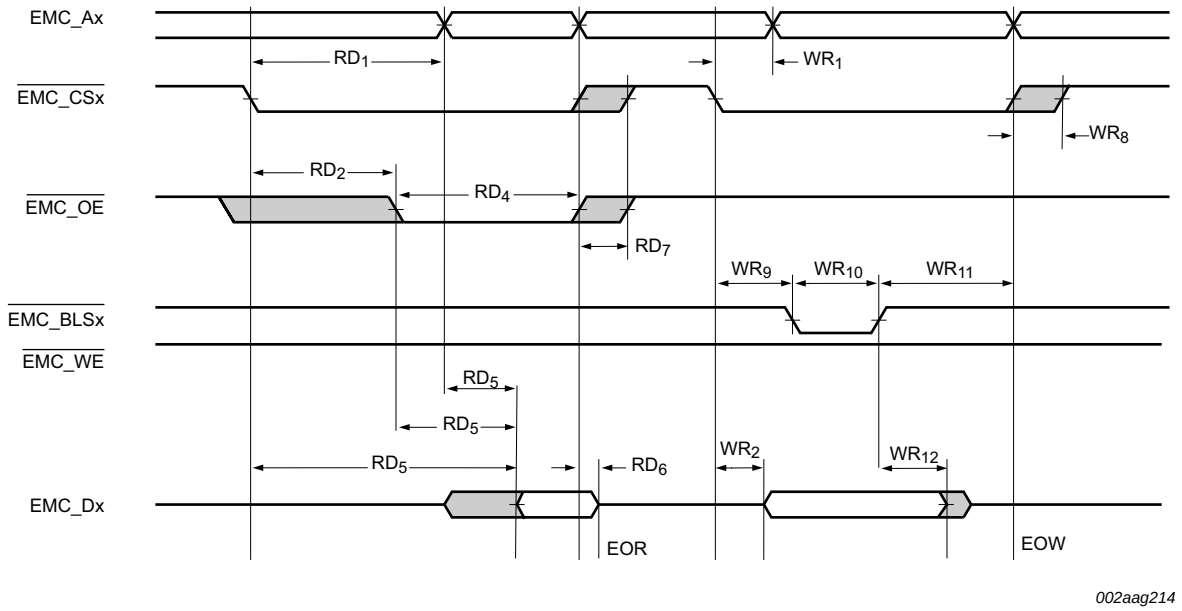


Fig 16. External static memory read/write access (PB = 0)

11.3 External clock

Table 23. Dynamic characteristic: external clock (see Figure 36)
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Min	Typ	Max	Unit
f_{osc}	oscillator frequency	1	12	25	MHz
$T_{cy(clk)}$	clock cycle time	40	83.3	1000	ns
t_{CHCX}	clock HIGH time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time	-	-	5	ns
t_{CHCL}	clock fall time	-	-	5	ns

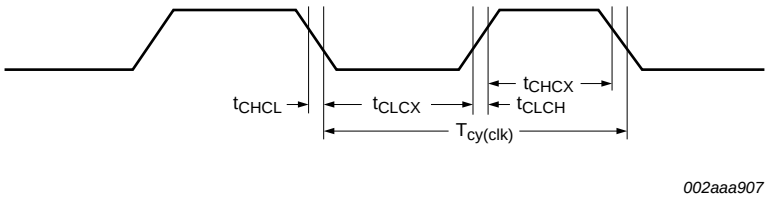


Fig 20. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.4 Internal oscillators

Table 24. Dynamic characteristic: internal oscillators
T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	11.88	12	12.12	MHz
$f_{i(RTC)}$	RTC input frequency	-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.5 I/O pins

Table 25. Dynamic characteristic: I/O pins[1]
C_L = 10 pF; T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ = 3.0 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins.

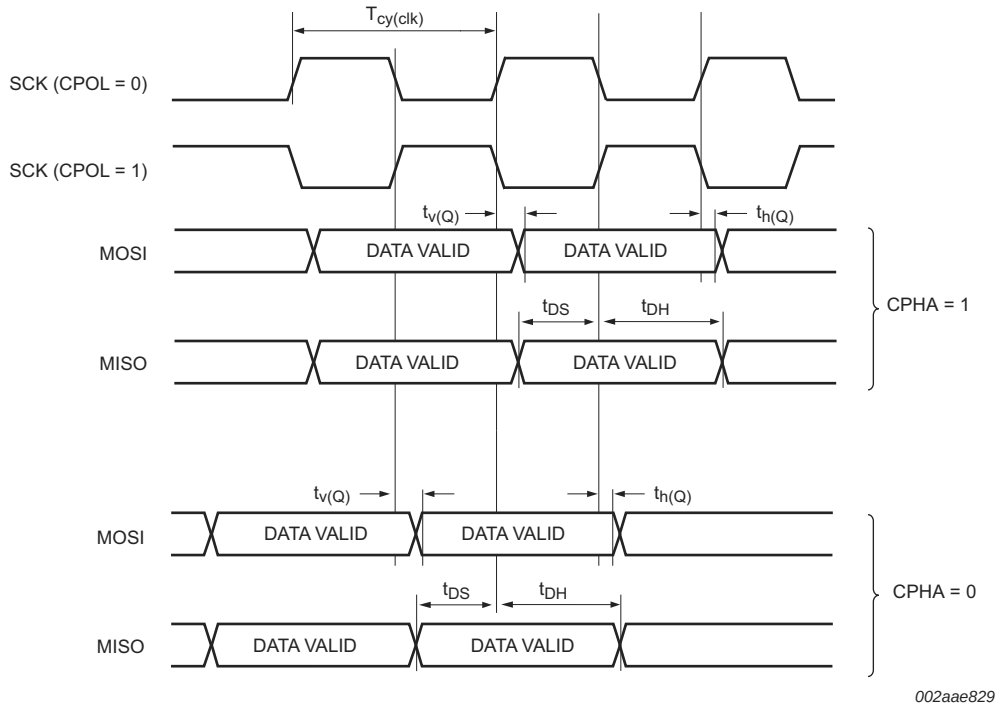


Fig 21. SSP master timing in SPI mode

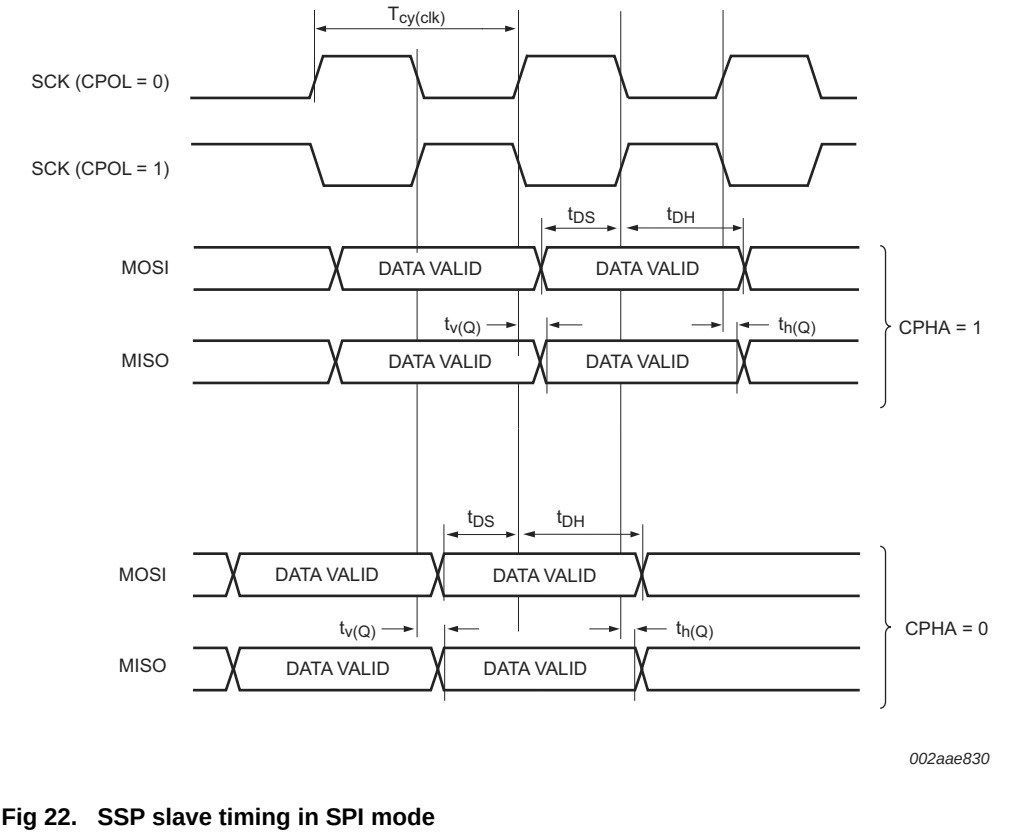
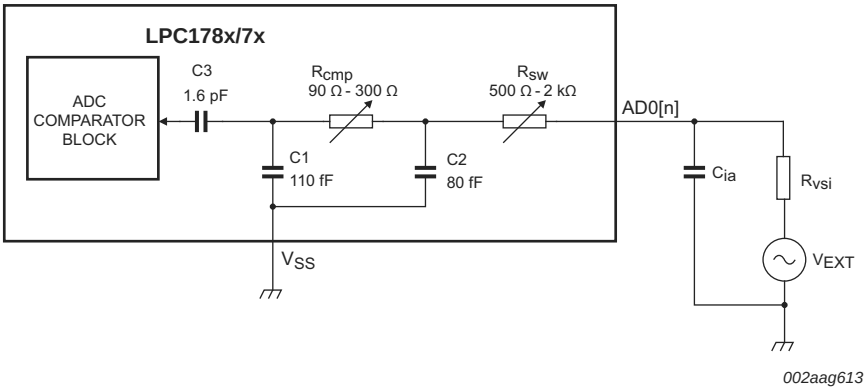


Fig 22. SSP slave timing in SPI mode



The values of resistor components R_{cmp} and R_{sw} vary with temperature and input voltage and are process-dependent.

Fig 29. ADC interface to pins ADC0_IN[n]

Table 32. ADC interface components

Component	Range	Description
R_{cmp}	90 Ω to 300 Ω	Switch-on resistance for the comparator input switch. Varies with temperature, input voltage, and process.
R_{sw}	500 Ω to 2 kΩ	Switch-on resistance for channel selection switch. Varies with temperature, input voltage, and process.
C1	110 fF	Parasitic capacitance from the ADC block level.
C2	80 fF	Parasitic capacitance from the ADC block level.
C3	1.6 pF	Sampling capacitor.

13. DAC electrical characteristics

Table 33. 10-bit DAC electrical characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
E_D	differential linearity error	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity	-	±1.5	-	LSB
E_O	offset error	-	0.6	-	%
E_G	gain error	-	0.6	-	%
C_L	load capacitance	-	-	200	pF
R_L	load resistance	1	-	-	kΩ

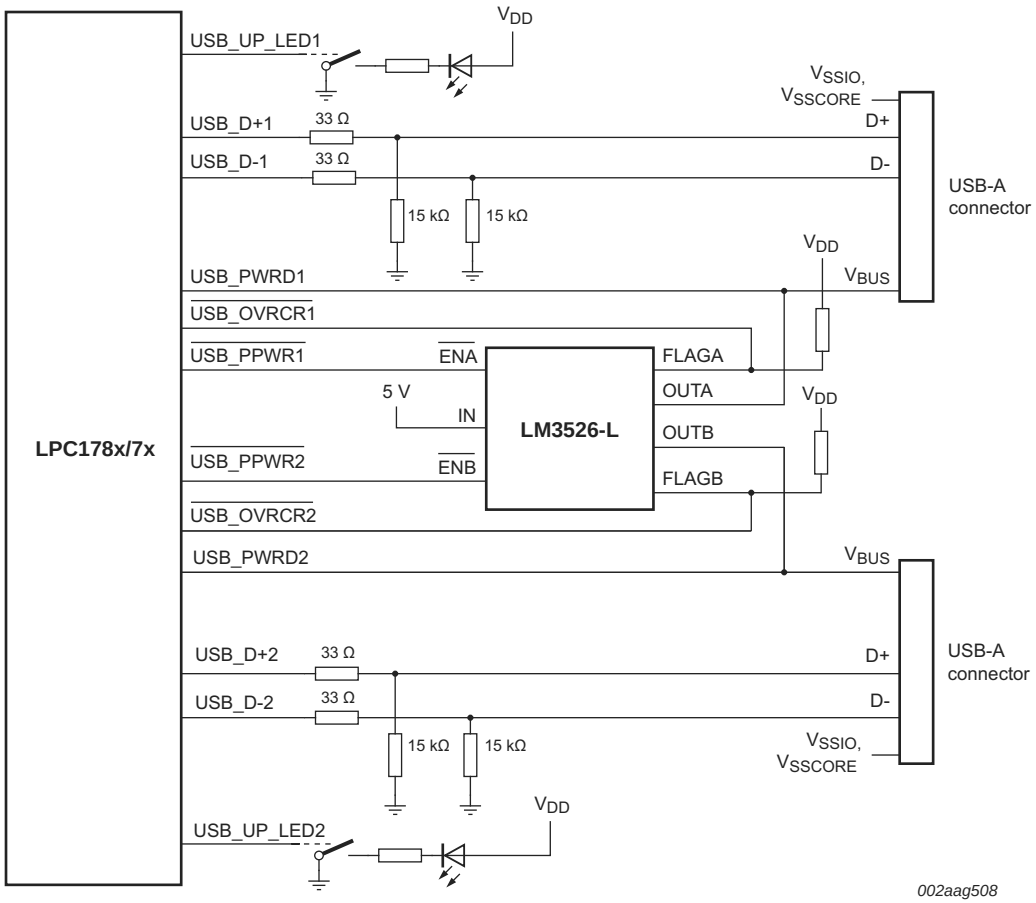
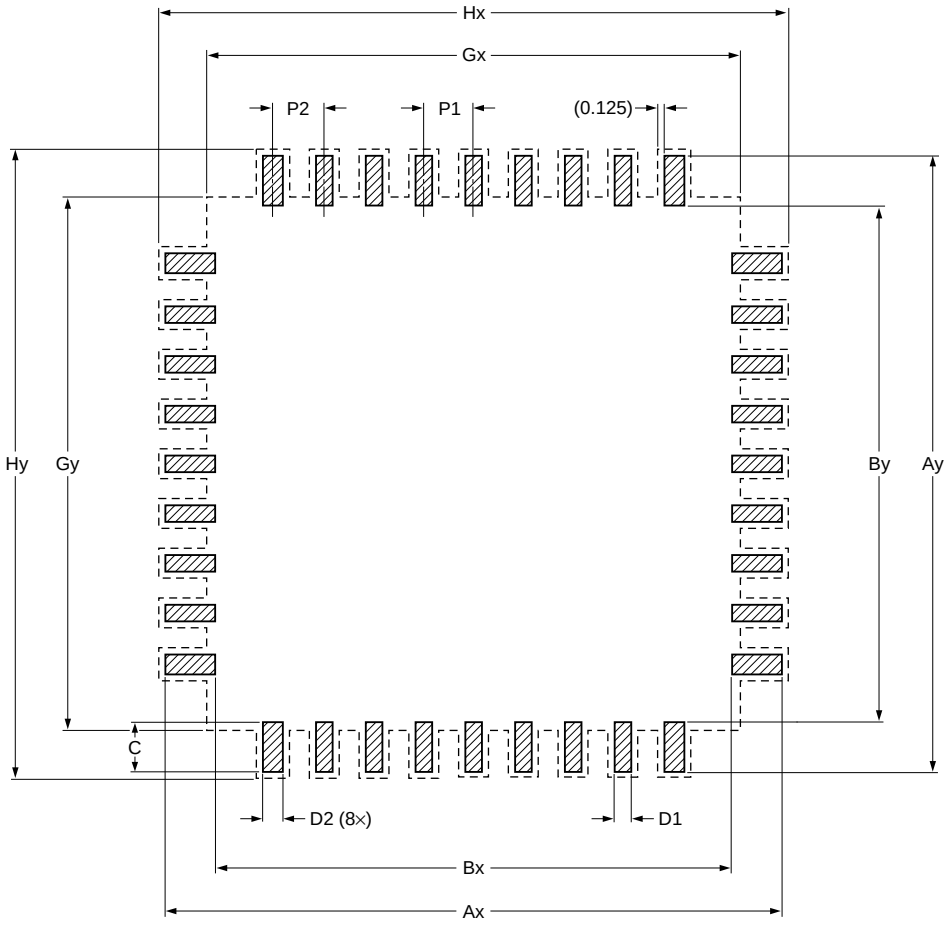


Fig 34. USB host port configuration: port 1 and port 2 as hosts

16. Soldering

Footprint information for reflow soldering of LQFP208 package **SOT459-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	31.300	31.300	28.300	28.300	1.500	0.280	0.400	28.500	28.500	31.550	31.550

sot459-1_fr

Fig 45. Reflow soldering of the LQFP208 package

19. Revision history

Table 37. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC178X_7X v.5.5	20160426	Product data sheet	-	LPC178X_7X v.5.4
Modifications:	• Updated Table 29 “Dynamic characteristics: LCD”: $t_{d(QV)}$ max value is 9 ns for accuracy; was 12 ns.			
LPC178X_7X v.5.4	20160321	Product data sheet	CIN 201603016I	LPC178X_7X v.5.3
Modifications:	• Added Table 18 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00” for 10 pF load. • Updated Table 19 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00” for 30 pF load. • Added Table 20 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01” for 10 pF load. • Updated Table 21 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01” for 30 pF load. • Updated Table 22 “Dynamic characteristics: Dynamic external memory interface programmable clock delays (CMDDLY, FBCLKDLY, CLKOUT0DLY and CLKOUT1DLY)”. • Updated Figure 19 “Dynamic external memory interface signal timing”.			
LPC178X_7X v.5.3	20151015	Product data sheet	-	LPC178X_7X v.5.2
Modifications:	• Corrected max value of $t_{v(Q)}$ (data output valid time) in SPI mode to $3*T_{cy(PCLK)}$ + 6.3 ns. Was: $3*T_{cy(PCLK)}$ + 2.5 ns. See Table 26 “Dynamic characteristics: SSP pins in SPI mode”.			
LPC178X_7X v.5.2	20150814	Product data sheet	-	LPC178X_7X v.5.1
Modifications:	• Updated max value of $t_{v(Q)}$ (data output valid time) in SPI mode to $3*T_{cy(PCLK)}$ + 2.5 ns. See Table 24 “Dynamic characteristics: SSP pins in SPI mode”. • Added a column for GPIO pins and device order part number to the ordering options table. See Table 2 “LPC178x/7x ordering options”.			
LPC178X_7X v.5.1	20140501	Product data sheet	-	LPC178X_7X v.5
Modifications:	• Updated parameter $t_{su(D)}$ in Table 18 “Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00”: Minimum value changed to (FBCLKDLY + 1) × 0.25 + 0.3. Maximum value removed. • Removed max value from parameter $t_{h(D)}$ in Table 17. • Removed min value from parameter t_{deact} in Table 17. • Specified ADC conversion rate in burst mode in Table 29 “12-bit ADC characteristics”.			

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC178X_7X v.5	20140501	Product data sheet	-	LPC178X_7X v.4.1
Modifications:	• Removed overbar from NMI. • Table 3: – Added minimum reset pulse width of 50 ns to $\overline{\text{RESET}}$ pin. – Updated Table note 14 for RTCX pins (32 kHz crystal must be used to operate RTC). – Added boundary scan information to description for $\overline{\text{RESET}}$ pin. – Updated pin description of STCLK. • Table 13: Added Table note 3 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.”. • Table 23: Removed reference to $\overline{\text{RESET}}$ pin from Table note 1. • Table 24: – Removed $T_{cy(PCLK)}$ spec; already given by the maximum chip frequency. – Changed min clock cycle time for SSP slave from 120 to 100. – Updated Table note 1 and Table note 3. • Table 29: Added Table note 1 “VDDA and VREFP should be tied to VDD(3V3) if the ADC and DAC are not used.”. • Section 7.21.1 “Features”: Changed max speed for SSP master from 60 to 33. • and added typical specs Table 17, Table 18, Table 19. • SOT570-2 obsolete; replaced with SOT570-3. • Table 17: – Updated EMC timing specs to CL = 30 pF. – Added typical specs. – Table note 3: Changed $T_{cy(clk)}$ = 1/CCLK to $T_{cy(clk)}$ = 1/EMC_CLK. • Table 18: – Updated EMC timing specs to CL = 30 pF – Added typical specs. – Removed “All programmable delays EMCDLYCTL are bypassed” from table title. • Table 19: – Updated EMC timing specs to CL = 30 pF – Added typical specs. – Removed “All programmable delays EMCDLYCTL are bypassed” from table title.			

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC178X_7X v.3	20111220	Objective data sheet	-	LPC178X_7X v.2
Modifications:	• Removed BOOT function from pin P3[14]. • I_{BAT} and $I_{DD(REG)(3V3)}$ updated for Deep power-down mode in Table 13. • Maximum SDRAM clock of 80 MHz specified in Section 2, Table 18, and Table 19. • Power consumption data added (Figure 9 and Figure 10). • Removed parameter Z_{DRV} in Table 13. • Specified maximum value for parameter C_L in Table 33 and remove typical value. • Specified setting of boost bits in Table 14, Table note 5 and in Table 13, Table note 6 . • USB connection diagrams updated (Figure 33 to Figure 36). • Current drain condition on battery supply specified in Section 7.33.6. • Table note 10 in Table 13 updated. • ADC characteristics updated (Table 31). • Section 14.6 “Reset pin configuration for RTC operation” added. • EEPROM size for parts LPC1774 corrected in Table 2 and Figure 1. • Changed function LCD_VD[5] on pin P0[10] to Reserved. • Changed function LCD_VD[10] on pin P0[11] to Reserved. • Changed function LCD_VD[13] on pin P0[19] to Reserved. • Changed function LCD_VD[14] on pin P0[20] to Reserved. • ADC interface model updated (see Table 32 and Figure 30).			
LPC178X_7X v.2	20110527	Objective data sheet	-	LPC178X_7X v.1
Modifications:	• Symbol names in Table 3 to Table 5 abbreviated. • Reserved functions added in Table 3. • Added function LCD_VD[5] to pin P0[10]. • Added function LCD_VD[10] to pin P0[11]. • Added function LCD_VD[13] to pin P0[19]. • Added function LCD_VD[14] to pin P0[20]. • Added function U4_SCLK to pin P0[21]. • Added function • Added function MOSI to pin P5[0]. • Added function SSP2_MISO to pin P5[1]. • Added EMC dynamic characteristics.			
LPC178X_7X v.1	20110524	Objective data sheet	-	-

22. Contents

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