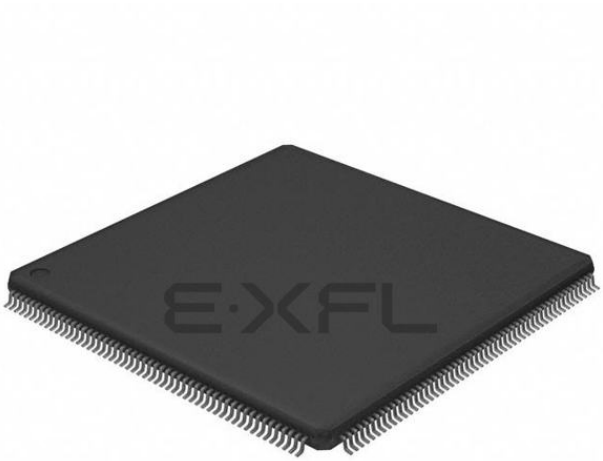

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, Motor Control PWM, POR, PWM, WDT
Number of I/O	165
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1786fbd208-551

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1788			
LPC1788FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1788FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 ´ 15 ´ 0.7 mm	SOT950-1
LPC1788FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1788FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1787			
LPC1787FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1786			
LPC1786FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1785			
LPC1785FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1778			
LPC1778FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1778FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 ´ 15 ´ 0.7 mm	SOT950-1
LPC1778FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1778FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1777			
LPC1777FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1776			
LPC1776FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1776FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1774			
LPC1774FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1774FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[20]	120	M17	K14	83	[3]	I; PU	I/O	**P0[20] —** General purpose digital input/output pin.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I/O	**SD_CMD —** Command line for SD card interface.
							I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
P0[21]	118	M16	K11	82	[3]	I; PU	I/O	**P0[21] —** General purpose digital input/output pin.
							I	**U1_RI —** Ring Indicator input for UART1.
							O	**SD_PWR —** Power Supply Enable for external SD card power supply.
							O	**U4_OE —** RS-485/EIA-485 output enable signal for UART4.
							I	**CAN_RD1 —** CAN1 receiver input.
							I/O	**U4_SCLK —** USART 4 clock input or output in synchronous mode.
P0[22]	116	N17	L14	80	[6]	I; PU	I/O	**P0[22] —** General purpose digital input/output pin.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I/O	**SD_DAT[0] —** Data line 0 for SD card interface.
							O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
							O	**CAN_TD1 —** CAN1 transmitter output.
P0[23]	18	H1	F5	13	[5]	I; PU	I/O	**P0[23] —** General purpose digital input/output pin.
							I	**ADC0_IN[0] —** A/D converter 0, input 0. When configured as an ADC input, the digital function of the pin must be disabled.
							I/O	**I2S_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P0[24]	16	G2	E1	11	[5]	I; PU	I/O	**P0[24] —** General purpose digital input/output pin.
							I	**ADC0_IN[1] —** A/D converter 0, input 1. When configured as an ADC input, the digital function of the pin must be disabled.
							I/O	**I2S_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I	**T3_CAP1 —** Capture input for Timer 3, channel 1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[8]	190	C7	B6	132	[3]	I; PU	I/O	**P1[8] —** General purpose digital input/output pin.
							I	**ENET_CRS (ENET_CRS_DV) —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							-	**R —** Function reserved.
							O	**T3_MAT1 —** Match output for Timer 3, channel 1.
							I/O	**SSP2_SSEL —** Slave Select for SSP2.
P1[9]	188	A6	D7	131	[3]	I; PU	I/O	**P1[9] —** General purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
							-	**R —** Function reserved.
							O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P1[10]	186	C8	A7	129	[3]	I; PU	I/O	**P1[10] —** General purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
							-	**R —** Function reserved.
							I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P1[11]	163	A14	A12	-	[3]	I; PU	I/O	**P1[11] —** General purpose digital input/output pin.
							I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
							I/O	**SD_DAT[2] —** Data line 2 for SD card interface.
							O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
P1[12]	157	A16	A14	-	[3]	I; PU	I/O	**P1[12] —** General purpose digital input/output pin.
							I	**ENET_RXD3 —** Ethernet Receive Data (MII interface).
							I/O	**SD_DAT[3] —** Data line 3 for SD card interface.
							I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
P1[13]	147	D16	D14	-	[3]	I; PU	I/O	**P1[13] —** General purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface).
P1[14]	184	A7	D8	128	[3]	I; PU	I/O	**P1[14] —** General purpose digital input/output pin.
							I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
							-	**R —** Function reserved.
							I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
P1[15]	182	A8	A8	126	[3]	I; PU	I/O	**P1[15] —** General purpose digital input/output pin.
							I	**ENET_RX_CLK (ENET_REF_CLK) —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							-	**R —** Function reserved.
							I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[21]	72	R8	N6	50	[3]	I; PU	I/O	**P1[21] —** General purpose digital input/output pin.
							O	**USB_TX_DM1 —** D− transmit data for USB port 1 (OTG transceiver).
							O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I	**$\overline{\text{MC\_ABORT}}$ —** Motor control PWM, active low fast abort.
							-	**R —** Function reserved.
							O	**LCD_VD[7] —** LCD data.
							O	**LCD_VD[11] —** LCD data.
P1[22]	74	U8	M6	51	[3]	I; PU	I/O	**P1[22] —** General purpose digital input/output pin.
							I	**USB_RCV1 —** Differential receive data for USB port 1 (OTG transceiver).
							I	**USB_PWRD1 —** Power Status for USB port 1 (host power switch).
							O	**T1_MAT0 —** Match output for Timer 1, channel 0.
							O	**MC_0B —** Motor control PWM channel 0, output B.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							O	**LCD_VD[8] —** LCD data.
							O	**LCD_VD[12] —** LCD data.
P1[23]	76	P9	N7	53	[3]	I; PU	I/O	**P1[23] —** General purpose digital input/output pin.
							I	**USB_RX_DP1 —** D+ receive data for USB port 1 (OTG transceiver).
							O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
							I	**QEI_PHB —** Quadrature Encoder Interface PHB input.
							I	**MC_FB1 —** Motor control PWM channel 1 feedback input.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							O	**LCD_VD[9] —** LCD data.
							O	**LCD_VD[13] —** LCD data.
P1[24]	78	T9	P7	54	[3]	I; PU	I/O	**P1[24] —** General purpose digital input/output pin.
							I	**USB_RX_DM1 —** D− receive data for USB port 1 (OTG transceiver).
							O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
							I	**QEI_IDX —** Quadrature Encoder Interface INDEX input.
							I	**MC_FB2 —** Motor control PWM channel 2 feedback input.
							I/O	**SSP0_MOSI —** Master Out Slave in for SSP0.
							O	**LCD_VD[10] —** LCD data.
							O	**LCD_VD[14] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[25]	80	T10	L7	56	[3]	I; PU	I/O	**P1[25] —** General purpose digital input/output pin.
							O	**USB_LS1 —** Low Speed status for USB port 1 (OTG transceiver).
							O	**USB_HSTEN1 —** Host Enabled status for USB port 1.
							O	**T1_MAT1 —** Match output for Timer 1, channel 1.
							O	**MC_1A —** Motor control PWM channel 1, output A.
							O	**CLKOUT —** Selectable clock output.
							O	**LCD_VD[11] —** LCD data.
							O	**LCD_VD[15] —** LCD data.
P1[26]	82	R10	P8	57	[3]	I; PU	I/O	**P1[26] —** General purpose digital input/output pin.
							O	**USB_SSPND1 —** USB port 1 Bus Suspend status (OTG transceiver).
							O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
							I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
							O	**MC_1B —** Motor control PWM channel 1, output B.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							O	**LCD_VD[12] —** LCD data.
							O	**LCD_VD[20] —** LCD data.
P1[27]	88	T12	M9	61	[3]	I; PU	I/O	**P1[27] —** General purpose digital input/output pin.
							I	**USB_INT1 —** USB port 1 OTG transceiver interrupt (OTG transceiver).
							I	**USB_OVRCR1 —** USB port 1 Over-Current status.
							I	**T0_CAP1 —** Capture input for Timer 0, channel 1.
							O	**CLKOUT —** Selectable clock output.
							-	**R —** Function reserved.
							O	**LCD_VD[13] —** LCD data.
							O	**LCD_VD[21] —** LCD data.
P1[28]	90	T13	P10	63	[3]	I; PU	I/O	**P1[28] —** General purpose digital input/output pin.
							I/O	**USB_SCL1 —** USB port 1 I^2C serial clock (OTG transceiver).
							I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
							O	**T0_MAT0 —** Match output for Timer 0, channel 0.
							O	**MC_2A —** Motor control PWM channel 2, output A.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							O	**LCD_VD[14] —** LCD data.
							O	**LCD_VD[22] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P2[1]	152	E14	C14	106	[3]	I; PU	I/O	**P2[1] —** General purpose digital input/output pin.
							O	**PWM1[2] —** Pulse Width Modulator 1, channel 2 output.
							I	**U1_RXD —** Receiver input for UART1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_LE —** Line end signal.
P2[2]	150	D15	E11	105	[3]	I; PU	I/O	**P2[2] —** General purpose digital input/output pin.
							O	**PWM1[3] —** Pulse Width Modulator 1, channel 3 output.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
							-	**R —** Function reserved.
							O	**TRACEDATA[3] —** Trace data, bit 3.
							-	**R —** Function reserved.
							O	**LCD_DCLK —** LCD panel clock.
P2[3]	144	E16	E13	100	[3]	I; PU	I/O	**P2[3] —** General purpose digital input/output pin.
							O	**PWM1[4] —** Pulse Width Modulator 1, channel 4 output.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
							-	**R —** Function reserved.
							O	**TRACEDATA[2] —** Trace data, bit 2.
							-	**R —** Function reserved.
							O	**LCD_FP —** Frame pulse (STN). Vertical synchronization pulse (TFT).
P2[4]	142	D17	E14	99	[3]	I; PU	I/O	**P2[4] —** General purpose digital input/output pin.
							O	**PWM1[5] —** Pulse Width Modulator 1, channel 5 output.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**T2_MAT1 —** Match output for Timer 2, channel 1.
							-	**R —** Function reserved.
							O	**TRACEDATA[1] —** Trace data, bit 1.
							-	**R —** Function reserved.
							O	**LCD_ENAB_M —** STN AC bias drive or TFT data enable output.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P2[23]	64	U5	-	-	[3]	I; PU	I/O	**P2[23] —** General purpose digital input/output pin.
							O	**EMC_DYCS3 —** SDRAM chip select 3.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
							I	**T3_CAP1 —** Capture input for Timer 3, channel 1.
P2[24]	53	P5	P1	-	[3]	I; PU	I/O	**P2[24] —** General purpose digital input/output pin.
							O	**EMC_CKE0 —** SDRAM clock enable 0.
P2[25]	54	R4	P2	-	[3]	I; PU	I/O	**P2[25] —** General purpose digital input/output pin.
							O	**EMC_CKE1 —** SDRAM clock enable 1.
P2[26]	57	T4	-	-	[3]	I; PU	I/O	**P2[26] —** General purpose digital input/output pin.
							O	**EMC_CKE2 —** SDRAM clock enable 2.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
							O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P2[27]	47	P3	-	-	[3]	I; PU	I/O	**P2[27] —** General purpose digital input/output pin.
							O	**EMC_CKE3 —** SDRAM clock enable 3.
							I/O	**SSP0_MOSI —** Master Out Slave In for SSP0.
							O	**T3_MAT1 —** Match output for Timer 3, channel 1.
P2[28]	49	P4	M2	-	[3]	I; PU	I/O	**P2[28] —** General purpose digital input/output pin.
							O	**EMC_DQM0 —** Data mask 0 used with SDRAM and static devices.
P2[29]	43	N3	L1	-	[3]	I; PU	I/O	**P2[29] —** General purpose digital input/output pin.
							O	**EMC_DQM1 —** Data mask 1 used with SDRAM and static devices.
P2[30]	31	L4	-	-	[3]	I; PU	I/O	**P2[30] —** General purpose digital input/output pin.
							O	**EMC_DQM2 —** Data mask 2 used with SDRAM and static devices.
							I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT2 —** Match output for Timer 3, channel 2.
P2[31]	39	N2	-	-	[3]	I; PU	I/O	**P2[31] —** General purpose digital input/output pin.
							O	**EMC_DQM3 —** Data mask 3 used with SDRAM and static devices.
							I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT3 —** Match output for Timer 3, channel 3.
P3[0] to P3[31]							I/O	**Port 3:** Port 3 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the pin connect block.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P3[17]	143	F15	-	-	[3]	I; PU	I/O	**P3[17] —** General purpose digital input/output pin.
							I/O	**EMC_D[17] —** External memory data line 17.
							O	**PWM0[2] —** Pulse Width Modulator 0, output 2.
							I	**U1_RXD —** Receiver input for UART1.
P3[18]	151	C15	-	-	[3]	I; PU	I/O	**P3[18] —** General purpose digital input/output pin.
							I/O	**EMC_D[18] —** External memory data line 18.
							O	**PWM0[3] —** Pulse Width Modulator 0, output 3.
							I	**U1_CTS —** Clear to Send input for UART1.
P3[19]	161	B14	-	-	[3]	I; PU	I/O	**P3[19] —** General purpose digital input/output pin.
							I/O	**EMC_D[19] —** External memory data line 19.
							O	**PWM0[4] —** Pulse Width Modulator 0, output 4.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
P3[20]	167	A13	-	-	[3]	I; PU	I/O	**P3[20] —** General purpose digital input/output pin.
							I/O	**EMC_D[20] —** External memory data line 20.
							O	**PWM0[5] —** Pulse Width Modulator 0, output 5.
							I	**U1_DSR —** Data Set Ready input for UART1.
P3[21]	175	C10	-	-	[3]	I; PU	I/O	**P3[21] —** General purpose digital input/output pin.
							I/O	**EMC_D[21] —** External memory data line 21.
							O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
P3[22]	195	C6	-	-	[3]	I; PU	I/O	**P3[22] —** General purpose digital input/output pin.
							I/O	**EMC_D[22] —** External memory data line 22.
							I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
							I	**U1_RI —** Ring Indicator input for UART1.
P3[23]	65	T6	M4	45	[3]	I; PU	I/O	**P3[23] —** General purpose digital input/output pin.
							I/O	**EMC_D[23] —** External memory data line 23.
							I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
							I	**T0_CAP0 —** Capture input for Timer 0, channel 0.
P3[24]	58	R5	N3	40	[3]	I; PU	I/O	**P3[24] —** General purpose digital input/output pin.
							I/O	**EMC_D[24] —** External memory data line 24.
							O	**PWM1[1] —** Pulse Width Modulator 1, output 1.
							I	**T0_CAP1 —** Capture input for Timer 0, channel 1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P4[29]	176	B10	B9	122	[3]	I; PU	I/O	**P4[29] —** General purpose digital input/output pin.
							O	**EMC_BLS3 —** LOW active Byte Lane select signal 3.
							I	**U3_RXD —** Receiver input for UART3.
							O	**T2_MAT1 —** Match output for Timer 2, channel 1.
							I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
							O	**LCD_VD[7] —** LCD data.
							O	**LCD_VD[11] —** LCD data.
							O	**LCD_VD[3] —** LCD data.
P4[30]	187	B7	C7	130	[3]	I; PU	I/O	**P4[30] —** General purpose digital input/output pin.
							O	**EMC_CS0 —** LOW active Chip Select 0 signal.
P4[31]	193	A4	E7	134	[3]	I; PU	I/O	**P4[31] —** General purpose digital input/output pin.
							O	**EMC_CS1 —** LOW active Chip Select 1 signal.
P5[0] to P5[4]							I/O	**Port 5:** Port 5 is a 5-bit I/O port with individual direction controls for each bit. The operation of port 5 pins depends upon the pin function selected via the pin connect block.
P5[0]	9	F4	E5	6	[3]	I; PU	I/O	**P5[0] —** General purpose digital input/output pin.
							I/O	**EMC_A[24] —** External memory address line 24.
							I/O	**SSP2_MOSI —** Master Out Slave In for SSP2.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
P5[1]	30	J4	H1	21	[3]	I; PU	I/O	**P5[1] —** General purpose digital input/output pin.
							I/O	**EMC_A[25] —** External memory address line 25.
							I/O	**SSP2_MISO —** Master In Slave Out for SSP2.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
P5[2]	117	L14	L12	81	[11]	I	I/O	**P5[2] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output for Timer 3, channel 2.
							-	**R —** Function reserved.
							I/O	**I2C0_SDA —** I^2C0 data input/output (this pin uses a specialized I^2C pad that supports I^2C Fast Mode Plus).

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

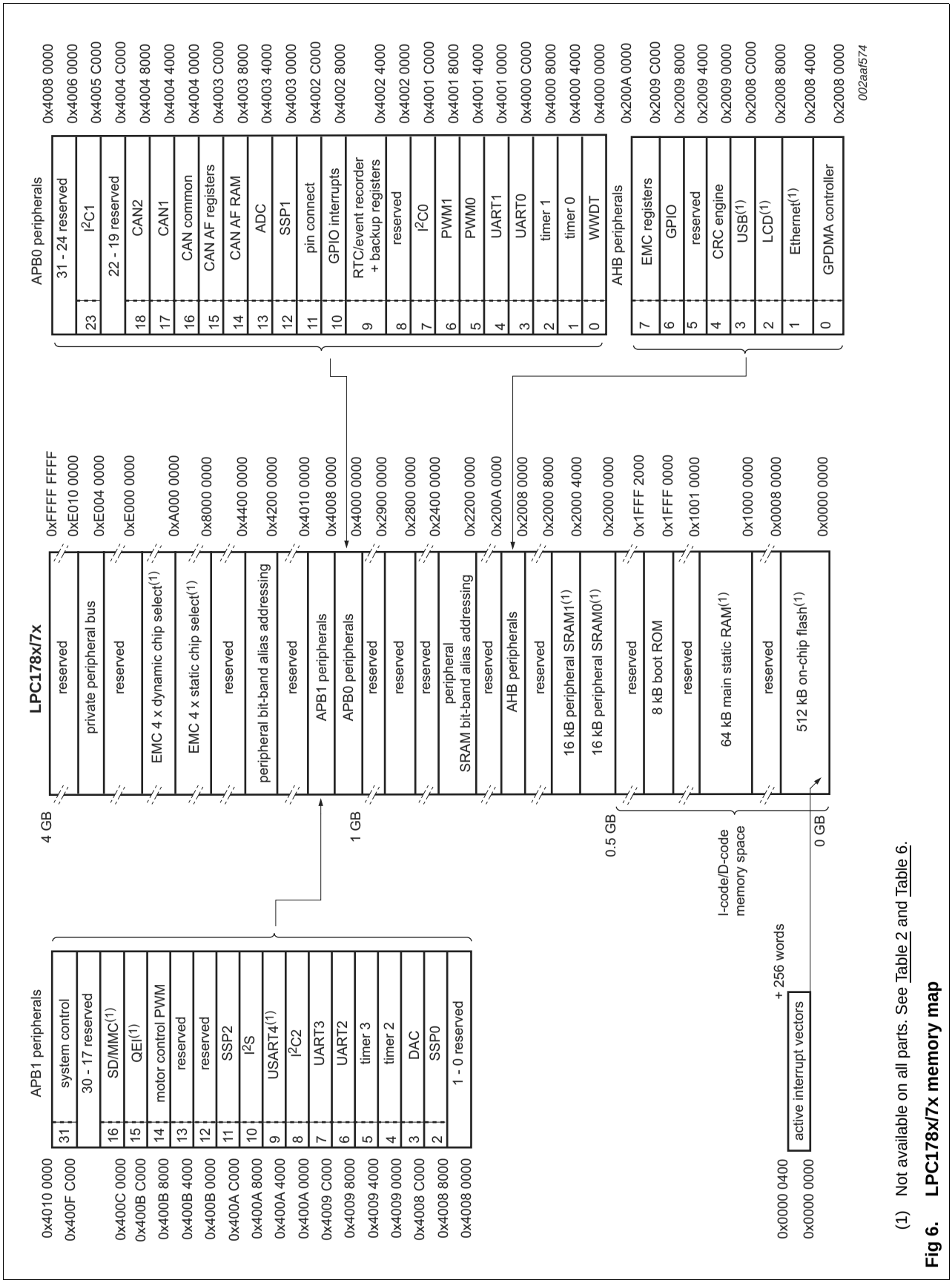
7.7 Memory map

Table 6. LPC178x/177x memory usage and details

Address range	General Use	Address range details and description	
0x0000 0000 to 0x1FFF FFFF	On-chip non-volatile memory	0x0000 0000 - 0x0007 FFFF	For devices with 512 kB of flash memory.
		0x0000 0000 - 0x0003 FFFF	For devices with 256 kB of flash memory.
		0x0000 0000 - 0x0001 FFFF	For devices with 128 kB of flash memory.
		0x0000 0000 - 0x0000 FFFF	For devices with 64 kB of flash memory.
	On-chip main SRAM	0x1000 0000 - 0x1000 FFFF	For devices with 64 kB of main SRAM.
		0x1000 0000 - 0x1000 7FFF	For devices with 32 kB of main SRAM.
		0x1000 0000 - 0x1000 3FFF	For devices with 16 kB of main SRAM.
	Boot ROM	0x1FFF 0000 - 0x1FFF 1FFF	8 kB Boot ROM with flash services.
0x2000 0000 to 0x3FFF FFFF	On-chip SRAM (typically used for peripheral data)	0x2000 0000 - 0x2000 1FFF	Peripheral RAM - bank 0 (first 8 kB)
		0x2000 2000 - 0x2000 3FFF	Peripheral RAM - bank 0 (second 8 kB)
		0x2000 4000 - 0x2000 7FFF	Peripheral RAM - bank 1 (16 kB)
	AHB peripherals	0x2008 0000 - 0x200B FFFF	See Figure 6 for details
0x4000 0000 to 0x7FFF FFFF	APB Peripherals	0x4000 0000 - 0x4007 FFFF	APB0 Peripherals, up to 32 peripheral blocks of 16 kB each.
		0x4008 0000 - 0x400F FFFF	APB1 Peripherals, up to 32 peripheral blocks of 16 kB each.
0x8000 0000 to 0xDFFF FFFF	Off-chip Memory via the External Memory Controller	Four static memory chip selects:	
		0x8000 0000 - 0x83FF FFFF	Static memory chip select 0 (up to 64 MB)
		0x9000 0000 - 0x93FF FFFF	Static memory chip select 1 (up to 64 MB)
		0x9800 0000 - 0x9BFF FFFF	Static memory chip select 2 (up to 64 MB)
		0x9C00 0000 - 0x9FFF FFFF	Static memory chip select 3 (up to 64 MB)
		Four dynamic memory chip selects:	
		0xA000 0000 - 0xAFFF FFFF	Dynamic memory chip select 0 (up to 256MB)
		0xB000 0000 - 0xBFFF FFFF	Dynamic memory chip select 1 (up to 256MB)
		0xC000 0000 - 0xCFFF FFFF	Dynamic memory chip select 2 (up to 256MB)
		0xD000 0000 - 0xDFFF FFFF	Dynamic memory chip select 3 (up to 256MB)
0xE000 0000 to 0xE00F FFFF	Cortex-M3 Private Peripheral Bus	0xE000 0000 - 0xE00F FFFF	Cortex-M3 related functions, includes the NVIC and System Tick Timer.

The LPC178x/7x incorporate several distinct memory regions, shown in the following figures. Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size, and is divided to allow for up to 128 peripherals. The APB peripheral area is 1 MB in size and is divided to allow for up to 64 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.



(1) Not available on all parts. See Table 2 and Table 6.

Fig 6. LPC178x/7x memory map

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the PWMMR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

7.26.1 Features

- LPC178x/7x has two PWM blocks with Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

7.27 Motor control PWM

The LPC178x/7x contain one motor control PWM.

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the

- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Backup registers (20 bytes) powered by VBAT.
- RTC power supply is isolated from the rest of the chip.

7.32 Event monitor/recorder

The event monitor/recorder allows recording of tampering events in sealed product enclosures. Sensors report any attempt to open the enclosure, or to tamper with the device in any other way. The event monitor/recorder stores records of such events when the device is powered only by the backup battery.

7.32.1 Features

- Supports three digital event inputs in the VBAT power domain.
- An event is defined as a level change at the digital event inputs.
- For each event channel, two timestamps mark the first and the last occurrence of an event. Each channel also has a dedicated counter tracking the total number of events. Timestamp values are taken from the RTC.
- Runs in VBAT power domain, independent of system power supply. The event/recorder/monitor can therefore operate in Deep power-down mode.
- Very low power consumption.
- Interrupt available if system is running.
- A qualified event can be used as a wake-up trigger.
- State of event interrupts accessible by software through GPIO.

7.33 Clocking and power control

7.33.1 Crystal oscillators

The LPC178x/7x include four independent oscillators. These are the main oscillator, the IRC oscillator, the watchdog oscillator, and the RTC oscillator.

Following reset, the LPC178x/7x will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the boot loader code to operate at a known frequency.

See Figure 7 for an overview of the LPC178x/7x clock generation.

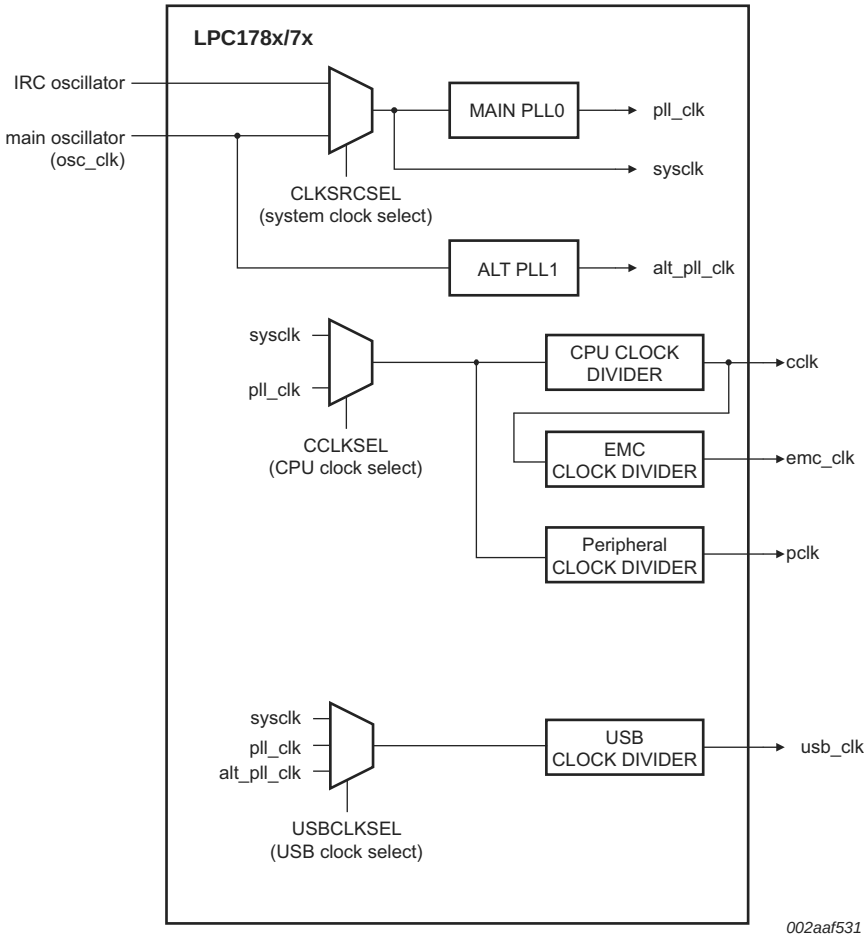


Fig 7. LPC178x/7x clock generation block diagram

7.33.1.1 Internal RC oscillator

The IRC may be used as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC178x/7x use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.33.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator also provides the clock source for the alternate PLL1.

The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the main PLL. The clock selected as the PLL input is PLLCLKIN. The ARM processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The clock frequency for each peripheral can be selected individually and is referred to as PCLK. Refer to Section 7.33.2 for additional information.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

Table 10. Thermal characteristics
V_{DD} = 3.0 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified;

Symbol	Parameter	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature	-	-	125	°C

Table 11. Thermal resistance (LQFP packages)
T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Conditions	Thermal resistance in °C/W ±15 %	
		LQFP208	LQFP144
θja	JEDEC (4.5 in × 4 in)		
	0 m/s	27.4	31.5
	1 m/s	25.7	28.1
	2.5 m/s	24.4	26.2
	Single-layer (4.5 in × 3 in)		
	0 m/s	35.4	43.2
	1 m/s	31.2	35.7
	2.5 m/s	29.2	32.8
θjc	-	8.8	7.8
θjb	-	15.4	13.8

Table 12. Thermal resistance value (TFBGA packages)
T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Conditions	Thermal resistance in °C/W ±15 %	
		TFBGA208	TFBGA180
θja	JEDEC (4.5 in × 4 in)		
	0 m/s	41	45.5
	1 m/s	35	38.3
	2.5 m/s	31	33.8
	8-layer (4.5 in × 3 in)		
	0 m/s	34.9	38
	1 m/s	30.9	33.5
	2.5 m/s	28	29.8
θjc	-	8.3	8.9
θjb	-	13.6	12

11.3 External clock

Table 23. Dynamic characteristic: external clock (see Figure 36)
T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ over specified ranges.

Symbol	Parameter	Min	Typ	Max	Unit
f_{osc}	oscillator frequency	1	12	25	MHz
$T_{cy(clk)}$	clock cycle time	40	83.3	1000	ns
t_{CHCX}	clock HIGH time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time	$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time	-	-	5	ns
t_{CHCL}	clock fall time	-	-	5	ns

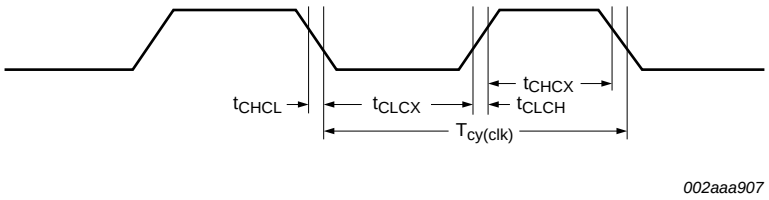


Fig 20. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11.4 Internal oscillators

Table 24. Dynamic characteristic: internal oscillators
T_{amb} = −40 °C to +85 °C; 2.7 V ≤ $V_{DD(REG)(3V3)}$ ≤ 3.6 V.[1]

Symbol	Parameter	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	11.88	12	12.12	MHz
$f_{i(RTC)}$	RTC input frequency	-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.5 I/O pins

Table 25. Dynamic characteristic: I/O pins[1]
C_L = 10 pF; T_{amb} = −40 °C to +85 °C; $V_{DD(3V3)}$ = 3.0 V to 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins.

12. ADC electrical characteristics

Table 31. 12-bit ADC characteristics

V_{DDA} = 2.7 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
12-bit resolution							
E_D	differential linearity error		[2][3][4]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[2][5]	-	-	±6	LSB
E_O	offset error		[2][6]	-	-	±5	LSB
E_G	gain error		[2][7]	-	-	±5	LSB
E_T	absolute error		[2][8]	-	-	< ±8	LSB
$f_{clk(ADC)}$	ADC clock frequency			-	-	12.4	MHz
$f_{c(ADC)}$	ADC conversion frequency	single conversion mode		-	-	400	kSample/s
		burst mode		-	-	375	kSample/s
C_{ia}	analog input capacitance			-	-	5	pF
R_{vsi}	voltage source interface resistance		[9]	-	-	1	kΩ
8-bit resolution[10]							
E_D	differential linearity error		[2][3][4]	-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		[2][5]	-	±1	-	LSB
E_O	offset error		[2][6]	-	±1	-	LSB
E_G	gain error		[2][7]	-	±1	-	LSB
E_T	absolute error		[2][8]	-	-	< ±1.5	LSB
$f_{clk(ADC)}$	ADC clock frequency			-	-	36	MHz
$f_{c(ADC)}$	ADC conversion frequency			-	-	1.16	Msample/s
C_{ia}	analog input capacitance			-	-	5	pF
R_{vsi}	voltage source interface resistance		[9]	-	-	1	kΩ

[1] V_{DDA} and VREFP should be tied to $V_{DD(3V3)}$ if the ADC and DAC are not used.

[2] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[3] The ADC is monotonic, there are no missing codes.

[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 28.

[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 28.

Table 34. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 35. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Smaller values of C_{x1} and C_{x2} should be chosen according to the increase in parasitics of the PCB layout.

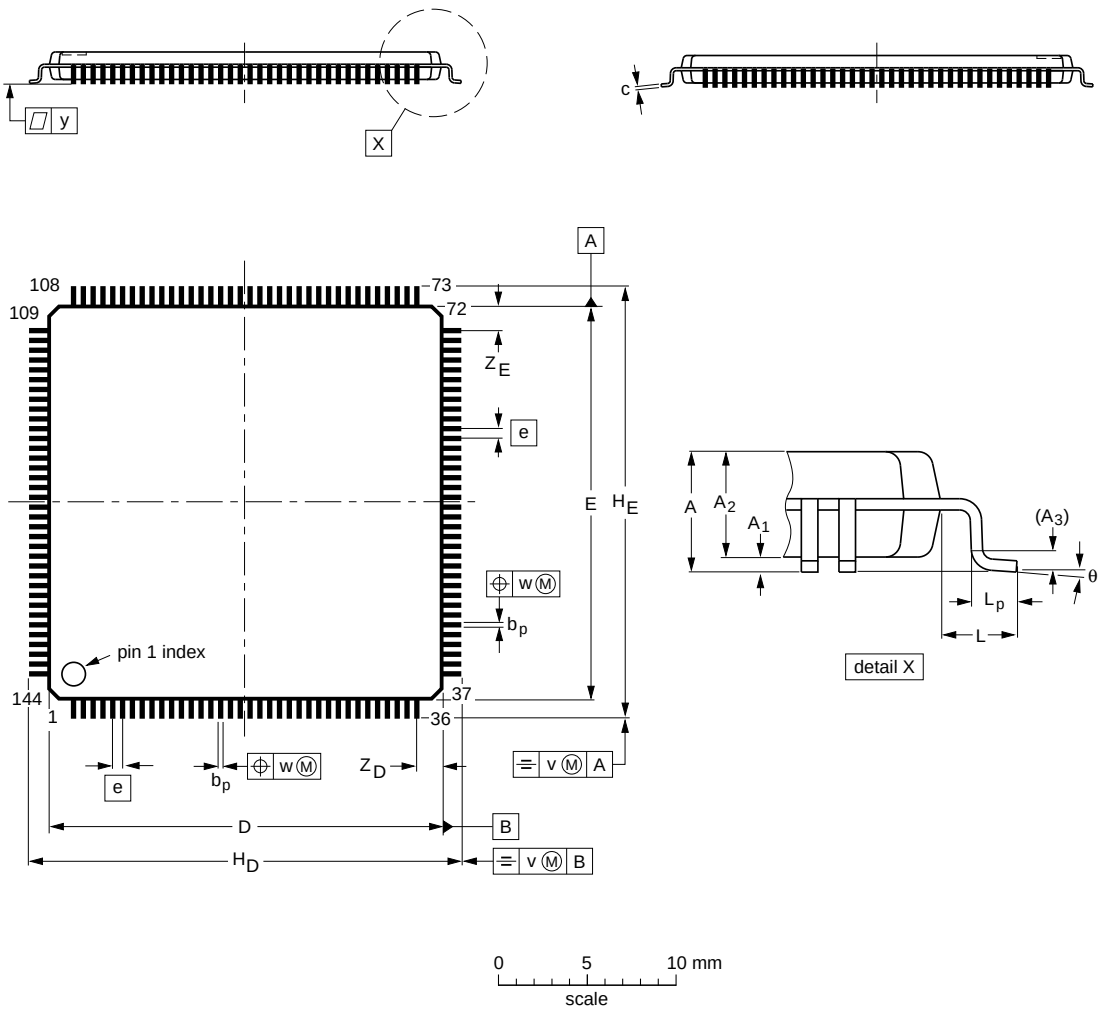
14.4 Standard I/O pin configuration

Figure 38 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver: Open-drain mode enabled/disabled.
- Digital input: Pull-up enabled/disabled.
- Digital input: Pull-down enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Analog input.

The default configuration for standard I/O pins is input with pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 44. LQFP144 package

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC178X_7X v.3	20111220	Objective data sheet	-	LPC178X_7X v.2
Modifications:	• Removed BOOT function from pin P3[14]. • I_{BAT} and $I_{DD(REG)(3V3)}$ updated for Deep power-down mode in Table 13. • Maximum SDRAM clock of 80 MHz specified in Section 2, Table 18, and Table 19. • Power consumption data added (Figure 9 and Figure 10). • Removed parameter Z_{DRV} in Table 13. • Specified maximum value for parameter C_L in Table 33 and remove typical value. • Specified setting of boost bits in Table 14, Table note 5 and in Table 13, Table note 6 . • USB connection diagrams updated (Figure 33 to Figure 36). • Current drain condition on battery supply specified in Section 7.33.6. • Table note 10 in Table 13 updated. • ADC characteristics updated (Table 31). • Section 14.6 “Reset pin configuration for RTC operation” added. • EEPROM size for parts LPC1774 corrected in Table 2 and Figure 1. • Changed function LCD_VD[5] on pin P0[10] to Reserved. • Changed function LCD_VD[10] on pin P0[11] to Reserved. • Changed function LCD_VD[13] on pin P0[19] to Reserved. • Changed function LCD_VD[14] on pin P0[20] to Reserved. • ADC interface model updated (see Table 32 and Figure 30).			
LPC178X_7X v.2	20110527	Objective data sheet	-	LPC178X_7X v.1
Modifications:	• Symbol names in Table 3 to Table 5 abbreviated. • Reserved functions added in Table 3. • Added function LCD_VD[5] to pin P0[10]. • Added function LCD_VD[10] to pin P0[11]. • Added function LCD_VD[13] to pin P0[19]. • Added function LCD_VD[14] to pin P0[20]. • Added function U4_SCLK to pin P0[21]. • Added function • Added function MOSI to pin P5[0]. • Added function SSP2_MISO to pin P5[1]. • Added EMC dynamic characteristics.			
LPC178X_7X v.1	20110524	Objective data sheet	-	-