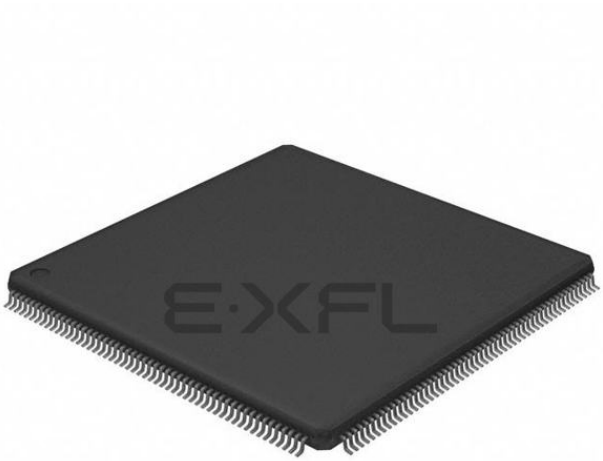


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, Motor Control PWM, POR, PWM, WDT
Number of I/O	165
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1787fbd208-551

- Multilayer AHB matrix interconnect provides a separate bus for each AHB master. AHB masters include the CPU, USB, Ethernet, and the General Purpose DMA controller. This interconnect provides communication with no arbitration delays unless two masters attempt to access the same slave at the same time.
- Split APB bus allows for higher throughput with fewer stalls between the CPU and DMA. A single level of write buffering allows the CPU to continue without waiting for completion of APB writes if the APB was not already busy.
- Cortex-M3 system tick timer, including an external clock input option.
- Standard JTAG test/debug interface as well as Serial Wire Debug and Serial WireTrace Port options.
- Embedded Trace Macrocell (ETM) module supports real-time trace.
- Boundary scan for simplified board testing.
- Non-maskable Interrupt (NMI) input.

- Memory:
  - Up to 512 kB on-chip flash program memory with In-System Programming (ISP) and In-Application Programming (IAP) capabilities. The combination of an enhanced flash memory accelerator and location of the flash memory on the CPU local code/data bus provides high code performance from flash.
  - Up to 96 kB on-chip SRAM includes:

    64 kB of main SRAM on the CPU with local code/data bus for high-performance CPU access.

    Two 16 kB peripheral SRAM blocks with separate access paths for higher throughput. These SRAM blocks may be used for DMA memory as well as for general purpose instruction and data storage.
  - Up to 4032 byte on-chip EEPROM.
- LCD controller, supporting both Super-Twisted Nematic (STN) and Thin-Film Transistors (TFT) displays.
  - Dedicated DMA controller.
  - Selectable display resolution (up to 1024 $\times$ 768 pixels).
  - Supports up to 24-bit true-color mode.
- External Memory Controller (EMC) provides support for asynchronous static memory devices such as RAM, ROM and flash, as well as dynamic memories such as single data rate SDRAM with an SDRAM clock of up to 80 MHz.
- Eight channel General Purpose DMA controller (GPDMA) on the AHB multilayer matrix that can be used with the SSP, I2S, UART, CRC engine, Analog-to-Digital and Digital-to-Analog converter peripherals, timer match signals, GPIO, and for memory-to-memory transfers.
- Serial interfaces:
  - Ethernet MAC with MII/RMII interface and associated DMA controller. These functions reside on an independent AHB.
  - USB 2.0 full-speed dual-port device/host/OTG controller with on-chip PHY and associated DMA controller.
  - Five UARTs with fractional baud rate generation, internal FIFO, DMA support, and RS-485/EIA-485 support. One UART (UART1) has full modem control I/O, and one UART (USART4) supports IrDA, synchronous mode, and a smart card mode conforming to ISO7816-3.
  - Three SSP controllers with FIFO and multi-protocol capabilities. The SSP controllers can be used with the GPDMA.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC1788			
LPC1788FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1788FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 ´ 15 ´ 0.7 mm	SOT950-1
LPC1788FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1788FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1787			
LPC1787FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1786			
LPC1786FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1785			
LPC1785FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1778			
LPC1778FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1778FET208	TFBGA208	plastic thin fine-pitch ball grid array package; 208 balls; body 15 ´ 15 ´ 0.7 mm	SOT950-1
LPC1778FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1778FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC1777			
LPC1777FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1776			
LPC1776FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1776FET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC1774			
LPC1774FBD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC1774FBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

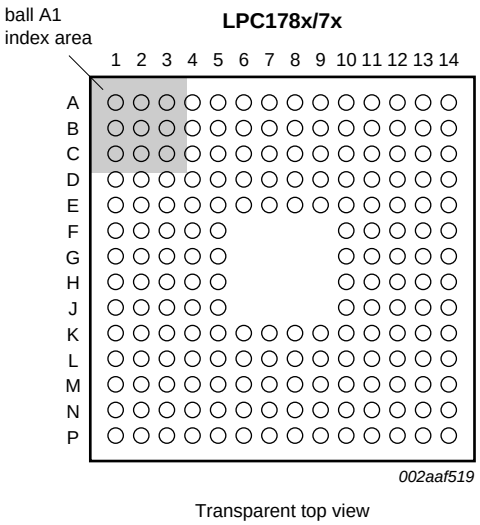


Fig 4. Pin configuration (TFBGA180)

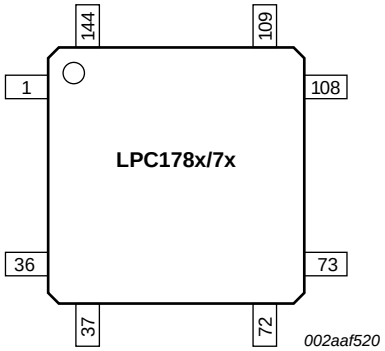


Fig 5. Pin configuration (LQFP144)

6.2 Pin description

I/O pins on the LPC178x/7x are 5 V tolerant and have input hysteresis unless otherwise indicated in the table below. Crystal pins, power pins, and reference voltage pins are not 5 V tolerant. In addition, when pins are selected to be ADC inputs, they are no longer 5 V tolerant and the input voltage must be limited to the voltage at the ADC positive reference pin (VREFP).

All port pins Pn[m] are multiplexed, and the multiplexed functions appear in Table 3 in the order defined by the FUNC bits of the corresponding IOCON register up to the highest used function number. Each port pin can support up to eight multiplexed functions. IOCON register FUNC values which are reserved are noted as ‘R’ in the pin configuration table.

Table 3. Pin description *…continued*

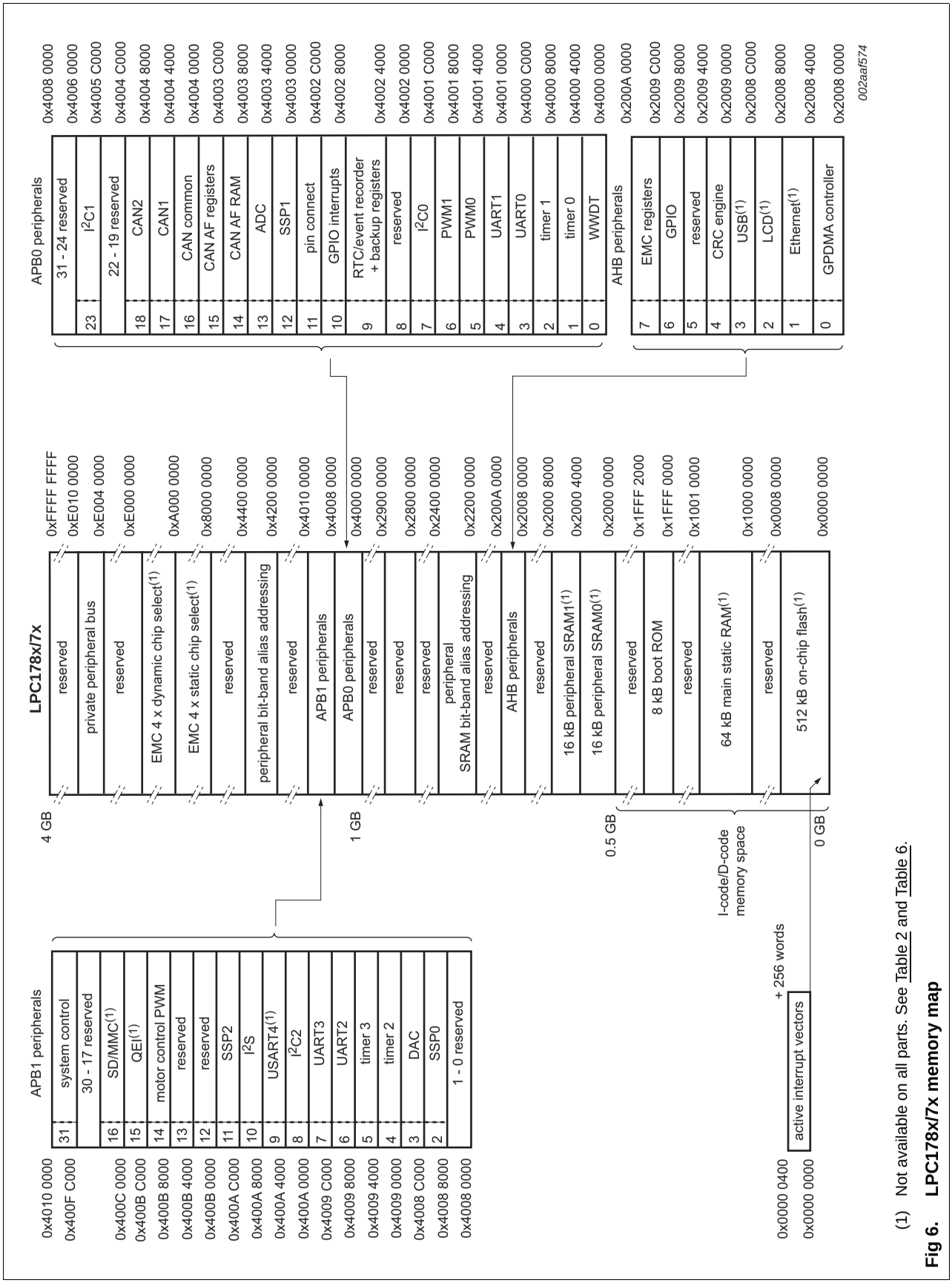
Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P2[5]	140	F16	F12	97	[3]	I; PU	I/O	**P2[5] —** General purpose digital input/output pin.
							O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							O	**T2_MAT0 —** Match output for Timer 2, channel 0.
							-	**R —** Function reserved.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
P2[6]	138	E17	F13	96	[3]	I; PU	I/O	**P2[6] —** General purpose digital input/output pin.
							I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
							I	**U1_RI —** Ring Indicator input for UART1.
							I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
							O	**U2_OE —** RS-485/EIA-485 output enable signal for UART2.
							O	**TRACECLK —** Trace clock.
							O	**LCD_VD[0] —** LCD data.
							O	**LCD_VD[4] —** LCD data.
P2[7]	136	G16	G11	95	[3]	I; PU	I/O	**P2[7] —** General purpose digital input/output pin.
							I	**CAN_RD2 —** CAN2 receiver input.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[1] —** LCD data.
							O	**LCD_VD[5] —** LCD data.
P2[8]	134	H15	G14	93	[3]	I; PU	I/O	**P2[8] —** General purpose digital input/output pin.
							O	**CAN_TD2 —** CAN2 transmitter output.
							O	**U2_TXD —** Transmitter output for UART2.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**ENET_MDC —** Ethernet MIIM clock.
							-	**R —** Function reserved.
							O	**LCD_VD[2] —** LCD data.
							O	**LCD_VD[6] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P4[1]	79	U10	M7	55	[3]	I; PU	I/O	**P4[1] —** General purpose digital input/output pin.
							I/O	**EMC_A[1] —** External memory address line 1.
P4[2]	83	T11	M8	58	[3]	I; PU	I/O	**P4[2] —** General purpose digital input/output pin.
							I/O	**EMC_A[2] —** External memory address line 2.
P4[3]	97	U16	K9	68	[3]	I; PU	I/O	**P4[3] —** General purpose digital input/output pin.
							I/O	**EMC_A[3] —** External memory address line 3.
P4[4]	103	R15	P13	72	[3]	I; PU	I/O	**P4[4] —** General purpose digital input/output pin.
							I/O	**EMC_A[4] —** External memory address line 4.
P4[5]	107	R16	H10	74	[3]	I; PU	I/O	**P4[5] —** General purpose digital input/output pin.
							I/O	**EMC_A[5] —** External memory address line 5.
P4[6]	113	M14	K10	78	[3]	I; PU	I/O	**P4[6] —** General purpose digital input/output pin.
							I/O	**EMC_A[6] —** External memory address line 6.
P4[7]	121	L16	K12	84	[3]	I; PU	I/O	**P4[7] —** General purpose digital input/output pin.
							I/O	**EMC_A[7] —** External memory address line 7.
P4[8]	127	J17	J11	88	[3]	I; PU	I/O	**P4[8] —** General purpose digital input/output pin.
							I/O	**EMC_A[8] —** External memory address line 8.
P4[9]	131	H17	H12	91	[3]	I; PU	I/O	**P4[9] —** General purpose digital input/output pin.
							I/O	**EMC_A[9] —** External memory address line 9.
P4[10]	135	G17	G12	94	[3]	I; PU	I/O	**P4[10] —** General purpose digital input/output pin.
							I/O	**EMC_A[10] —** External memory address line 10.
P4[11]	145	F14	F11	101	[3]	I; PU	I/O	**P4[11] —** General purpose digital input/output pin.
							I/O	**EMC_A[11] —** External memory address line 11.
P4[12]	149	C16	F10	104	[3]	I; PU	I/O	**P4[12] —** General purpose digital input/output pin.
							I/O	**EMC_A[12] —** External memory address line 12.
P4[13]	155	B16	B14	108	[3]	I; PU	I/O	**P4[13] —** General purpose digital input/output pin.
							I/O	**EMC_A[13] —** External memory address line 13.
P4[14]	159	B15	E8	110	[3]	I; PU	I/O	**P4[14] —** General purpose digital input/output pin.
							I/O	**EMC_A[14] —** External memory address line 14.
P4[15]	173	A11	C10	120	[3]	I; PU	I/O	**P4[15] —** General purpose digital input/output pin.
							I/O	**EMC_A[15] —** External memory address line 15.
P4[16]	101	U17	N12	-	[3]	I; PU	I/O	**P4[16] —** General purpose digital input/output pin.
							I/O	**EMC_A[16] —** External memory address line 16.
P4[17]	104	P14	N13	-	[3]	I; PU	I/O	**P4[17] —** General purpose digital input/output pin.
							I/O	**EMC_A[17] —** External memory address line 17.
P4[18]	105	P15	P14	-	[3]	I; PU	I/O	**P4[18] —** General purpose digital input/output pin.
							I/O	**EMC_A[18] —** External memory address line 18.



(1) Not available on all parts. See Table 2 and Table 6.

Fig 6. LPC178x/7x memory map

The LPC178x/7x EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

See Table 6 for EMC memory access.

7.10.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.11 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral and can be accessed through the AHB master. The GPDMA controller allows data transfers between the various on-chip SRAM areas and supports the SD/MMC card interface, all SSPs, the I^2S, all UARTs, the A/D Converter, and the D/A Converter peripherals. DMA can also be triggered by selected timer match conditions. Memory-to-memory transfers and transfers to or from GPIO are supported.

- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

7.13 LCD controller

Remark: The LCD controller is available on parts LPC1788/87/86/85.

The LCD controller provides all of the necessary control signals to interface directly to a variety of color and monochrome LCD panels. Both STN (single and dual panel) and TFT panels can be operated. The display resolution is selectable and can be up to 1024 × 768 pixels. Several color modes are provided, up to a 24-bit true-color non-palettized mode. An on-chip 512-byte color palette allows reducing bus utilization (i.e. memory size of the displayed data) while still supporting a large number of colors.

The LCD interface includes its own DMA controller to allow it to operate independently of the CPU and other system functions. A built-in FIFO acts as a buffer for display data, providing flexibility for system timing. Hardware cursor support can further reduce the amount of CPU time needed to operate the display.

7.13.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized, for color STN and TFT.
- 24 bpp true-color non-palettized, for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.14 Ethernet

Remark: The Ethernet block is available on parts LPC1788/86 and LPC1778/76.

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share the ARM Cortex-M3 D-code and system bus through the AHB-multilayer matrix to access the various on-chip SRAM blocks for Ethernet data, control, and status information.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Media Independent Interface (MII) or Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.14.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame suppor
  - .
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching.
  - Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.

- Physical interface:
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

7.15 USB interface

Remark: The USB Device/Host/OTG controller is available on parts LPC1788/87/86/85 and LPC1778/77/76. The USB Device-only controller is available on parts LPC1774.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

Details on typical USB interfacing solutions can be found in Section 14.1.

7.15.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the USB RAM.

7.15.1.1 Features

- Fully compliant with *USB 2.0 Specification* (full speed).
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the LPC178x/7x can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

7.15.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

7.15.2.1 Features

- OHCI compliant.

- Dedicated power supply pin can be connected to a battery or to the main 3.3 V.
- Periodic interrupts can be generated from increments of any field of the time registers.
- Backup registers (20 bytes) powered by VBAT.
- RTC power supply is isolated from the rest of the chip.

7.32 Event monitor/recorder

The event monitor/recorder allows recording of tampering events in sealed product enclosures. Sensors report any attempt to open the enclosure, or to tamper with the device in any other way. The event monitor/recorder stores records of such events when the device is powered only by the backup battery.

7.32.1 Features

- Supports three digital event inputs in the VBAT power domain.
- An event is defined as a level change at the digital event inputs.
- For each event channel, two timestamps mark the first and the last occurrence of an event. Each channel also has a dedicated counter tracking the total number of events. Timestamp values are taken from the RTC.
- Runs in VBAT power domain, independent of system power supply. The event/recorder/monitor can therefore operate in Deep power-down mode.
- Very low power consumption.
- Interrupt available if system is running.
- A qualified event can be used as a wake-up trigger.
- State of event interrupts accessible by software through GPIO.

7.33 Clocking and power control

7.33.1 Crystal oscillators

The LPC178x/7x include four independent oscillators. These are the main oscillator, the IRC oscillator, the watchdog oscillator, and the RTC oscillator.

Following reset, the LPC178x/7x will operate from the Internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the boot loader code to operate at a known frequency.

See Figure 7 for an overview of the LPC178x/7x clock generation.

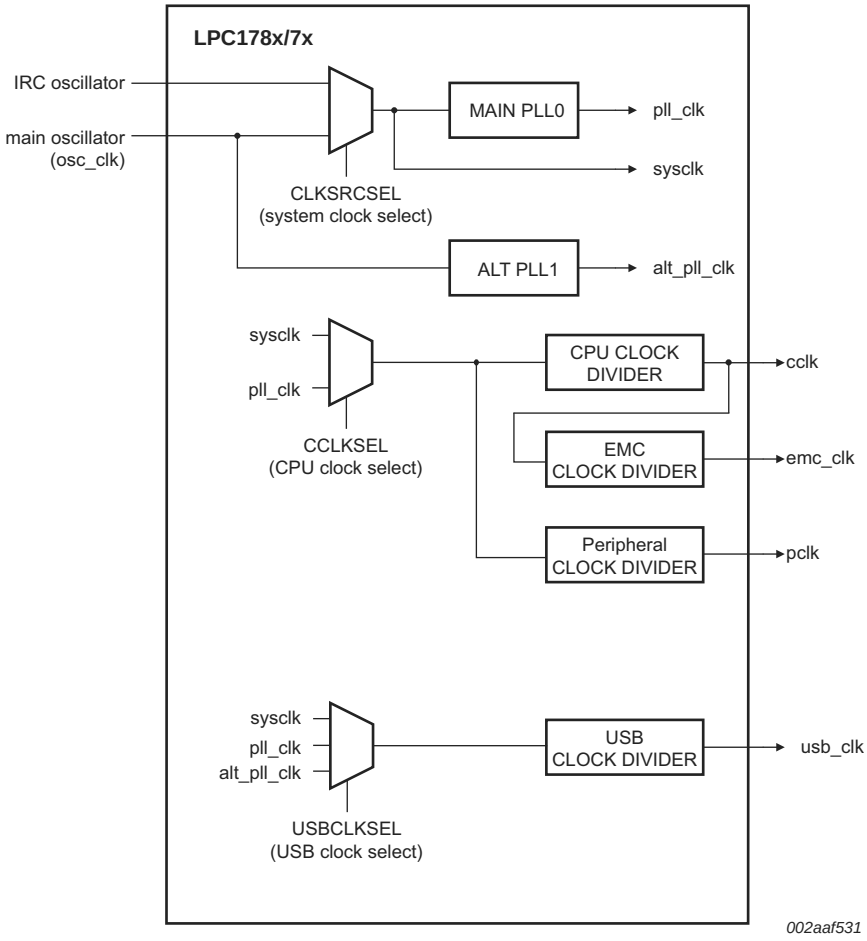


Fig 7. LPC178x/7x clock generation block diagram

7.33.1.1 Internal RC oscillator

The IRC may be used as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the LPC178x/7x use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.33.1.2 Main oscillator

The main oscillator can be used as the clock source for the CPU, with or without using the PLL. The main oscillator also provides the clock source for the alternate PLL1.

The main oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the main PLL. The clock selected as the PLL input is PLLCLKIN. The ARM processor clock frequency is referred to as CCLK elsewhere in this document. The frequencies of PLLCLKIN and CCLK are the same value unless the PLL is active and connected. The clock frequency for each peripheral can be selected individually and is referred to as PCLK. Refer to Section 7.33.2 for additional information.

The alternate PLL accepts an input clock frequency from the main oscillator in the range of 10 MHz to 25 MHz only. When used as the USB clock, the input frequency is multiplied up to a multiple of 48 MHz (192 MHz or 288 MHz as described above).

7.33.3 Wake-up timer

The LPC178x/7x begin operation at power-up and when awakened from Power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

When the main oscillator is initially activated, the wake-up timer allows software to ensure that the main oscillator is fully functional before the processor uses it as a clock source and starts to execute instructions. This is important at power on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the wake-up Timer.

The wake-up timer monitors the crystal oscillator to check whether it is safe to begin code execution. When power is applied to the chip, or when some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of $V_{DD(3V3)}$ ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g., capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

7.33.4 Power control

The LPC178x/7x support a variety of power control features. There are four special modes of processor power reduction: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, the peripheral power control allows shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Each of the peripherals has its own clock divider which provides even better power control.

The integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep-sleep, Power-down, and Deep power-down modes.

The LPC178x/7x also implement a separate power domain to allow turning off power to the bulk of the device while maintaining operation of the RTC and a small set of registers for storing data during any of the power-down modes.

7.33.4.1 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence other than re-enabling the clock to the ARM core.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this, four IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 12 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. Users need to reconfigure the PLL and clock dividers accordingly.

7.33.4.4 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

To optimize power conservation, the user has the additional option of turning off or retaining power to the 32 kHz oscillator. It is also possible to use external circuitry to turn off power to the on-chip regulator via the $V_{DD(REG)(3V3)}$ pins and/or the I/O power via the $V_{DD(3V3)}$ pins after entering Deep Power-down mode. Power must be restored before device operation can be restarted.

The LPC178x/7x can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

7.33.4.5 Wake-up Interrupt Controller (WIC)

The WIC allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep-sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC.This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

7.33.5 Peripheral power control

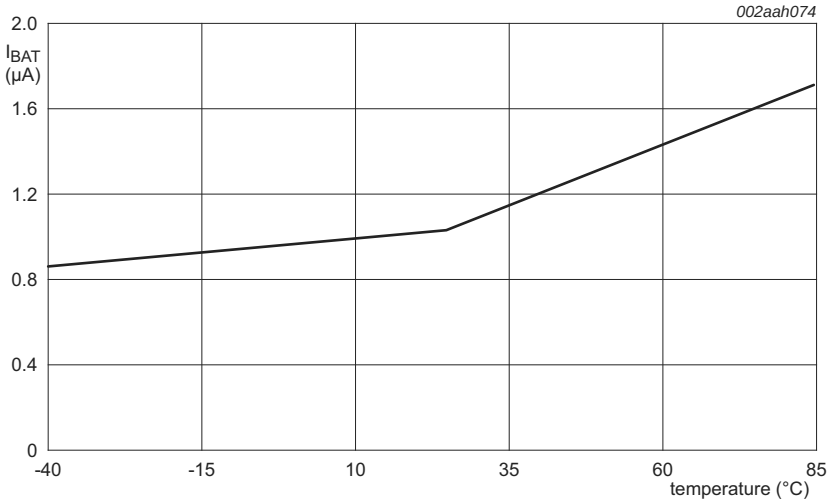
A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

7.33.6 Power domains

The LPC178x/7x provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup registers.

On the LPC178x/7x, I/O pads are powered by $V_{DD(3V3)}$, while $V_{DD(REG)(3V3)}$ powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC178x/7x application, a design can use two power options to manage power consumption.



Conditions: $V_{DD(REG)(3V3)} = V_{DDA} = V_{DD(3V3)} = 0$; $V_{BAT} = 3.0$ V.

Fig 11. Part powered off: Typical battery supply current (I_{BAT}) versus temperature

11. Dynamic characteristics

11.1 Flash memory

Table 15. Flash characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance	-	[1]	10000	100000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		20	-	-	years
t_{er}	erase time	sector or multiple consecutive sectors		95	100	105	ms
t_{prog}	programming time	-	[2]	0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash. Data must be written to the flash in blocks of 256 bytes.

Table 16. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; $V_{DD(REG)(3V3)}$ = 2.7 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency	-		200	375	400	kHz
N_{endu}	endurance	-		100000	500000	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	64 bytes	[1]	-	1.8	-	ms
t_{prog}	programming time	64 bytes	[1]	-	1.1	-	ms

[1] EEPROM clock frequency = 375 kHz. Programming/erase times increase with decreasing EEPROM clock frequency.

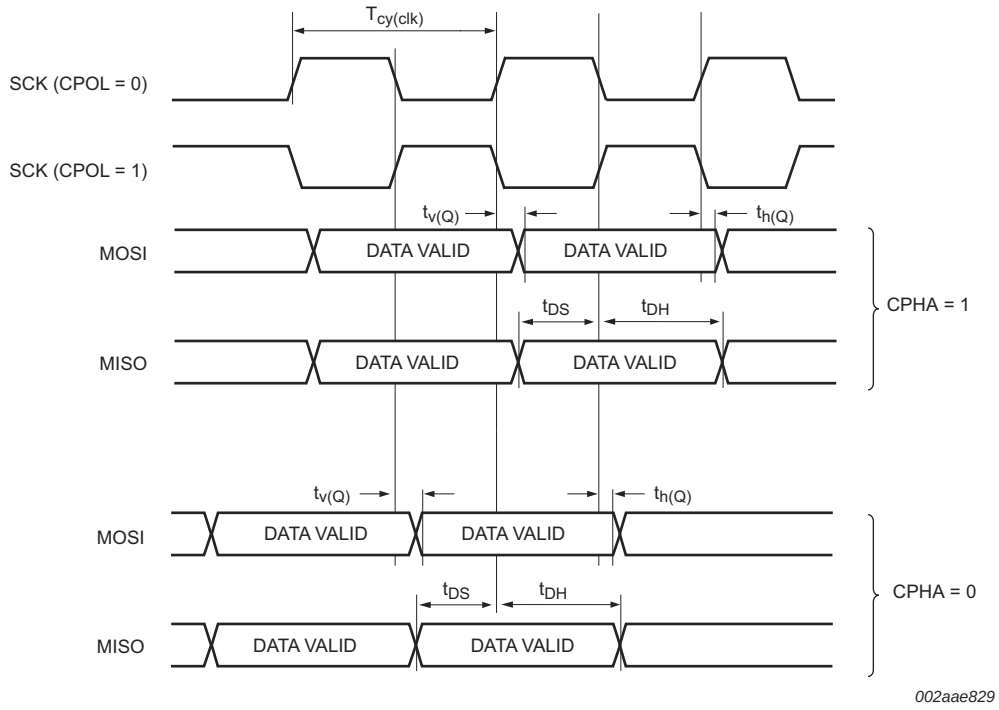


Fig 21. SSP master timing in SPI mode

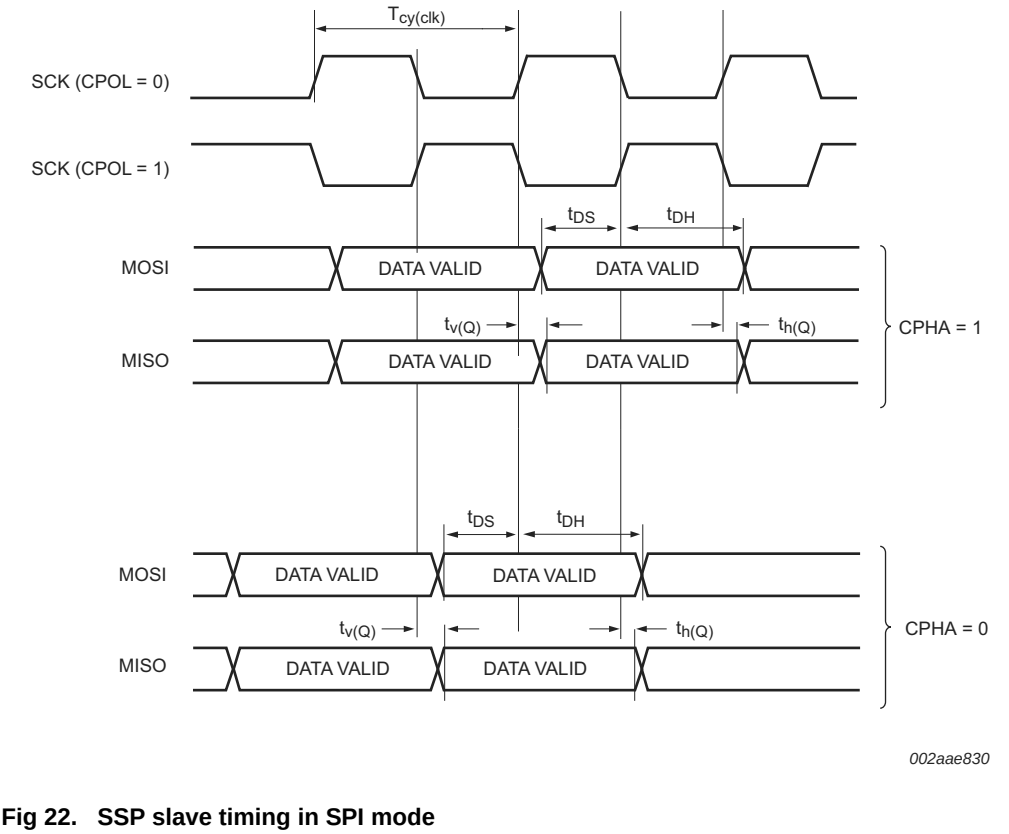


Fig 22. SSP slave timing in SPI mode

11.7 I²C-bus

Table 27. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = −40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

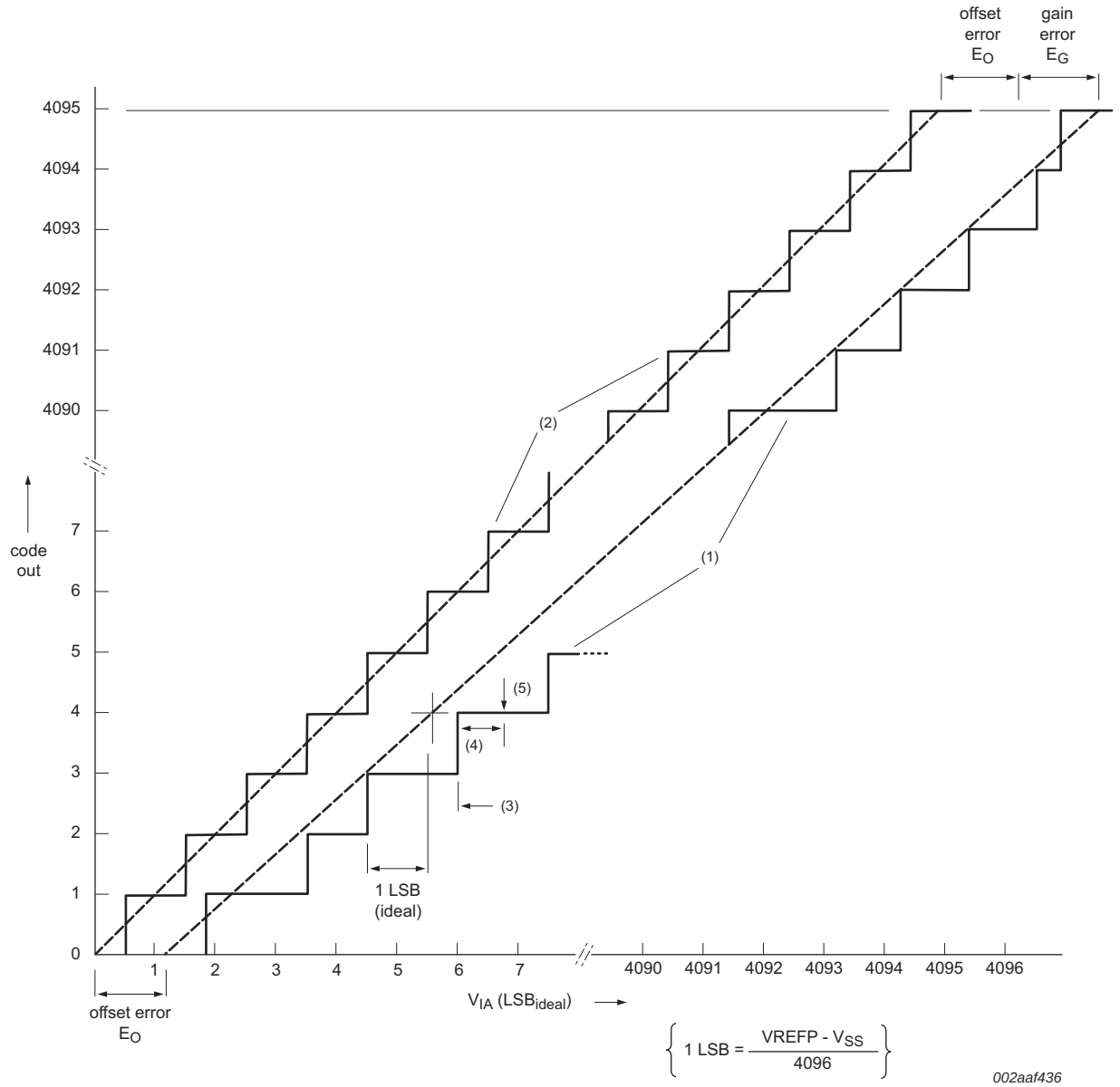
[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 28. 12-bit ADC characteristics

18. References

[1] LPC178x/7x User manual UM10470:
http://www.nxp.com/documents/user_manual/UM10470.pdf

[2] LPC177x/8x Errata sheet:
http://www.nxp.com/documents/errata_sheet/ES_LPC177X_8X.pdf

[3] Technical note ADC design guidelines:
http://www.nxp.com/documents/technical_note/TN00009.pdf