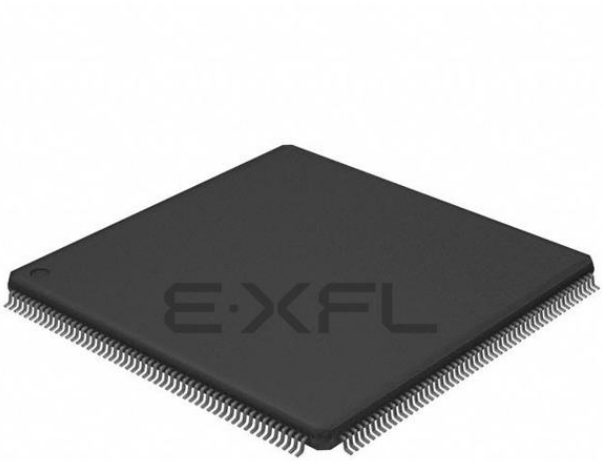


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, Motor Control PWM, POR, PWM, WDT
Number of I/O	165
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1788fbd208-551

- The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, PORT0/2 pin interrupt, and NMI).
- Brownout detect with separate threshold for interrupt and forced reset.
- On-chip Power-On Reset (POR).

- Clock generation:
  - Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, USB clock, or the watchdog timer clock.
  - On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC oscillator (IRC) trimmed to 1% accuracy that can optionally be used as a system clock.
  - An on-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator or the internal RC oscillator.
  - A second, dedicated PLL may be used for USB interface in order to allow added flexibility for the Main PLL settings.
- Versatile pin function selection feature allows many possibilities for using on-chip peripheral functions.
- Unique device serial number for identification purposes.
- Single 3.3 V power supply (2.4 V to 3.6 V). Temperature range of −40 °C to 85 °C.
- Available as LQFP208, TFBGA208, TFBGA180, and LQFP144 package.

3. Applications

- Communications:
  - Point-of-sale terminals, web servers, multi-protocol bridges
- Industrial/Medical:
  - Automation controllers, application control, robotics control, HVAC, PLC, inverters, circuit breakers, medical scanning, security monitoring, motor drive, video intercom
- Consumer/Appliance:
  - Audio, MP3 decoders, alarm systems, displays, printers, scanners, small appliances, fitness equipment
- Automotive:
  - After-market, car alarms, GPS/fleet monitors

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[20]	120	M17	K14	83	[3]	I; PU	I/O	**P0[20] —** General purpose digital input/output pin.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I/O	**SD_CMD —** Command line for SD card interface.
							I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
P0[21]	118	M16	K11	82	[3]	I; PU	I/O	**P0[21] —** General purpose digital input/output pin.
							I	**U1_RI —** Ring Indicator input for UART1.
							O	**SD_PWR —** Power Supply Enable for external SD card power supply.
							O	**U4_OE —** RS-485/EIA-485 output enable signal for UART4.
							I	**CAN_RD1 —** CAN1 receiver input.
							I/O	**U4_SCLK —** USART 4 clock input or output in synchronous mode.
P0[22]	116	N17	L14	80	[6]	I; PU	I/O	**P0[22] —** General purpose digital input/output pin.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							I/O	**SD_DAT[0] —** Data line 0 for SD card interface.
							O	**U4_TXD —** Transmitter output for USART4 (input/output in smart card mode).
							O	**CAN_TD1 —** CAN1 transmitter output.
P0[23]	18	H1	F5	13	[5]	I; PU	I/O	**P0[23] —** General purpose digital input/output pin.
							I	**ADC0_IN[0] —** A/D converter 0, input 0. When configured as an ADC input, the digital function of the pin must be disabled.
							I/O	**I2S_RX_SCK —** Receive Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P0[24]	16	G2	E1	11	[5]	I; PU	I/O	**P0[24] —** General purpose digital input/output pin.
							I	**ADC0_IN[1] —** A/D converter 0, input 1. When configured as an ADC input, the digital function of the pin must be disabled.
							I/O	**I2S_RX_WS —** Receive Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I	**T3_CAP1 —** Capture input for Timer 3, channel 1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P1[8]	190	C7	B6	132	[3]	I; PU	I/O	**P1[8] —** General purpose digital input/output pin.
							I	**ENET_CRS (ENET_CRS_DV) —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							-	**R —** Function reserved.
							O	**T3_MAT1 —** Match output for Timer 3, channel 1.
							I/O	**SSP2_SSEL —** Slave Select for SSP2.
P1[9]	188	A6	D7	131	[3]	I; PU	I/O	**P1[9] —** General purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
							-	**R —** Function reserved.
							O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P1[10]	186	C8	A7	129	[3]	I; PU	I/O	**P1[10] —** General purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1 (RMII/MII interface).
							-	**R —** Function reserved.
							I	**T3_CAP0 —** Capture input for Timer 3, channel 0.
P1[11]	163	A14	A12	-	[3]	I; PU	I/O	**P1[11] —** General purpose digital input/output pin.
							I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
							I/O	**SD_DAT[2] —** Data line 2 for SD card interface.
							O	**PWM0[6] —** Pulse Width Modulator 0, output 6.
P1[12]	157	A16	A14	-	[3]	I; PU	I/O	**P1[12] —** General purpose digital input/output pin.
							I	**ENET_RXD3 —** Ethernet Receive Data (MII interface).
							I/O	**SD_DAT[3] —** Data line 3 for SD card interface.
							I	**PWM0_CAP0 —** Capture input for PWM0, channel 0.
P1[13]	147	D16	D14	-	[3]	I; PU	I/O	**P1[13] —** General purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet Receive Data Valid (MII interface).
P1[14]	184	A7	D8	128	[3]	I; PU	I/O	**P1[14] —** General purpose digital input/output pin.
							I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
							-	**R —** Function reserved.
							I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
P1[15]	182	A8	A8	126	[3]	I; PU	I/O	**P1[15] —** General purpose digital input/output pin.
							I	**ENET_RX_CLK (ENET_REF_CLK) —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							-	**R —** Function reserved.
							I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P2[9]	132	H16	H11	92	[3]	I; PU	I/O	**P2[9] —** General purpose digital input/output pin.
							O	**USB_CONNECT1 —** USB1 SoftConnect control. Signal used to switch an external 1.5 kΩ resistor under the software control. Used with the SoftConnect USB feature.
							I	**U2_RXD —** Receiver input for UART2.
							I	**U4_RXD —** Receiver input for USART4.
							I/O	**ENET_MDIO —** Ethernet MIIM data input and output.
							-	**R —** Function reserved.
							I	**LCD_VD[3] —** LCD data.
							I	**LCD_VD[7] —** LCD data.
P2[10]	110	N15	M13	76	[10]	I; PU	I/O	**P2[10] —** General purpose digital input/output pin. This pin includes a 10 ns input . A LOW on this pin while $\overline{\text{RESET}}$ is LOW forces the on-chip boot loader to take over control of the part after a reset and go into ISP mode.
							I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.
							I	**NMI —** Non-maskable interrupt input.
P2[11]	108	T17	M12	75	[10]	I; PU	I/O	**P2[11] —** General purpose digital input/output pin. This pin includes a 10 ns input glitch filter.
							I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.
							I/O	**SD_DAT[1] —** Data line 1 for SD card interface.
							I/O	**I2S_TX_SCK —** Transmit Clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_CLKIN —** LCD clock.
P2[12]	106	N14	N14	73	[10]	I; PU	I/O	**P2[12] —** General purpose digital input/output pin. This pin includes a 10 ns input glitch filter.
							I	**$\overline{\text{EINT2}}$ —** External interrupt 2 input.
							I/O	**SD_DAT[2] —** Data line 2 for SD card interface.
							I/O	**I2S_TX_WS —** Transmit Word Select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							O	**LCD_VD[4] —** LCD data.
							O	**LCD_VD[3] —** LCD data.
							O	**LCD_VD[8] —** LCD data.
							O	**LCD_VD[18] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P4[1]	79	U10	M7	55	[3]	I; PU	I/O	**P4[1] —** General purpose digital input/output pin.
							I/O	**EMC_A[1] —** External memory address line 1.
P4[2]	83	T11	M8	58	[3]	I; PU	I/O	**P4[2] —** General purpose digital input/output pin.
							I/O	**EMC_A[2] —** External memory address line 2.
P4[3]	97	U16	K9	68	[3]	I; PU	I/O	**P4[3] —** General purpose digital input/output pin.
							I/O	**EMC_A[3] —** External memory address line 3.
P4[4]	103	R15	P13	72	[3]	I; PU	I/O	**P4[4] —** General purpose digital input/output pin.
							I/O	**EMC_A[4] —** External memory address line 4.
P4[5]	107	R16	H10	74	[3]	I; PU	I/O	**P4[5] —** General purpose digital input/output pin.
							I/O	**EMC_A[5] —** External memory address line 5.
P4[6]	113	M14	K10	78	[3]	I; PU	I/O	**P4[6] —** General purpose digital input/output pin.
							I/O	**EMC_A[6] —** External memory address line 6.
P4[7]	121	L16	K12	84	[3]	I; PU	I/O	**P4[7] —** General purpose digital input/output pin.
							I/O	**EMC_A[7] —** External memory address line 7.
P4[8]	127	J17	J11	88	[3]	I; PU	I/O	**P4[8] —** General purpose digital input/output pin.
							I/O	**EMC_A[8] —** External memory address line 8.
P4[9]	131	H17	H12	91	[3]	I; PU	I/O	**P4[9] —** General purpose digital input/output pin.
							I/O	**EMC_A[9] —** External memory address line 9.
P4[10]	135	G17	G12	94	[3]	I; PU	I/O	**P4[10] —** General purpose digital input/output pin.
							I/O	**EMC_A[10] —** External memory address line 10.
P4[11]	145	F14	F11	101	[3]	I; PU	I/O	**P4[11] —** General purpose digital input/output pin.
							I/O	**EMC_A[11] —** External memory address line 11.
P4[12]	149	C16	F10	104	[3]	I; PU	I/O	**P4[12] —** General purpose digital input/output pin.
							I/O	**EMC_A[12] —** External memory address line 12.
P4[13]	155	B16	B14	108	[3]	I; PU	I/O	**P4[13] —** General purpose digital input/output pin.
							I/O	**EMC_A[13] —** External memory address line 13.
P4[14]	159	B15	E8	110	[3]	I; PU	I/O	**P4[14] —** General purpose digital input/output pin.
							I/O	**EMC_A[14] —** External memory address line 14.
P4[15]	173	A11	C10	120	[3]	I; PU	I/O	**P4[15] —** General purpose digital input/output pin.
							I/O	**EMC_A[15] —** External memory address line 15.
P4[16]	101	U17	N12	-	[3]	I; PU	I/O	**P4[16] —** General purpose digital input/output pin.
							I/O	**EMC_A[16] —** External memory address line 16.
P4[17]	104	P14	N13	-	[3]	I; PU	I/O	**P4[17] —** General purpose digital input/output pin.
							I/O	**EMC_A[17] —** External memory address line 17.
P4[18]	105	P15	P14	-	[3]	I; PU	I/O	**P4[18] —** General purpose digital input/output pin.
							I/O	**EMC_A[18] —** External memory address line 18.

Table 7. External memory controller pin configuration

Part	Data bus pins	Address bus pins	Control pins	
			SRAM	SDRAM
LPC1788FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1788FET208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1788FET180	EMC_D[15:0]	EMC_A[19:0]	EMC_BLS[1:0], EMC_CS[1:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC1788FBD144	EMC_D[7:0]	EMC_A[15:0]	EMC_BLS[3:2], EMC_CS[1:0], EMC_OE, EMC_WE	not available
LPC1787FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS_[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1786FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1785FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1778FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1778FET208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1778FET180	EMC_D[15:0]	EMC_A[19:0]	EMC_BLS[1:0], EMC_CS[1:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC1778FBD144	EMC_D[7:0]	EMC_A[15:0]	EMC_CS[1:0], EMC_OE, EMC_WE	not available
LPC1777FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1776FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1776FET180	EMC_D[15:0]	EMC_A[19:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[1:0], EMC_CLK[1:0], EMC_CKE[1:0], EMC_DQM[1:0]
LPC1774FBD208	EMC_D[31:0]	EMC_A[25:0]	EMC_BLS[3:0], EMC_CS[3:0], EMC_OE, EMC_WE	EMC_RAS, EMC_CAS, EMC_DYCS[3:0], EMC_CLK[1:0], EMC_CKE[3:0], EMC_DQM[3:0]
LPC1774FBD144	EMC_D[7:0]	EMC_A[15:0]	EMC_CS[1:0], EMC_OE, EMC_WE	not available

The LPC178x/7x EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

See Table 6 for EMC memory access.

7.10.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.11 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral and can be accessed through the AHB master. The GPDMA controller allows data transfers between the various on-chip SRAM areas and supports the SD/MMC card interface, all SSPs, the I^2S, all UARTs, the A/D Converter, and the D/A Converter peripherals. DMA can also be triggered by selected timer match conditions. Memory-to-memory transfers and transfers to or from GPIO are supported.

- Physical interface:
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

7.15 USB interface

Remark: The USB Device/Host/OTG controller is available on parts LPC1788/87/86/85 and LPC1778/77/76. The USB Device-only controller is available on parts LPC1774.

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

Details on typical USB interfacing solutions can be found in Section 14.1.

7.15.1 USB device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the USB RAM.

7.15.1.1 Features

- Fully compliant with *USB 2.0 Specification* (full speed).
- Supports 32 physical (16 logical) endpoints with a 4 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- Supports SoftConnect and GoodLink features.
- While USB is in the Suspend mode, the LPC178x/7x can enter one of the reduced power modes and wake up on USB activity.
- Supports DMA transfers with all on-chip SRAM blocks on all non-control endpoints.
- Allows dynamic switching between CPU-controlled and DMA modes.
- Double buffer implementation for Bulk and Isochronous endpoints.

7.15.2 USB host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

7.15.2.1 Features

- OHCI compliant.

The first option assumes that power consumption is not a concern and the design ties the $V_{DD(3V3)}$ and $V_{DD(REG)(3V3)}$ pins together. This approach requires only one 3.3 V power supply for both pads, the CPU, and peripherals. While this solution is simple, it does not support powering down the I/O pad ring “on the fly” while keeping the CPU and peripherals alive.

The second option uses two power supplies; a 3.3 V supply for the I/O pads ($V_{DD(3V3)}$) and a dedicated 3.3 V supply for the CPU ($V_{DD(REG)(3V3)}$). Having the on-chip voltage regulator powered independently from the I/O pad ring enables shutting down of the I/O pad power supply “on the fly” while the CPU and peripherals stay active.

The VBAT pin supplies power only to the RTC domain. The RTC operates at very low power, which can be supplied by an external battery. The device core power ($V_{DD(REG)(3V3)}$) is used to operate the RTC whenever $V_{DD(REG)(3V3)}$ is present. There is no power drain from the RTC battery when $V_{DD(REG)(3V3)}$ is at nominal levels and $V_{DD(REG)(3V3)} > V_{BAT}$.

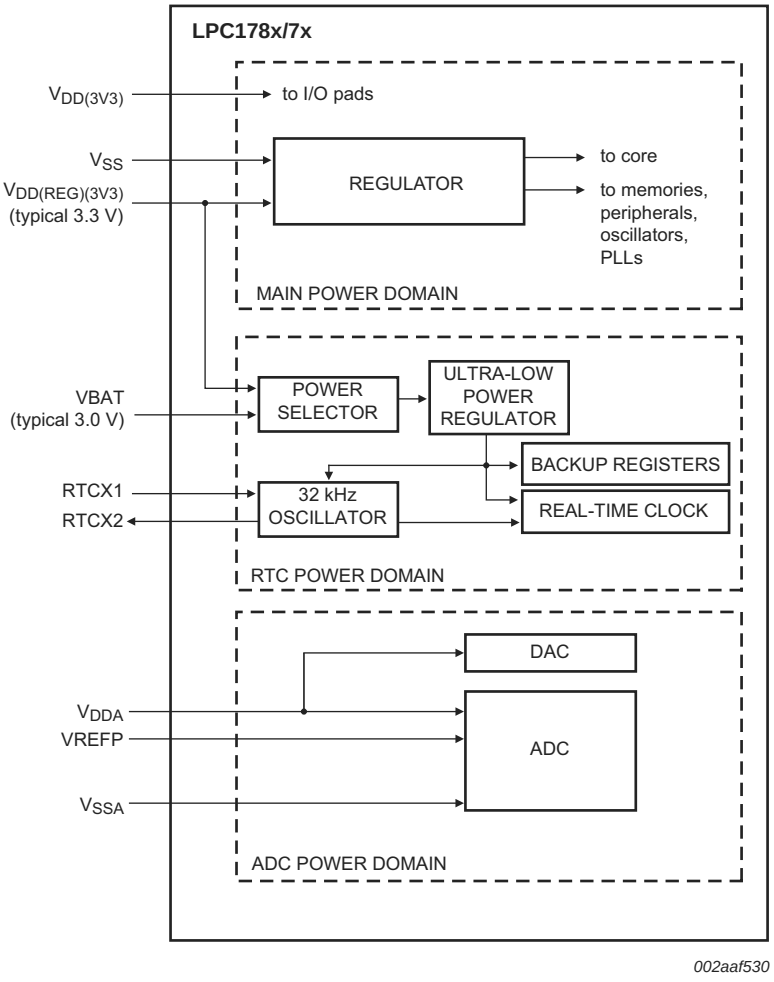


Fig 8. Power distribution

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.34.4 APB interface

The APB peripherals are split into two separate APB buses in order to distribute the bus bandwidth and thereby reducing stalls caused by contention between the CPU and the GPDMA controller.

7.34.5 AHB multilayer matrix

The LPC178x/7x use an AHB multilayer matrix. This matrix connects the instruction (I-code) and data (D-code) CPU buses of the ARM Cortex-M3 to the flash memory, the main (64 kB) SRAM, and the Boot ROM. The GPDMA can also access all of these memories. Additionally, the matrix connects the CPU system bus and all of the DMA controllers to the various peripheral functions.

7.34.6 External interrupt inputs

The LPC178x/7x include up to 30 edge sensitive interrupt inputs combined with one level sensitive external interrupt input as selectable pin function. The external interrupt input can optionally be used to wake up the processor from Power-down mode.

7.34.7 Memory mapping control

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M3 address space. The vector table must be located on a 128 word (512 byte) boundary because the NVIC on the LPC178x/7x is configured for 128 total interrupts.

7.35 Debug control

Debug and trace functions are integrated into the ARM Cortex-M3. Serial wire debug and trace functions are supported in addition to a standard JTAG debug and parallel trace functions. The ARM Cortex-M3 is configured to support up to eight breakpoints and four watch points.

Table 13. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[15][16][17]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[18]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[18]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	µA
		$V_{DD(3V3)} < V_I < 5$ V		0	0	0	µA
I^2C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05 \times V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[19]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[20]	-	-	±10	µA
V_{BUS}	bus supply voltage		[20]	-	-	5.25	V

10.2 Peripheral power consumption

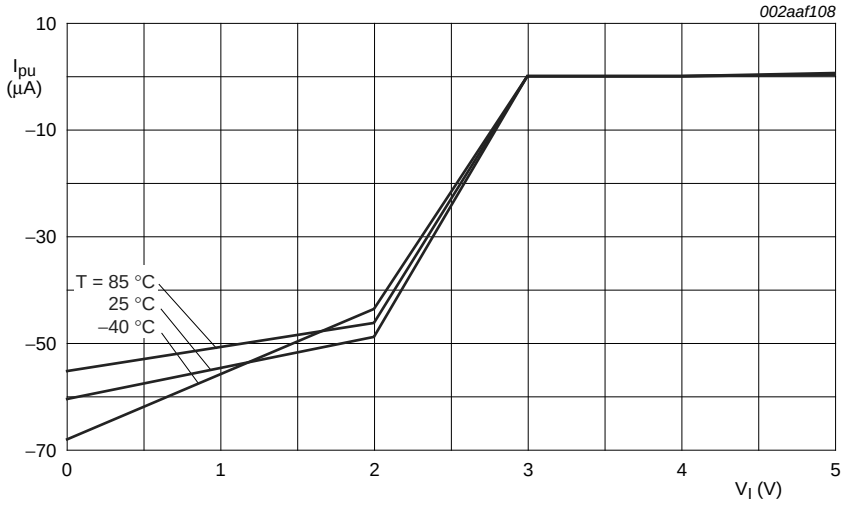
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the PCONP register. All other blocks are disabled and no code is executed. Measured on a typical sample at T_{amb} = 25 °C. The peripheral clock was set to PCLK = CCLK/4 with CCLK = 12 MHz, 48 MHz, and 120 MHz.

The combined current of several peripherals running at the same time can be less than the sum of each individual peripheral current measured separately.

Table 14. Power consumption for individual analog and digital blocks

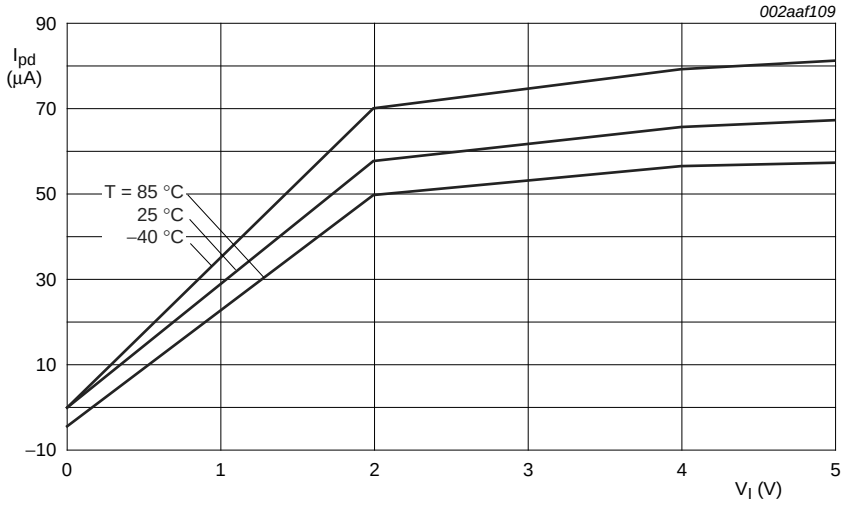
T_{amb} = 25 °C; $V_{DD(REG)(3V3)} = V_{DD(3V3)} = V_{DDA}$ = 3.3 V; PCLK = CCLK/4.

Peripheral	Conditions	Typical supply current in mA		
		12 MHz[1]	48 MHz[1]	120 MHz[2]
Timer0	-	0.01	0.06	0.15
Timer1	-	0.02	0.07	0.16
Timer2	-	0.02	0.07	0.17
Timer3	-	0.01	0.07	0.16
Timer0 + Timer1 + Timer2 + Timer3	-	0.07	0.28	0.67
UART0	-	0.05	0.19	0.45
UART1	-	0.06	0.24	0.56
UART2	-	0.05	0.2	0.47
UART3	-	0.06	0.23	0.56
USART4	-	0.07	0.27	0.66
UART0 + UART1 + UART2 + UART3 + USART4	-	0.29	1.13	2.74
PWM0 + PWM1	-	0.08	0.31	0.75
Motor control PWM	-	0.04	0.15	0.36
I2C0	-	0.01	0.03	0.08
I2C1	-	0.01	0.03	0.1
I2C2	-	0.01	0.03	0.08
I2C0 + I2C1 + I2C2	-	0.02	0.1	0.26
SSP0	-	0.03	0.1	0.26
SSP1	-	0.02	0.11	0.27
DAC	-	0.3	0.31	0.33
ADC (12 MHz clock)	-	1.51	1.61	1.7
CAN1	-	0.11	0.44	1.08
CAN2	-	0.1	0.4	0.98
CAN1 + CAN2	-	0.15	0.59	1.44
DMA	PCLK = CCLK	1.1	4.27	10.27
QEI	-	0.02	0.11	0.28
GPIO	-	0.4	1.72	4.16
LCD	-	0.99	3.84	9.25
I2S	-	0.04	0.18	0.46



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

Fig 14. Typical pull-up current I_{pu} versus input voltage V_I



Conditions: $V_{DD(REG)(3V3)} = V_{DD(3V3)} = 3.3$ V; standard port pins.

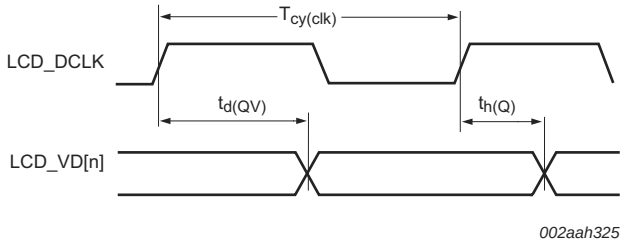
Fig 15. Typical pull-down current I_{pd} versus input voltage V_I

Table 20. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01

C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1 $t_{clk0dly}$ = 0 and $t_{clk1dly}$ = 0						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	12.5	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	t_{cmddly} + 4.1	t_{cmddly} + 6.0	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 1.0	t_{cmddly} + 1.6	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		-	t_{cmddly} + 4.1	t_{cmddly} + 6.0	ns
$t_{h(RAS)}$	row address strobe hold time		t_{cmddly} + 1.1	t_{cmddly} + 1.7	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	t_{cmddly} + 4.1	t_{cmddly} + 6.1	ns
$t_{h(CAS)}$	column address strobe hold time		t_{cmddly} + 1.2	t_{cmddly} + 1.8	-	ns
$t_{d(WV)}$	write valid delay time		-	t_{cmddly} + 4.8	t_{cmddly} + 7.1	ns
$t_{h(W)}$	write hold time		t_{cmddly} + 1.6	t_{cmddly} + 2.3	-	ns
$t_{d(AV)}$	address valid delay time		-	t_{cmddly} + 4.9	t_{cmddly} + 7.3	ns
$t_{h(A)}$	address hold time		t_{cmddly} + 1.0	t_{cmddly} + 1.6	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		7.1 - t_{fbdly}	4.8 - t_{fbdly}	-	ns
$t_{h(D)}$	data input hold time		-1.9 + t_{fbdly}	-2.5 + t_{fbdly}	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	t_{cmddly} + 4.9	t_{cmddly} + 7.3	ns
$t_{h(Q)}$	data output hold time		t_{cmddly} + 0.2	t_{cmddly} + 0.5	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.



The LCD panel clock is shown with the default polarity. The clock can be inverted via the IPC bit in the LCD_POL register. Typically, the LCD panel uses the falling edge of the LCD_DCLK to sample the data.

Fig 26. LCD timing

11.10 SD/MMC

Remark: The SD/MMC card interface is available on parts LPC1788/87/86 and parts LPC1778/77/76.

Table 30. Dynamic characteristics: SD/MMC

C_L = 10 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	25	MHz
		on pin SD_CLK; identification mode		25	MHz
$t_{su(D)}$	data input set-up time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{h(D)}$	data input hold time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{d(QV)}$	data output valid delay time	on pins SD_CMD, SD_DAT[3:0] as outputs	-	23	ns
$t_{h(Q)}$	data output hold time	on pins SD_CMD, SD_DAT[3:0] as outputs	3.5	-	ns

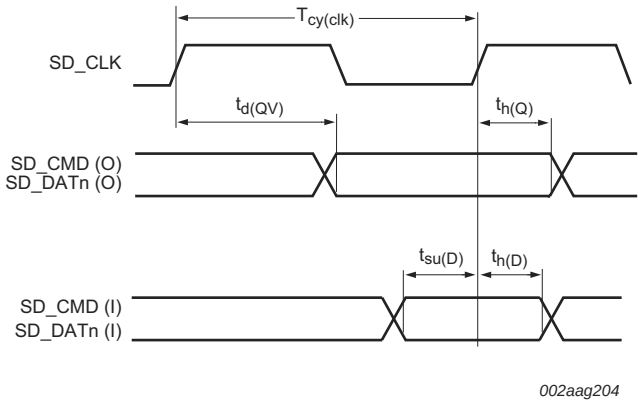


Fig 27. SD/MMC timing

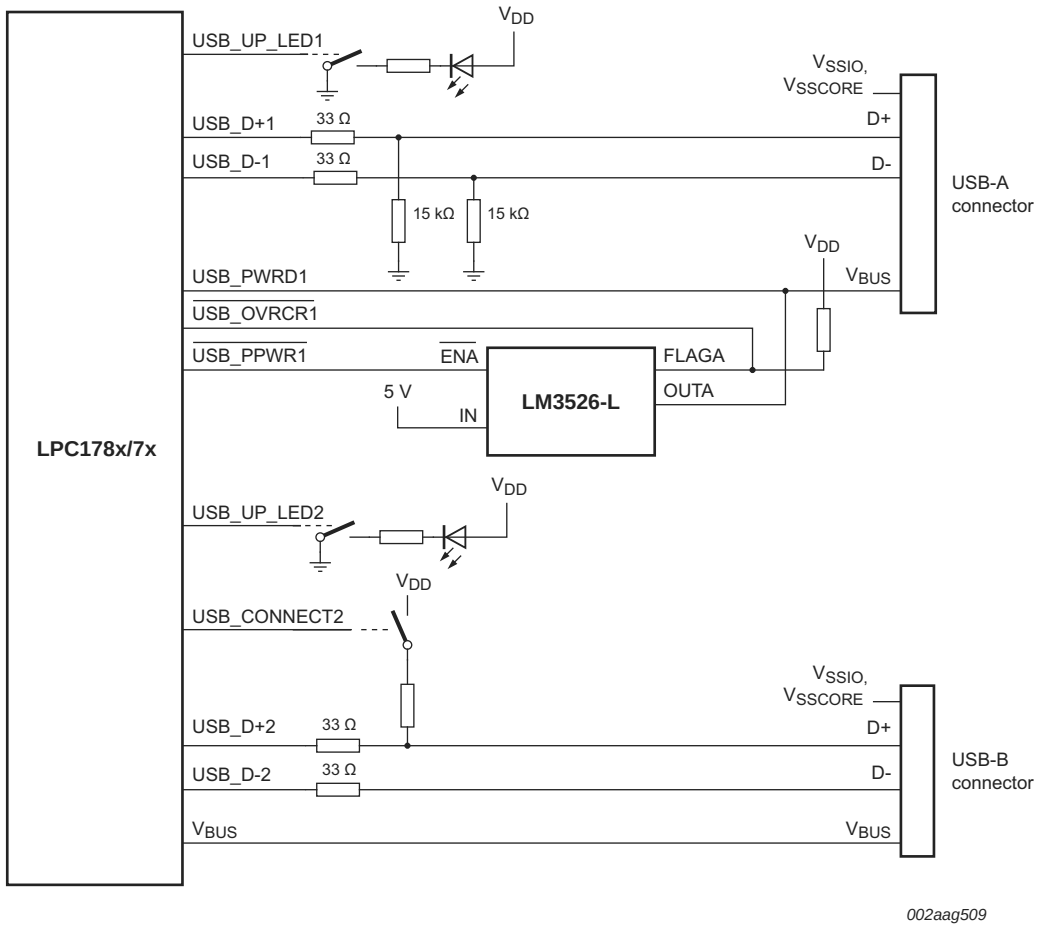


Fig 35. USB device port configuration: port 1 host and port 2 device

14.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

Table 34. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 35. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

14.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plane. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Smaller values of C_{x1} and C_{x2} should be chosen according to the increase in parasitics of the PCB layout.

14.4 Standard I/O pin configuration

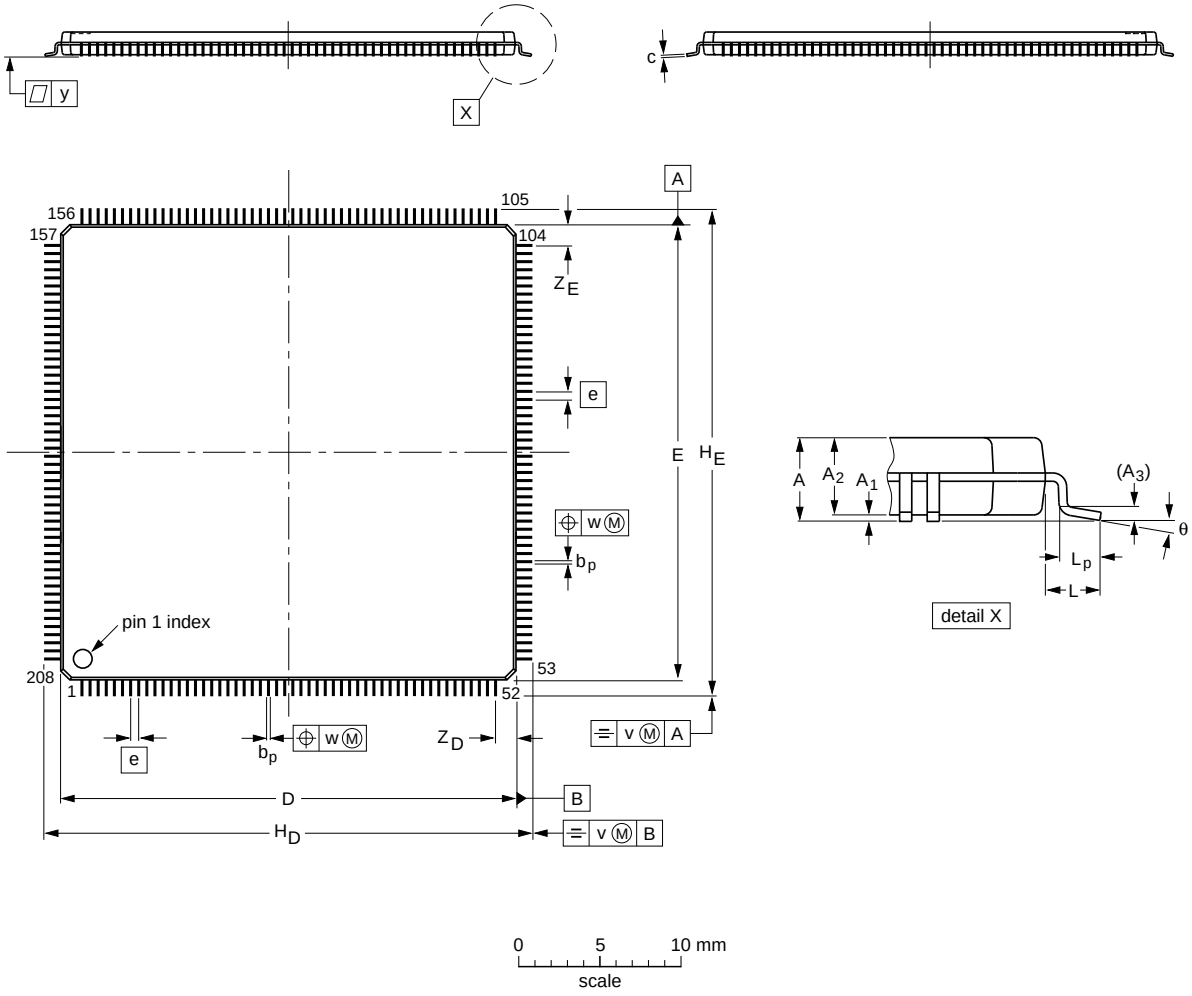
Figure 38 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver: Open-drain mode enabled/disabled.
- Digital input: Pull-up enabled/disabled.
- Digital input: Pull-down enabled/disabled.
- Digital input: Repeater mode enabled/disabled.
- Analog input.

The default configuration for standard I/O pins is input with pull-up enabled. The weak MOS devices provide a drive capability equivalent to pull-up and pull-down resistors.

15. Package outline

LQFP208; plastic low profile quad flat package; 208 leads; body 28 x 28 x 1.4 mm **SOT459-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	Z_D	Z_E	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	28.1 27.9	28.1 27.9	0.5	30.15 29.85	30.15 29.85	1	0.75 0.45	0.12	0.08	0.08	1.43 1.08	1.43 1.08	7^o 0^o

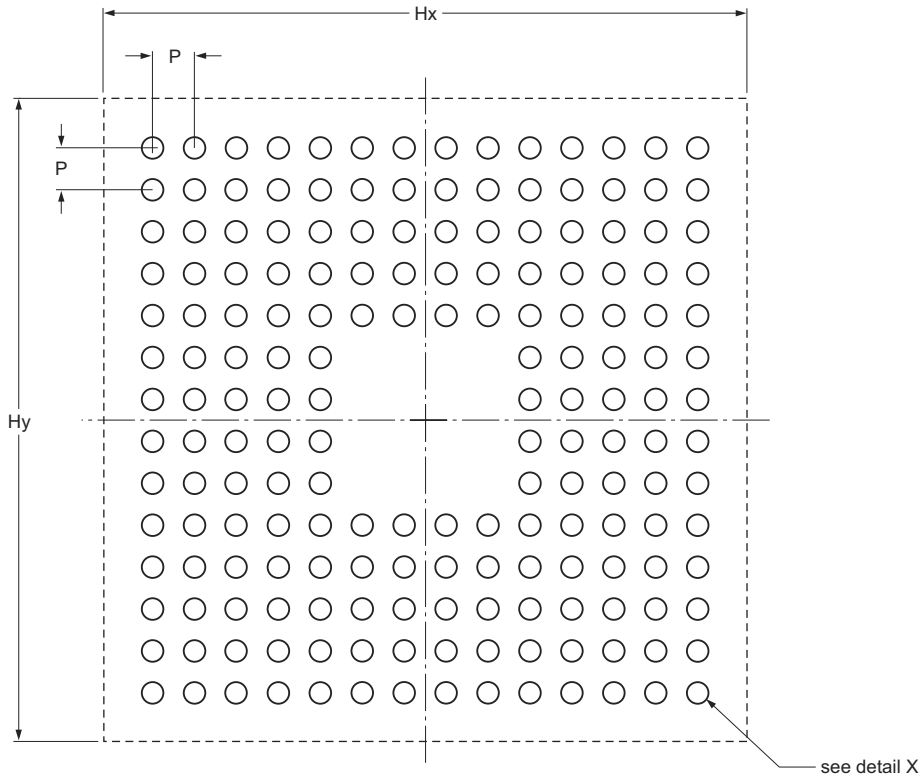
Note

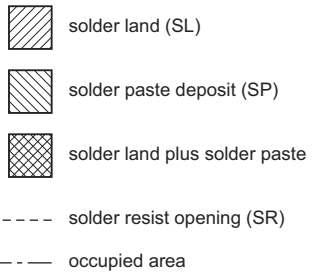
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

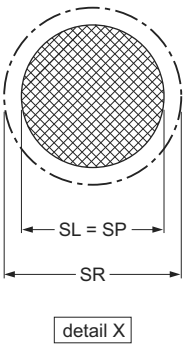
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT459-1	136E30	MS-026				~~00-02-06~~ 03-02-20

Fig 41. LQFP208 package

Footprint information for reflow soldering of TFBGA180 package **SOT570-3**







detail X

Dimensions in mm

P	SL	SP	SR	Hx	Hy
0.80	0.40	0.40	0.50	12.30	12.30

Issue date ~~14-01-30~~ 15-08-27

Recommend stencil thickness: 0.1 mm

sot570-3_fr

Fig 46. Reflow soldering of the TFBGA180 package

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 26 April 2016
Document identifier: LPC178X_7X