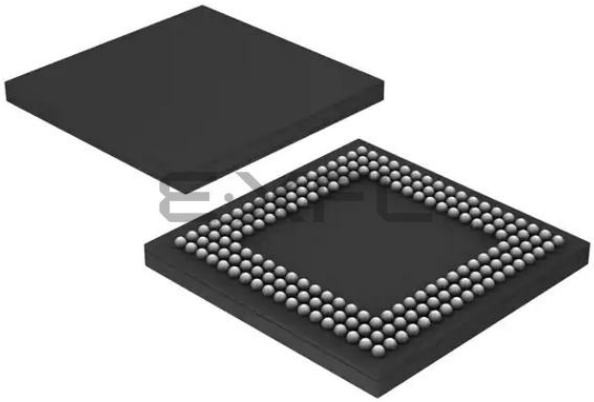

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, Motor Control PWM, POR, PWM, WDT
Number of I/O	141
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1788fet180-551

- The Wake-up Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.
- Processor wake-up from Power-down mode via any interrupt able to operate during Power-down mode (includes external interrupts, RTC interrupt, PORT0/2 pin interrupt, and NMI).
- Brownout detect with separate threshold for interrupt and forced reset.
- On-chip Power-On Reset (POR).

- Clock generation:
  - Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, USB clock, or the watchdog timer clock.
  - On-chip crystal oscillator with an operating range of 1 MHz to 25 MHz.
  - 12 MHz Internal RC oscillator (IRC) trimmed to 1% accuracy that can optionally be used as a system clock.
  - An on-chip PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator or the internal RC oscillator.
  - A second, dedicated PLL may be used for USB interface in order to allow added flexibility for the Main PLL settings.
- Versatile pin function selection feature allows many possibilities for using on-chip peripheral functions.
- Unique device serial number for identification purposes.
- Single 3.3 V power supply (2.4 V to 3.6 V). Temperature range of −40 °C to 85 °C.
- Available as LQFP208, TFBGA208, TFBGA180, and LQFP144 package.

3. Applications

- Communications:
  - Point-of-sale terminals, web servers, multi-protocol bridges
- Industrial/Medical:
  - Automation controllers, application control, robotics control, HVAC, PLC, inverters, circuit breakers, medical scanning, security monitoring, motor drive, video intercom
- Consumer/Appliance:
  - Audio, MP3 decoders, alarm systems, displays, printers, scanners, small appliances, fitness equipment
- Automotive:
  - After-market, car alarms, GPS/fleet monitors

Table 3. Pin description

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[0] to P0[31]							I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the pin connect block.
P0[0]	94	U15	M10	66	[3]	I; PU	I/O	**P0[0] —** General purpose digital input/output pin.
							I	**CAN_RD1 —** CAN1 receiver input.
							O	**U3_TXD —** Transmitter output for UART3.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).
							O	**U0_TXD —** Transmitter output for UART0.
P0[1]	96	T14	N11	67	[3]	I; PU	I/O	**P0[1] —** General purpose digital input/output pin.
							O	**CAN_TD1 —** CAN1 transmitter output.
							I	**U3_RXD —** Receiver input for UART3.
							I/O	**I2C1_SCL —** I^2C1 clock input/output (this pin does not use a specialized I2C pad).
							I	**U0_RXD —** Receiver input for UART0.
P0[2]	202	C4	D5	141	[3]	I; PU	I/O	**P0[2] —** General purpose digital input/output pin.
							O	**U0_TXD —** Transmitter output for UART0.
							O	**U3_TXD —** Transmitter output for UART3.
P0[3]	204	D6	A3	142	[3]	I; PU	I/O	**P0[3] —** General purpose digital input/output pin.
							I	**U0_RXD —** Receiver input for UART0.
							I	**U3_RXD —** Receiver input for UART3.
P0[4]	168	B12	A11	116	[3]	I; PU	I/O	**P0[4] —** General purpose digital input/output pin.
							I/O	**I2S_RX_SCK —** I^2S Receive clock. It is driven by the master and received by the slave. Corresponds to the signal SCK in the *I^2S-bus specification*.
							I	**CAN_RD2 —** CAN2 receiver input.
							I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[0] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[8]	160	A15	C12	111	[4]	I; IA	I/O	**P0[8] —** General purpose digital input/output pin.
							I/O	**I2S_TX_WS —** I^2S Transmit word select. It is driven by the master and received by the slave. Corresponds to the signal WS in the *I^2S-bus specification*.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
							I	**RTC_EV1 —** Event input 1 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[16] —** LCD data.
P0[9]	158	C14	A13	109	[4]	I; IA	I/O	**P0[9] —** General purpose digital input/output pin.
							I/O	**I2S_TX_SDA —** I^2S transmit data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
							I	**RTC_EV2 —** Event input 2 to Event Monitor/Recorder.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[17] —** LCD data.
P0[10]	98	T15	L10	69	[3]	I; PU	I/O	**P0[10] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for UART2.
							I/O	**I2C2_SDA —** I^2C2 data input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT0 —** Match output for Timer 3, channel 0.
P0[11]	100	R14	P12	70	[3]	I; PU	I/O	**P0[11] —** General purpose digital input/output pin.
							I	**U2_RXD —** Receiver input for UART2.
							I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
							O	**T3_MAT1 —** Match output for Timer 3, channel 1.
P0[12]	41	R1	J4	29	[5]	I; PU	I/O	**P0[12] —** General purpose digital input/output pin.
							O	**$\overline{\text{USB\_PPWR2}}$ —** Port Power enable signal for USB port 2.
							I/O	**SSP1_MISO —** Master In Slave Out for SSP1.
							I	**ADC0_IN[6] —** A/D converter 0, input 6. When configured as an ADC input, the digital function of the pin must be disabled.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P2[5]	140	F16	F12	97	[3]	I; PU	I/O	**P2[5] —** General purpose digital input/output pin.
							O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							O	**T2_MAT0 —** Match output for Timer 2, channel 0.
							-	**R —** Function reserved.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
P2[6]	138	E17	F13	96	[3]	I; PU	I/O	**P2[6] —** General purpose digital input/output pin.
							I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
							I	**U1_RI —** Ring Indicator input for UART1.
							I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
							O	**U2_OE —** RS-485/EIA-485 output enable signal for UART2.
							O	**TRACECLK —** Trace clock.
							O	**LCD_VD[0] —** LCD data.
							O	**LCD_VD[4] —** LCD data.
P2[7]	136	G16	G11	95	[3]	I; PU	I/O	**P2[7] —** General purpose digital input/output pin.
							I	**CAN_RD2 —** CAN2 receiver input.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[1] —** LCD data.
							O	**LCD_VD[5] —** LCD data.
P2[8]	134	H15	G14	93	[3]	I; PU	I/O	**P2[8] —** General purpose digital input/output pin.
							O	**CAN_TD2 —** CAN2 transmitter output.
							O	**U2_TXD —** Transmitter output for UART2.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**ENET_MDC —** Ethernet MIIM clock.
							-	**R —** Function reserved.
							O	**LCD_VD[2] —** LCD data.
							O	**LCD_VD[6] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P4[29]	176	B10	B9	122	[3]	I; PU	I/O	**P4[29] —** General purpose digital input/output pin.
							O	**EMC_BLS3 —** LOW active Byte Lane select signal 3.
							I	**U3_RXD —** Receiver input for UART3.
							O	**T2_MAT1 —** Match output for Timer 2, channel 1.
							I/O	**I2C2_SCL —** I^2C2 clock input/output (this pin does not use a specialized I2C pad).
							O	**LCD_VD[7] —** LCD data.
							O	**LCD_VD[11] —** LCD data.
							O	**LCD_VD[3] —** LCD data.
P4[30]	187	B7	C7	130	[3]	I; PU	I/O	**P4[30] —** General purpose digital input/output pin.
							O	**EMC_CS0 —** LOW active Chip Select 0 signal.
P4[31]	193	A4	E7	134	[3]	I; PU	I/O	**P4[31] —** General purpose digital input/output pin.
							O	**EMC_CS1 —** LOW active Chip Select 1 signal.
P5[0] to P5[4]							I/O	**Port 5:** Port 5 is a 5-bit I/O port with individual direction controls for each bit. The operation of port 5 pins depends upon the pin function selected via the pin connect block.
P5[0]	9	F4	E5	6	[3]	I; PU	I/O	**P5[0] —** General purpose digital input/output pin.
							I/O	**EMC_A[24] —** External memory address line 24.
							I/O	**SSP2_MOSI —** Master Out Slave In for SSP2.
							O	**T2_MAT2 —** Match output for Timer 2, channel 2.
P5[1]	30	J4	H1	21	[3]	I; PU	I/O	**P5[1] —** General purpose digital input/output pin.
							I/O	**EMC_A[25] —** External memory address line 25.
							I/O	**SSP2_MISO —** Master In Slave Out for SSP2.
							O	**T2_MAT3 —** Match output for Timer 2, channel 3.
P5[2]	117	L14	L12	81	[11]	I	I/O	**P5[2] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**T3_MAT2 —** Match output for Timer 3, channel 2.
							-	**R —** Function reserved.
							I/O	**I2C0_SDA —** I^2C0 data input/output (this pin uses a specialized I^2C pad that supports I^2C Fast Mode Plus).

Table 4. Pin allocation table TFBGA208

Not all functions are available on all parts. See Table 2 and Table 7 (EMC pins).

Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol
13		14	P0[16]	15	P4[23]	16	P0[15]
17	P4[8]		-		-		-
Row K							
1	VREFP	2	RTCX1	3	RSTOUT	4	VSSREG
13	-	14	P4[22]	15	P0[18]	16	$V_{DD(3V3)}$
17	P0[17]		-		-		-
Row L							
1	P3[7]	2	RTCX2	3	V_{SS}	4	P2[30]
5	-	6	-	7	-	8	-
9	-	10	-	11	-	12	-
13	-	14	P5[2]	15	P4[26]	16	P4[7]
17	P0[19]		-		-		-
Row M							
1	P3[15]	2	$\overline{\text{RESET}}$	3	VBAT	4	XTAL1
5	-	6	-	7	-	8	-
9	-	10	-	11	-	12	-
13	-	14	P4[6]	15	P4[21]	16	P0[21]
17	P0[20]		-		-		-
Row N							
1	RTC_ALARM	2	P2[31]	3	P2[29]	4	XTAL2
5	-	6	-	7	-	8	-
9	-	10	-	11	-	12	-
13	-	14	P2[12	15	P2[10]	16	V_{SS}
17	P0[22]		-		-		-
Row P							
1	P1[31]	2	P1[30]	3	P2[27]	4	P2[28]
5	P2[24]	6	$V_{DD(3V3)}$	7	P1[18]	8	$V_{DD(3V3)}$
9	P1[23]	10	VSSREG	11	$V_{DD(REG)(3V3)}$	12	V_{SS}
13	P2[15]	14	P4[17]	15	P4[18]	16	P4[19]
17	$V_{DD(3V3)}$		-		-		-
Row R							
1	P0[12]	2	P0[13]	3	P0[28]	4	P2[25]
5	P3[24]	6	P0[30]	7	P2[19]	8	P1[21]
9	V_{SS}	10	P1[26]	11	P2[16]	12	P2[14]
13	P2[17]	14	P0[11]	15	P4[4]	16	P4[5]
17	P4[20]		-		-		-
Row T							
1	P0[27]	2	P0[31]	3	P3[26]	4	P2[26]
5	V_{SS}	6	P3[23]	7	P0[14]	8	P2[20]
9	P1[24]	10	P1[25]	11	P4[2]	12	P1[27]

Table 4. Pin allocation table TFBGA208

Not all functions are available on all parts. See Table 2 and Table 7 (EMC pins).

Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol
13	P1[28]	14	P0[1]	15	P0[10]	16	P2[13]
17	P2[11]		-		-		-
Row U							
1	USB_D-2	2	P3[25]	3	P2[18]	4	P0[29]
5	P2[23]	6	P1[19]	7	P1[20]	8	P1[22]
9	P4[0]	10	P4[1]	11	P2[21]	12	P2[22]
13	$V_{DD(3V3)}$	14	P1[29]	15	P0[0]	16	P4[3]
17	P4[16]		-		-		-

Table 5. Pin allocation table TFBGA180

Not all functions are available on all parts. See Table 2 and Table 7 (EMC pins).

Ball	Symbol	Ball	Symbol	Ball	Symbol	Ball	Symbol
Row A							
5	P1[1]	6	P3[8]	7	P1[10]	8	P1[15]
9	P1[3]	10	V_{SSREG}	11	P0[4]	12	P1[11]
13	P0[9]	14	P1[12]		-		-
Row B							
1	JTAG_TDO (SWO)	2	P3[11]	3	P3[10]	4	V_{SS}
5	P1[0]	6	P1[8]	7	P1[2]	8	P1[16]
9	P4[29]	10	P1[6]	11	P0[5]	12	P0[7]
13	P1[5]	14	P4[13]		-		-
Row C							
1	P3[13]	2	JTAG_TMS (SWDIO)	3	JTAG_TDI	4	P5[4]
5	$V_{DD(3V3)}$	6	P1[4]	7	P4[30]	8	P4[24]
9	P1[17]	10	P4[15]	11	V_{SS}	12	P0[8]
13	P1[7]	14	P2[1]		-		-
Row D							
1	P0[26]	2	JTAG_TCK (SWDCLK)	3	P3[4]	4	$\overline{\text{JTAG\_TRST}}$
5	P0[2]	6	P3[0]	7	P1[9]	8	P1[14]
9	P4[25]	10	P4[28]	11	P0[6]	12	P2[0]
13	V_{SS}	14	P1[13]		-		-
Row E							
1	P0[24]	2	$V_{DD(3V3)}$	3	P3[5]	4	P0[25]
5	P5[0]	6	P3[1]	7	P4[31]	8	P4[14]
9	$V_{DD(REG)(3V3)}$	10	$V_{DD(3V3)}$	11	P2[2]	12	$V_{DD(3V3)}$
13	P2[3]	14	P2[4]		-		-
Row F							
1	P3[14]	2	V_{DDA}	3	V_{SSA}	4	P3[6]
5	P0[23]	6	-	7	-	8	-
9	-	10	P4[12]	11	P4[11]	12	P2[5]

7.14 Ethernet

Remark: The Ethernet block is available on parts LPC1788/86 and LPC1778/76.

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU.

The Ethernet block and the CPU share the ARM Cortex-M3 D-code and system bus through the AHB-multilayer matrix to access the various on-chip SRAM blocks for Ethernet data, control, and status information.

The Ethernet block interfaces between an off-chip Ethernet PHY using the Media Independent Interface (MII) or Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.14.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame suppor
  - .
- Memory management:
  - Independent transmit and receive buffers memory mapped to shared SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching.
  - Wake-on-LAN power management support allows system wake-up: using the receive filters or a magic frame detection filter.

Two match registers can be used to provide a single edge controlled PWM output. One match register (PWMMR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an PWMMR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the PWMMR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

7.26.1 Features

- LPC178x/7x has two PWM blocks with Counter or Timer operation (may use the peripheral clock or one of the capture inputs as the clock source).
- Seven match registers allow up to 6 single edge controlled or 3 double edge controlled PWM outputs, or a mix of both types. The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go high at the beginning of each cycle unless the output is a constant low. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.
- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard 32-bit timer/counter with a programmable 32-bit prescaler if the PWM mode is not enabled.

7.27 Motor control PWM

The LPC178x/7x contain one motor control PWM.

The motor control PWM is a specialized PWM supporting 3-phase motors and other combinations. Feedback inputs are provided to automatically sense rotor position and use that information to ramp speed up or down. An abort input is also provided that causes the

In Sleep mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

The DMA controller can continue to work in Sleep mode and has access to the peripheral RAMs and all peripheral registers. The flash memory and the main SRAM are not available in Sleep mode, they are disabled in order to save power.

Wake-up from Sleep mode will occur whenever any enabled interrupt occurs.

7.33.4.2 Deep-sleep mode

In Deep-sleep mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep-sleep mode and the logic levels of chip pins remain static. The output of the IRC is disabled but the IRC is not powered down to allow fast wake-up. The RTC oscillator is not stopped because the RTC interrupts may be used as the wake-up source. The PLL is automatically turned off and disconnected. The clock divider registers are automatically reset to zero.

The Deep-sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Deep-sleep mode reduces chip power consumption to a very low value. Power to the flash memory is left on in Deep-sleep mode, allowing a very quick wake-up.

Wake-up from Deep-sleep mode can initiated by the NMI, External Interrupts $\overline{\text{EINT0}}$ through $\overline{\text{EINT3}}$, GPIO interrupts, the Ethernet Wake-on-LAN interrupt, Brownout Detect, an RTC Alarm interrupt, a USB input pin transition (USB activity interrupt), a CAN input pin transition, or a Watchdog Timer time-out, when the related interrupt is enabled. Wake-up will occur whenever any enabled interrupt occurs.

On wake-up from Deep-sleep mode, the code execution and peripherals activities will resume after four cycles expire if the IRC was used before entering Deep-sleep mode. If the main external oscillator was used, the code execution will resume when 4096 cycles expire. PLL and clock dividers need to be reconfigured accordingly.

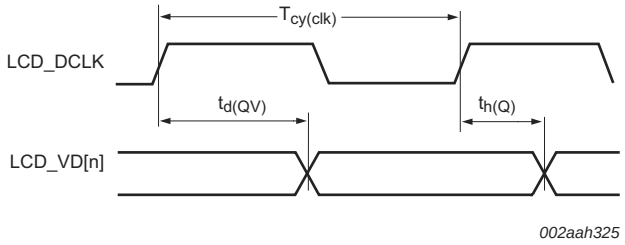
7.33.4.3 Power-down mode

Power-down mode does everything that Deep-sleep mode does but also turns off the power to the IRC oscillator and the flash memory. This saves more power but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished.

When the chip enters Power-down mode, the IRC, the main oscillator, and all clocks are stopped. The RTC remains running if it has been enabled and RTC interrupts may be used to wake up the CPU. The flash is forced into Power-down mode. The PLLs are automatically turned off and the clock selection multiplexers are set to use the system clock sysclk (the reset state). The clock divider control registers are automatically reset to zero. If the Watchdog timer is running, it will continue running in Power-down mode.

Table 13. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Standard port pins, $\overline{\text{RESET}}$							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[15][16][17]	0	-	5.0	V
V_O	output voltage	output active		0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA		$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V		−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[18]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[18]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	µA
		$V_{DD(3V3)} < V_I < 5$ V		0	0	0	µA
I^2C-bus pins (P0[27] and P0[28])							
V_{IH}	HIGH-level input voltage			$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage			-	$0.05 \times V_{DD(3V3)}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA		-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$	[19]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
USB pins							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[20]	-	-	±10	µA
V_{BUS}	bus supply voltage		[20]	-	-	5.25	V



The LCD panel clock is shown with the default polarity. The clock can be inverted via the IPC bit in the LCD_POL register. Typically, the LCD panel uses the falling edge of the LCD_DCLK to sample the data.

Fig 26. LCD timing

11.10 SD/MMC

Remark: The SD/MMC card interface is available on parts LPC1788/87/86 and parts LPC1778/77/76.

Table 30. Dynamic characteristics: SD/MMC

C_L = 10 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter	Conditions	Min	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	25	MHz
		on pin SD_CLK; identification mode		25	MHz
$t_{su(D)}$	data input set-up time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{h(D)}$	data input hold time	on pins SD_CMD, SD_DAT[3:0] as inputs	6	-	ns
$t_{d(QV)}$	data output valid delay time	on pins SD_CMD, SD_DAT[3:0] as outputs	-	23	ns
$t_{h(Q)}$	data output hold time	on pins SD_CMD, SD_DAT[3:0] as outputs	3.5	-	ns

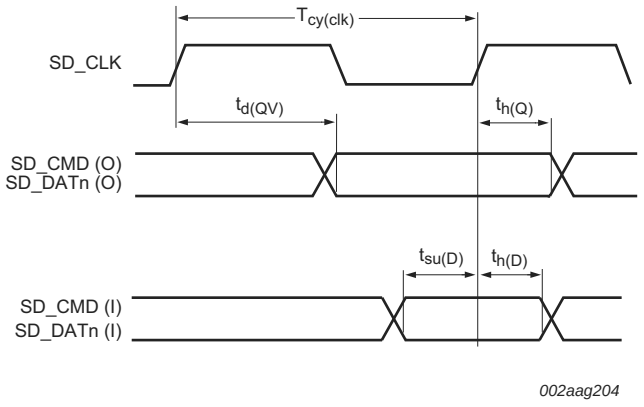


Fig 27. SD/MMC timing

14. Application information

14.1 Suggested USB interface solutions

Remark: The USB controller is available as a device/Host/OTG controller on parts LPC1788/87/86/85 and LPC1778/77/76 and as device-only controller on parts LPC1774.

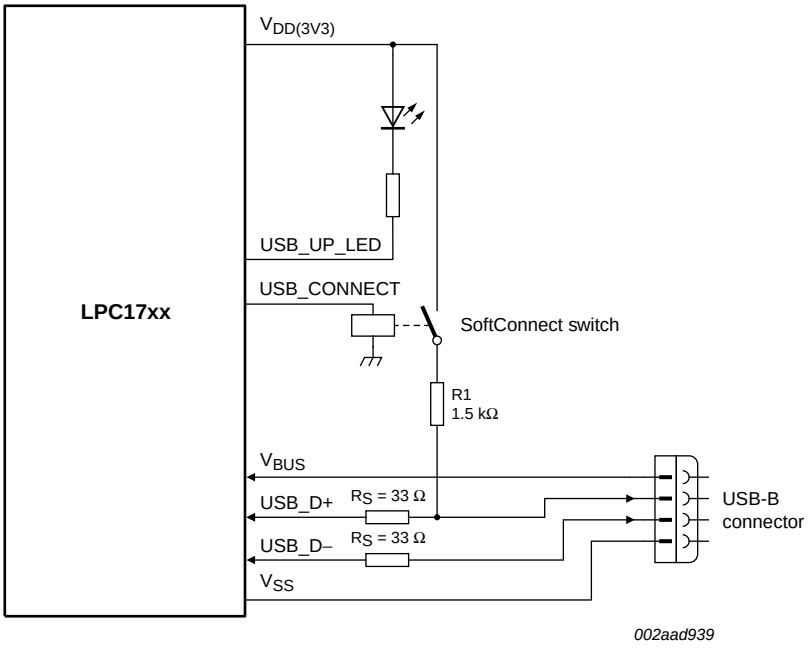


Fig 30. USB interface on a self-powered device

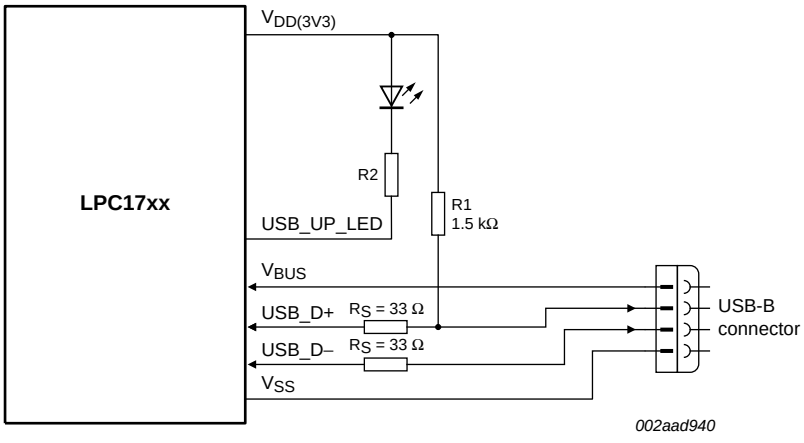


Fig 31. USB interface on a bus-powered device

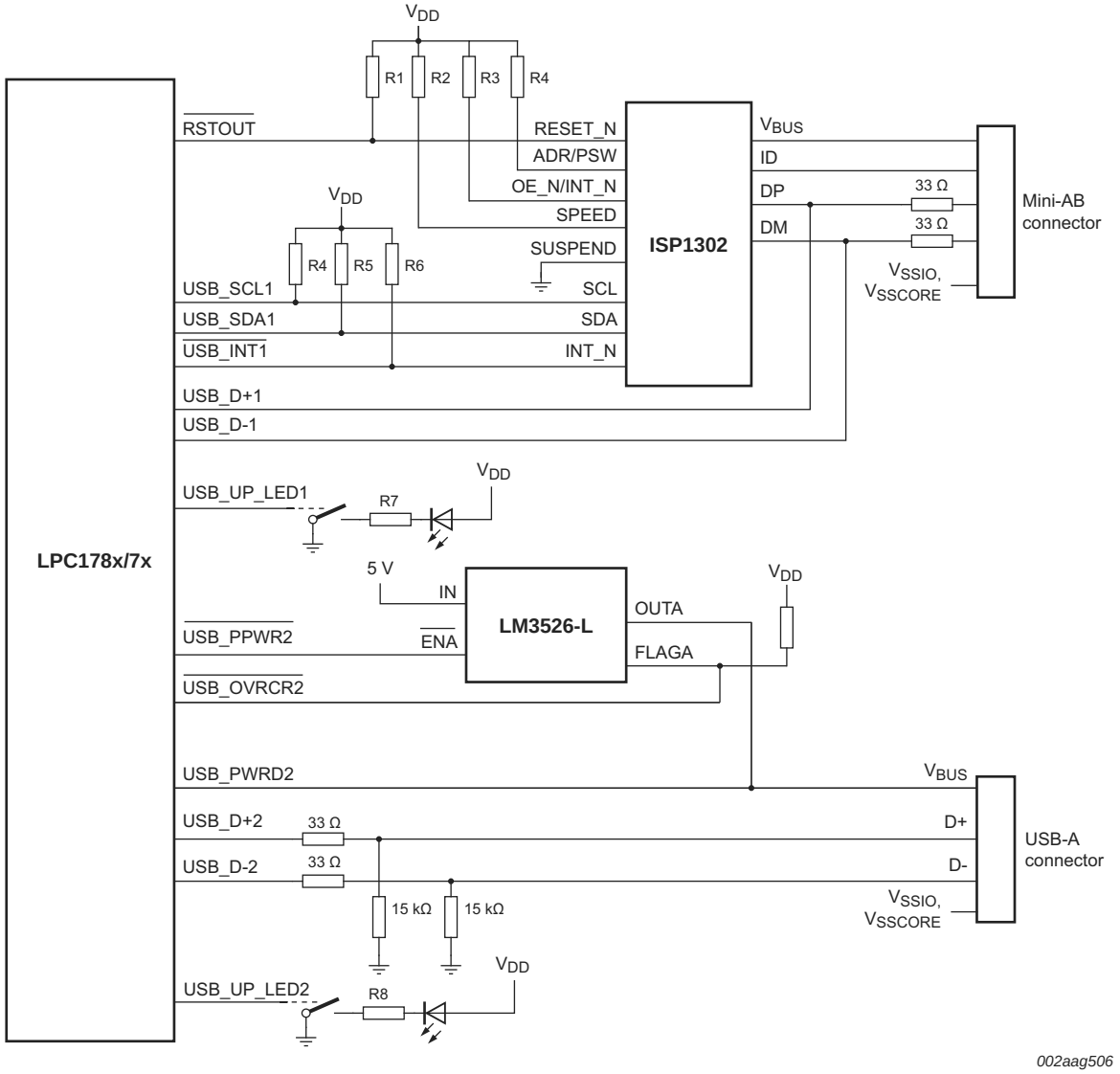


Fig 32. USB OTG port configuration: port 1 OTG dual-role device, port 2 host

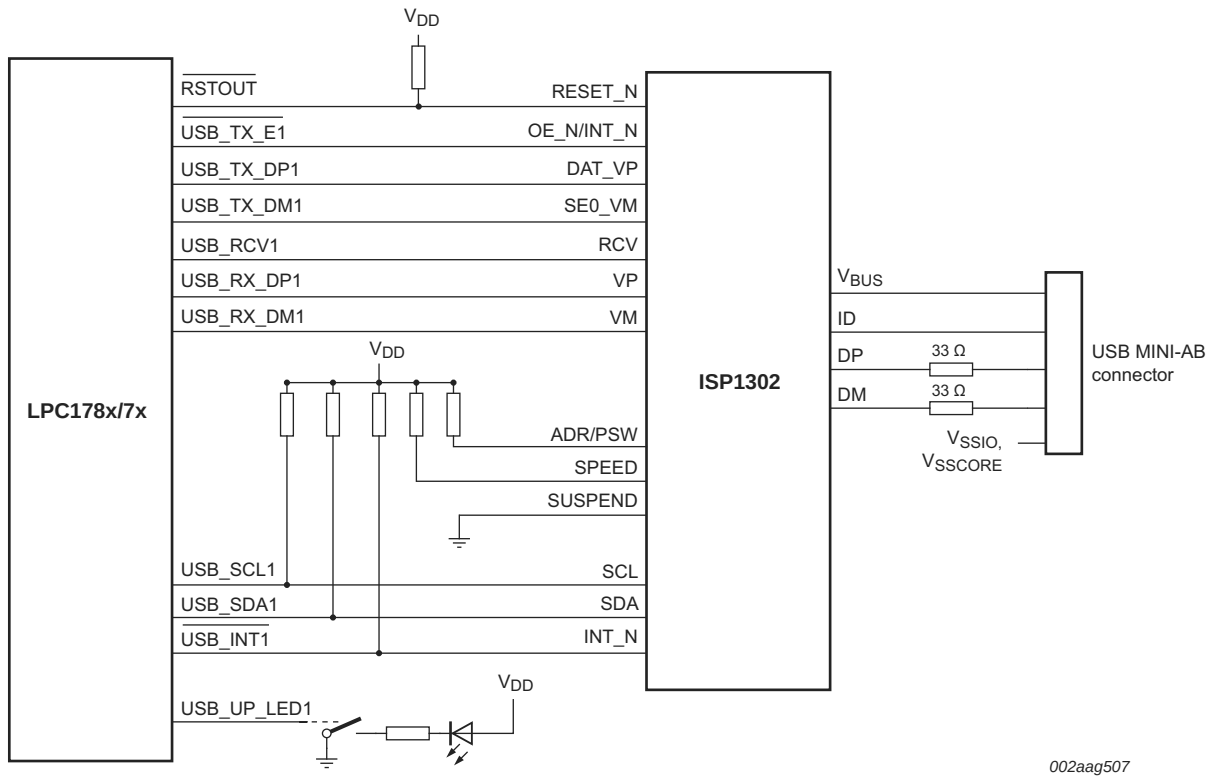


Fig 33. USB OTG port configuration: VP_VM mode

17. Abbreviations

Table 36. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
EOP	End Of Packet
ETM	Embedded Trace Macrocell
GPIO	General Purpose Input/Output
GPS	Global Positioning System
HVAC	Heating, Venting, and Air Conditioning
IRC	Internal RC
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
MAC	Media Access Control
MIIM	Media Independent Interface Management
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLC	Programmable Logic Controller
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TCM	Tightly Coupled Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC178X_7X v.4.1	20121115	Product data sheet	-	LPC178X_7X v.4
Modifications:	• LCD timing characteristics updated in Table 27 “Dynamic characteristics: LCD” and Figure 26 added. • Removed table note “The peak current is limited to 25 times the corresponding maximum current.” in Table 9. • Removed deep power-down spec Table 13 and associated table note. • Updated min value for t_{WEHEOW} Table 15. • Removed Fig 21 Internal RC oscillator frequency versus temperature. • Updated 12-bit and 8-bit values for E_T Table 29. • Changed data sheet status to Product.			
LPC178X_7X v.4	20120501	Preliminary data sheet	-	LPC178X_7X v.3
Modifications:	• Editorial updates. • BOD values added in Section 7.34.2. • Parameters $t_{CSLBLSL}$, t_{CSHOEH}, t_{OEHANV}, t_{deact}, $t_{BLSHEOW}$, $t_{BLSHDNV}$ updated in Table 17. • C_L = 10 pF added to Table 24, Table 26, Table 28. • $I_{DD(REG)(3V3)}$ corrected in Table 13 for conditions Deep-sleep mode, Power-down mode, and Deep-power down mode. • I_{BAT} corrected in Table 13 for condition Deep power-down mode. • Power consumption data in Figure 9 and Figure 10 corrected. • I/O voltage $V_{DD(3V3)}$ specified in Table 17, Table 18, Table 19, Table 24, Table 28. • $V_{DD(3V3)}$ range corrected in Table 23. • Parameter C_L changed to 10 pF for EMC timing in Table 17 to Table 20. • USB and Ethernet dynamic characteristics removed. Timing characteristics follow *USB 2.0 Specification* (full speed) and IEEE standard 802.3 standards (see Section 7.15 and Section 7.14 for compliance statements). • Pad characteristics updated in Table 3. • Parameter I_{BAT} updated in Table 13. • Figure 11 added. • SDRAM timing corrected in Figure 19. • EEPROM erase and programming times added (Table 16). • Data sheet status changed to preliminary.			

Table 37. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC178X_7X v.3	20111220	Objective data sheet	-	LPC178X_7X v.2
Modifications:	• Removed BOOT function from pin P3[14]. • I_{BAT} and $I_{DD(REG)(3V3)}$ updated for Deep power-down mode in Table 13. • Maximum SDRAM clock of 80 MHz specified in Section 2, Table 18, and Table 19. • Power consumption data added (Figure 9 and Figure 10). • Removed parameter Z_{DRV} in Table 13. • Specified maximum value for parameter C_L in Table 33 and remove typical value. • Specified setting of boost bits in Table 14, Table note 5 and in Table 13, Table note 6 . • USB connection diagrams updated (Figure 33 to Figure 36). • Current drain condition on battery supply specified in Section 7.33.6. • Table note 10 in Table 13 updated. • ADC characteristics updated (Table 31). • Section 14.6 “Reset pin configuration for RTC operation” added. • EEPROM size for parts LPC1774 corrected in Table 2 and Figure 1. • Changed function LCD_VD[5] on pin P0[10] to Reserved. • Changed function LCD_VD[10] on pin P0[11] to Reserved. • Changed function LCD_VD[13] on pin P0[19] to Reserved. • Changed function LCD_VD[14] on pin P0[20] to Reserved. • ADC interface model updated (see Table 32 and Figure 30).			
LPC178X_7X v.2	20110527	Objective data sheet	-	LPC178X_7X v.1
Modifications:	• Symbol names in Table 3 to Table 5 abbreviated. • Reserved functions added in Table 3. • Added function LCD_VD[5] to pin P0[10]. • Added function LCD_VD[10] to pin P0[11]. • Added function LCD_VD[13] to pin P0[19]. • Added function LCD_VD[14] to pin P0[20]. • Added function U4_SCLK to pin P0[21]. • Added function • Added function MOSI to pin P5[0]. • Added function SSP2_MISO to pin P5[1]. • Added EMC dynamic characteristics.			
LPC178X_7X v.1	20110524	Objective data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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