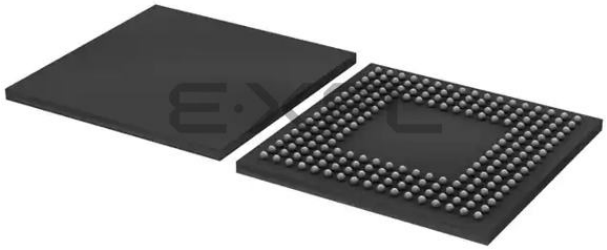

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, Microwire, Memory Card, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, Motor Control PWM, POR, PWM, WDT
Number of I/O	165
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 8x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-TFBGA
Supplier Device Package	208-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1788fet208-551

Table 2. LPC178x/7x ordering options

All parts include two CAN channels, three SSP interfaces, three I^2C interfaces, one I^2S interface, DAC, and an 8-channel 12-bit ADC.

Type number	Device order part number	Flash (kB)	Main SRAM (kB)	Peripheral SRAM (kB)	Total SRAM (kB)	EEPROM (byte)	Ethernet	USB	UART	EMC bus width (bit) [1]	GPIO	LCD	QEI	SD/ MMC
LPC178x														
LPC1788FBD208	LPC1788FBD208/CP3E	512	64	16 × 2	96	4032	Y	H/O/D	5	32	165	Y	Y	Y
LPC1788FET208	LPC1788FET208,551	512	64	16 × 2	96	4032	Y	H/O/D	5	32	165	Y	Y	Y
LPC1788FET180	LPC1788FET180,551	512	64	16 × 2	96	4032	Y	H/O/D	5	16	141	Y	Y	Y
LPC1788FBD144	LPC1788FBD144,551	512	64	16 × 2	96	4032	Y	H/O/D	5	8	109	Y	Y	Y
LPC1787FBD208	LPC1787FBD208,551	512	64	16 × 2	96	4032	N	H/O/D	5	32	165	Y	Y	Y
LPC1786FBD208	LPC1786FBD208,551	256	64	16	80	4032	Y	H/O/D	5	32	165	Y	Y	Y
LPC1785FBD208	LPC1785FBD208K	256	64	16	80	4032	N	H/O/D	5	32	165	Y	N	Y
LPC177x														
LPC1778FBD208	LPC1778FBD208,551	512	64	16 × 2	96	4032	Y	H/O/D	5	32	165	N	Y	Y
LPC1778FET208	LPC1778FET208,551	512	64	16 × 2	96	4032	Y	H/O/D	5	32	165	N	Y	Y
LPC1778FET180	LPC1778FET180,551	512	64	16 × 2	96	4032	Y	H/O/D	5	16	141	N	Y	Y
LPC1778FBD144	LPC1778FBD144,551	512	64	16 × 2	96	4032	Y	H/O/D	5	8	109	N	Y	Y
LPC1777FBD208	LPC1777FBD208,551	512	64	16 × 2	96	4032	N	H/O/D	5	32	165	N	Y	Y
LPC1776FBD208	LPC1776FBD208,551	256	64	16	80	4032	Y	H/O/D	5	32	165	N	Y	Y
LPC1776FET180	LPC1776FET180,551	256	64	16	80	4032	Y	H/O/D	5	16	141	N	Y	Y
LPC1774FBD208	LPC1774FBD208,551	128	32	8	40	2048	N	D	5	32	165	N	N	N
LPC1774FBD144	LPC1774FBD144,551	128	32	8	40	2048	N	D	4[2]	8	109	N	N	N

[1] Maximum data bus width of the External Memory Controller (EMC) depends on package size. Smaller widths may be used.

[2] USART4 not available.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[13]	45	R2	J5	32	[5]	I; PU	I/O	**P0[13] —** General purpose digital input/output pin.
							O	**USB_UP_LED2 —** USB port 2 GoodLink LED indicator. It is LOW when the device is configured (non-control endpoints enabled), or when the host is enabled and has detected a device on the bus. It is HIGH when the device is not configured, or when host is enabled and has not detected a device on the bus, or during global suspend. It transitions between LOW and HIGH (flashes) when the host is enabled and detects activity on the bus.
							I/O	**SSP1_MOSI —** Master Out Slave In for SSP1.
							I	**ADC0_IN[7] —** A/D converter 0, input 7. When configured as an ADC input, the digital function of the pin must be disabled.
P0[14]	69	T7	M5	48	[3]	I; PU	I/O	**P0[14] —** General purpose digital input/output pin.
							O	**$\overline{\text{USB\_HSTEN2}}$ —** Host Enabled status for USB port 2.
							I/O	**SSP1_SSEL —** Slave Select for SSP1.
							O	**USB_CONNECT2 —** SoftConnect control for USB port 2. Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature.
P0[15]	128	J16	H13	89	[3]	I; PU	I/O	**P0[15] —** General purpose digital input/output pin.
							O	**U1_TXD —** Transmitter output for UART1.
							I/O	**SSP0_SCK —** Serial clock for SSP0.
P0[16]	130	J14	H14	90	[3]	I; PU	I/O	**P0[16] —** General purpose digital input/output pin.
							I	**U1_RXD —** Receiver input for UART1.
							I/O	**SSP0_SSEL —** Slave Select for SSP0.
P0[17]	126	K17	J12	87	[3]	I; PU	I/O	**P0[17] —** General purpose digital input/output pin.
							I	**U1_CTS —** Clear to Send input for UART1.
							I/O	**SSP0_MISO —** Master In Slave Out for SSP0.
P0[18]	124	K15	J13	86	[3]	I; PU	I/O	**P0[18] —** General purpose digital input/output pin.
							I	**U1_DCD —** Data Carrier Detect input for UART1.
							I/O	**SSP0_MOSI —** Master Out Slave In for SSP0.
P0[19]	122	L17	J10	85	[3]	I; PU	I/O	**P0[19] —** General purpose digital input/output pin.
							I	**U1_DSR —** Data Set Ready input for UART1.
							O	**SD_CLK —** Clock output line for SD card interface.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I2C pad).

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P0[25]	14	F1	E4	10	[5]	I; PU	I/O	**P0[25] —** General purpose digital input/output pin.
							I	**ADC0_IN[2] —** A/D converter 0, input 2. When configured as an ADC input, the digital function of the pin must be disabled.
							I/O	**I2S_RX_SDA —** Receive data. It is driven by the transmitter and read by the receiver. Corresponds to the signal SD in the *I^2S-bus specification*.
							O	**U3_TXD —** Transmitter output for UART3.
P0[26]	12	E1	D1	8	[7]	I; PU	I/O	**P0[26] —** General purpose digital input/output pin.
							I	**ADC0_IN[3] —** A/D converter 0, input 3. When configured as an ADC input, the digital function of the pin must be disabled.
							O	**DAC_OUT —** D/A converter output. When configured as the DAC output, the digital function of the pin must be disabled.
							I	**U3_RXD —** Receiver input for UART3.
P0[27]	50	T1	L3	35	[8]	I	I/O	**P0[27] —** General purpose digital input/output pin.
							I/O	**I2C0_SDA —** I^2C0 data input/output (this pin uses a specialized I2C pad).
							I/O	**USB_SDA1 —** I2C serial data for communication with an external USB transceiver.
P0[28]	48	R3	M1	34	[8]	I	I/O	**P0[28] —** General purpose digital input/output pin.
							I/O	**I2C0_SCL —** I^2C0 clock input/output (this pin uses a specialized I2C pad).
							I/O	**USB_SCL1 —** I2C serial clock for communication with an external USB transceiver.
P0[29]	61	U4	K5	42	[9]	I	I/O	**P0[29] —** General purpose digital input/output pin.
							I/O	**USB_D+1 —** USB port 1 bidirectional D+ line.
							I	**$\overline{\text{EINT0}}$ —** External interrupt 0 input.
P0[30]	62	R6	N4	43	[9]	I	I/O	**P0[30] —** General purpose digital input/output pin.
							I/O	**USB_D–1 —** USB port 1 bidirectional D− line.
							I	**$\overline{\text{EINT1}}$ —** External interrupt 1 input.
P0[31]	51	T2	N1	36	[9]	I	I/O	**P0[31] —** General purpose digital input/output pin.
							I/O	**USB_D+2 —** USB port 2 bidirectional D+ line.
P1[0] to P1[31]							I/O	**Port 1:** Port 1 is a 32 bit I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block
P1[0]	196	A3	B5	136	[3]	I; PU	I/O	**P1[0] —** General purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0 (RMII/MII interface).
							-	**R —** Function reserved.
							I	**T3_CAP1 —** Capture input for Timer 3, channel 1.
							I/O	**SSP2_SCK —** Serial clock for SSP2.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P2[5]	140	F16	F12	97	[3]	I; PU	I/O	**P2[5] —** General purpose digital input/output pin.
							O	**PWM1[6] —** Pulse Width Modulator 1, channel 6 output.
							O	**U1_DTR —** Data Terminal Ready output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							O	**T2_MAT0 —** Match output for Timer 2, channel 0.
							-	**R —** Function reserved.
							O	**TRACEDATA[0] —** Trace data, bit 0.
							-	**R —** Function reserved.
							O	**LCD_LP —** Line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
P2[6]	138	E17	F13	96	[3]	I; PU	I/O	**P2[6] —** General purpose digital input/output pin.
							I	**PWM1_CAP0 —** Capture input for PWM1, channel 0.
							I	**U1_RI —** Ring Indicator input for UART1.
							I	**T2_CAP0 —** Capture input for Timer 2, channel 0.
							O	**U2_OE —** RS-485/EIA-485 output enable signal for UART2.
							O	**TRACECLK —** Trace clock.
							O	**LCD_VD[0] —** LCD data.
							O	**LCD_VD[4] —** LCD data.
P2[7]	136	G16	G11	95	[3]	I; PU	I/O	**P2[7] —** General purpose digital input/output pin.
							I	**CAN_RD2 —** CAN2 receiver input.
							O	**U1_RTS —** Request to Send output for UART1. Can also be configured to be an RS-485/EIA-485 output enable signal for UART1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**LCD_VD[1] —** LCD data.
							O	**LCD_VD[5] —** LCD data.
P2[8]	134	H15	G14	93	[3]	I; PU	I/O	**P2[8] —** General purpose digital input/output pin.
							O	**CAN_TD2 —** CAN2 transmitter output.
							O	**U2_TXD —** Transmitter output for UART2.
							I	**U1_CTS —** Clear to Send input for UART1.
							O	**ENET_MDC —** Ethernet MIIM clock.
							-	**R —** Function reserved.
							O	**LCD_VD[2] —** LCD data.
							O	**LCD_VD[6] —** LCD data.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P3[0]	197	B4	D6	137	[3]	I; PU	I/O	**P3[0] —** General purpose digital input/output pin.
							I/O	**EMC_D[0] —** External memory data line 0.
P3[1]	201	B3	E6	140	[3]	I; PU	I/O	**P3[1] —** General purpose digital input/output pin.
							I/O	**EMC_D[1] —** External memory data line 1.
P3[2]	207	B1	A2	144	[3]	I; PU	I/O	**P3[2] —** General purpose digital input/output pin.
							I/O	**EMC_D[2] —** External memory data line 2.
P3[3]	3	E4	G5	2	[3]	I; PU	I/O	**P3[3] —** General purpose digital input/output pin.
							I/O	**EMC_D[3] —** External memory data line 3.
P3[4]	13	F2	D3	9	[3]	I; PU	I/O	**P3[4] —** General purpose digital input/output pin.
							I/O	**EMC_D[4] —** External memory data line 4.
P3[5]	17	G1	E3	12	[3]	I; PU	I/O	**P3[5] —** General purpose digital input/output pin.
							I/O	**EMC_D[5] —** External memory data line 5.
P3[6]	23	J1	F4	16	[3]	I; PU	I/O	**P3[6] —** General purpose digital input/output pin.
							I/O	**EMC_D[6] —** External memory data line 6.
P3[7]	27	L1	G3	19	[3]	I; PU	I/O	**P3[7] —** General purpose digital input/output pin.
							I/O	**EMC_D[7] —** External memory data line 7.
P3[8]	191	D8	A6	-	[3]	I; PU	I/O	**P3[8] —** General purpose digital input/output pin.
							I/O	**EMC_D[8] —** External memory data line 8.
P3[9]	199	C5	A4	-	[3]	I; PU	I/O	**P3[9] —** General purpose digital input/output pin.
							I/O	**EMC_D[9] —** External memory data line 9.
P3[10]	205	B2	B3	-	[3]	I; PU	I/O	**P3[10] —** General purpose digital input/output pin.
							I/O	**EMC_D[10] —** External memory data line 10.
P3[11]	208	D5	B2	-	[3]	I; PU	I/O	**P3[11] —** General purpose digital input/output pin.
							I/O	**EMC_D[11] —** External memory data line 11.
P3[12]	1	D4	A1	-	[3]	I; PU	I/O	**P3[12] —** General purpose digital input/output pin.
							I/O	**EMC_D[12] —** External memory data line 12.
P3[13]	7	C1	C1	-	[3]	I; PU	I/O	**P3[13] —** General purpose digital input/output pin.
							I/O	**EMC_D[13] —** External memory data line 13.
P3[14]	21	H2	F1	-	[3]	I; PU	I/O	**P3[14] —** General purpose digital input/output pin.
							I/O	**EMC_D[14] —** External memory data line 14.
P3[15]	28	M1	G4	-	[3]	I; PU	I/O	**P3[15] —** General purpose digital input/output pin.
							I/O	**EMC_D[15] —** External memory data line 15.
P3[16]	137	F17	-	-	[3]	I; PU	I/O	**P3[16] —** General purpose digital input/output pin.
							I/O	**EMC_D[16] —** External memory data line 16.
							O	**PWM0[1] —** Pulse Width Modulator 0, output 1.
							O	**U1_TXD —** Transmitter output for UART1.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
P4[1]	79	U10	M7	55	[3]	I; PU	I/O	**P4[1] —** General purpose digital input/output pin.
							I/O	**EMC_A[1] —** External memory address line 1.
P4[2]	83	T11	M8	58	[3]	I; PU	I/O	**P4[2] —** General purpose digital input/output pin.
							I/O	**EMC_A[2] —** External memory address line 2.
P4[3]	97	U16	K9	68	[3]	I; PU	I/O	**P4[3] —** General purpose digital input/output pin.
							I/O	**EMC_A[3] —** External memory address line 3.
P4[4]	103	R15	P13	72	[3]	I; PU	I/O	**P4[4] —** General purpose digital input/output pin.
							I/O	**EMC_A[4] —** External memory address line 4.
P4[5]	107	R16	H10	74	[3]	I; PU	I/O	**P4[5] —** General purpose digital input/output pin.
							I/O	**EMC_A[5] —** External memory address line 5.
P4[6]	113	M14	K10	78	[3]	I; PU	I/O	**P4[6] —** General purpose digital input/output pin.
							I/O	**EMC_A[6] —** External memory address line 6.
P4[7]	121	L16	K12	84	[3]	I; PU	I/O	**P4[7] —** General purpose digital input/output pin.
							I/O	**EMC_A[7] —** External memory address line 7.
P4[8]	127	J17	J11	88	[3]	I; PU	I/O	**P4[8] —** General purpose digital input/output pin.
							I/O	**EMC_A[8] —** External memory address line 8.
P4[9]	131	H17	H12	91	[3]	I; PU	I/O	**P4[9] —** General purpose digital input/output pin.
							I/O	**EMC_A[9] —** External memory address line 9.
P4[10]	135	G17	G12	94	[3]	I; PU	I/O	**P4[10] —** General purpose digital input/output pin.
							I/O	**EMC_A[10] —** External memory address line 10.
P4[11]	145	F14	F11	101	[3]	I; PU	I/O	**P4[11] —** General purpose digital input/output pin.
							I/O	**EMC_A[11] —** External memory address line 11.
P4[12]	149	C16	F10	104	[3]	I; PU	I/O	**P4[12] —** General purpose digital input/output pin.
							I/O	**EMC_A[12] —** External memory address line 12.
P4[13]	155	B16	B14	108	[3]	I; PU	I/O	**P4[13] —** General purpose digital input/output pin.
							I/O	**EMC_A[13] —** External memory address line 13.
P4[14]	159	B15	E8	110	[3]	I; PU	I/O	**P4[14] —** General purpose digital input/output pin.
							I/O	**EMC_A[14] —** External memory address line 14.
P4[15]	173	A11	C10	120	[3]	I; PU	I/O	**P4[15] —** General purpose digital input/output pin.
							I/O	**EMC_A[15] —** External memory address line 15.
P4[16]	101	U17	N12	-	[3]	I; PU	I/O	**P4[16] —** General purpose digital input/output pin.
							I/O	**EMC_A[16] —** External memory address line 16.
P4[17]	104	P14	N13	-	[3]	I; PU	I/O	**P4[17] —** General purpose digital input/output pin.
							I/O	**EMC_A[17] —** External memory address line 17.
P4[18]	105	P15	P14	-	[3]	I; PU	I/O	**P4[18] —** General purpose digital input/output pin.
							I/O	**EMC_A[18] —** External memory address line 18.

Table 3. Pin description *…continued*

Not all functions are available on all parts. See Table 2 (Ethernet, USB, LCD, QEI, SD/MMC, DAC pins) and Table 7 (EMC pins).

Symbol	Pin LQFP208	Ball TFBGA208	Ball TFBGA180	Pin LQFP144		Reset state[1]	Type[2]	Description
VBAT	38	M3	K1	27		-	I	RTC power supply: 3.0 V on this pin supplies power to the RTC.
$V_{DD(REG)(3V3)}$	26, 86, 174	H4, P11, D11	G1, N9, E9	18, 60, 121		-	S	3.3 V regulator supply voltage: This is the power supply for the on-chip voltage regulator that supplies internal logic.
V_{DDA}	20	G4	F2	14		-	S	Analog 3.3 V pad supply voltage: This can be connected to the same supply as $V_{DD(3V3)}$ but should be isolated to minimize noise and error. This voltage is used to power the ADC and DAC. **Note: This pin should be tied to 3.3 V if the ADC and DAC are not used.**
$V_{DD(3V3)}$	15, 60, 71, 89, 112, 125, 146, 165, 181, 198	G3, P6, P8, U13, P17, K16, C17, B13, C9, D7	E2, L4, K8, L11, J14, E12, E10, C5	41, 62, 77, 102, 114, 138		-	S	3.3 V supply voltage: This is the power supply voltage for I/O other than pins in the VBAT domain.
VREFP	24	K1	G2	17		-	S	ADC positive reference voltage: This should be the same voltage as V_{DDA}, but should be isolated to minimize noise and error. The voltage level on this pin is used as a reference for ADC and DAC. **Note: This pin should be tied to 3.3 V if the ADC and DAC are not used.**
V_{SS}	33, 63, 77, 93, 114, 133, 148, 169, 189, 200	L3, T5, R9, P12, N16, H14, E15, A12, B6, A2	H4, P4, L9, L13, G13, D13, C11, B4	44, 65, 79, 103, 117, 139		-	G	Ground: 0 V reference for digital IO pins.
V_{SSREG}	32, 84, 172	D12, K4, P10	H3, L8, A10	22, 59, 119		-	G	Ground: 0 V reference for internal logic.
V_{SSA}	22	J2	F3	15		-	G	Analog ground: 0 V power supply and reference for the ADC and DAC. This should be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
XTAL1	44	M4	L2	31	[14] [16]	-	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	46	N4	K4	33	[14] [16]	-	O	Output from the oscillator amplifier.

The LPC178x/7x EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

See Table 6 for EMC memory access.

7.10.1 Features

- Dynamic memory interface support including single data rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.11 General purpose DMA controller

The GPDMA is an AMBA AHB compliant peripheral allowing selected peripherals to have DMA support.

The GPDMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. The source and destination areas can each be either a memory region or a peripheral and can be accessed through the AHB master. The GPDMA controller allows data transfers between the various on-chip SRAM areas and supports the SD/MMC card interface, all SSPs, the I^2S, all UARTs, the A/D Converter, and the D/A Converter peripherals. DMA can also be triggered by selected timer match conditions. Memory-to-memory transfers and transfers to or from GPIO are supported.

7.23 I²S-bus serial I/O controllers

The LPC178x/7x contain one I²S-bus interface. The I²S-bus provides a standard communication interface for digital audio applications.

The I²S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. The basic I²S connection has one master, which is always the master, and one slave. The I²S interface on the LPC178x/7x provides a separate transmit and receive channel, each of which can operate as either a master or a slave.

7.23.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- The sampling frequency can range from 16 kHz to 48 kHz (16, 22.05, 32, 44.1, 48) kHz.
- Configurable word select period in master mode (separately for I²S input and output).
- Two 8 word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop and mute options separately for I²S input and I²S output.

7.24 CAN controller and acceptance filters

The LPC178x/7x contain one CAN controller with two channels.

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high-speed networks to low cost multiplex wiring.

The CAN block is intended to support multiple CAN buses simultaneously, allowing the device to be used as a gateway, switch, or router between two of CAN buses in industrial or automotive applications.

Each CAN controller has a register structure similar to the NXP SJA1000 and the PeliCAN Library block, but the 8-bit registers of those devices have been combined in 32-bit words to allow simultaneous access in the ARM environment. The main operational difference is that the recognition of received Identifiers, known in CAN terminology as Acceptance Filtering, has been removed from the CAN controllers and centralized in a global Acceptance Filter.

7.24.1 Features

- Two CAN controllers and buses.
- Data rates to 1 Mbit/s on each bus.
- 32-bit register and RAM access.
- Compatible with *CAN specification 2.0B, ISO 11898-1*.

7.33.1.3 RTC oscillator

The RTC oscillator provides a 1 Hz clock to the RTC and a 32 kHz clock output that can be output on the CLKOUT pin in order to allow trimming the RTC oscillator without interference from a probe.

7.33.1.4 Watchdog oscillator

The Watchdog Timer has a dedicated watchdog oscillator that provides a 500 kHz clock to the Watchdog Timer. The watchdog oscillator is always running if the Watchdog Timer is enabled. The Watchdog oscillator clock can be output on the CLKOUT pin in order to allow observe its frequency.

In order to allow Watchdog Timer operation with minimum power consumption, which can be important in reduced power modes, the Watchdog oscillator frequency is not tightly controlled. The Watchdog oscillator frequency will vary over temperature and power supply within a particular part, and may vary by processing across different parts. This variation should be taken into account when determining Watchdog reload values.

Within a particular part, temperature and power supply variations can produce up to a ±17 % frequency variation. Frequency variation between devices under the same operating conditions can be up to ±30 %.

7.33.2 Main PLL (PLL0) and Alternate PLL (PLL1)

PLL0 (also called the Main PLL) and PLL1 (also called the Alternate PLL) are functionally identical but have somewhat different input possibilities and output connections. These possibilities are shown in Figure 7. The Main PLL can receive its input from either the IRC or the main oscillator and can potentially be used to provide the clocks to nearly everything on the device. The Alternate PLL receives its input only from the main oscillator and is intended to be used as an alternate source of clocking to the USB. The USB has timing needs that may not always be filled by the Main PLL.

Both PLLs are disabled and powered off on reset. If the Alternate PLL is left disabled, the USB clock can be supplied by PLL0 if everything is set up to provide 48 MHz to the USB clock through that route. The source for each clock must be selected via the CLKSEL registers and can be further reduced by clock dividers as needed.

PLL0 accepts an input clock frequency from either the IRC or the main oscillator. If only the Main PLL is used, then its output frequency must be an integer multiple of all other clocks needed in the system. PLL1 takes its input only from the main oscillator, requiring an external crystal in the range of 10 to 25 MHz. In each PLL, the Current Controlled Oscillator (CCO) operates in the range of 156 MHz to 320 MHz, so there are additional dividers to bring the output down to the desired frequencies. The minimum output divider value is 2, insuring that the output of the PLLs have a 50 % duty cycle.

If the USB is used, the possibilities for the CPU clock and other clocks will be limited by the requirements that the frequency be precise and very low jitter, and that the PLL0 output must be a multiple of 48 MHz. Even multiples of 48 MHz that are within the operating range of the PLL are 192 MHz and 288 MHz. Also, only the main oscillator in conjunction with the PLL can meet the precision and jitter specifications for USB. It is due to these limitations that the Alternate PLL is provided.

On the wake-up of Power-down mode, if the IRC was used before entering Power-down mode, it will take IRC 60 μs to start-up. After this, four IRC cycles will expire before the code execution can then be resumed if the code was running from SRAM. In the meantime, the flash wake-up timer then counts 12 MHz IRC clock cycles to make the 100 μs flash start-up time. When it times out, access to the flash will be allowed. Users need to reconfigure the PLL and clock dividers accordingly.

7.33.4.4 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the RTC module and the $\overline{\text{RESET}}$ pin.

To optimize power conservation, the user has the additional option of turning off or retaining power to the 32 kHz oscillator. It is also possible to use external circuitry to turn off power to the on-chip regulator via the $V_{DD(REG)(3V3)}$ pins and/or the I/O power via the $V_{DD(3V3)}$ pins after entering Deep Power-down mode. Power must be restored before device operation can be restarted.

The LPC178x/7x can wake up from Deep power-down mode via the $\overline{\text{RESET}}$ pin or an alarm match event of the RTC.

7.33.4.5 Wake-up Interrupt Controller (WIC)

The WIC allows the CPU to automatically wake up from any enabled priority interrupt that can occur while the clocks are stopped in Deep-sleep, Power-down, and Deep power-down modes.

The WIC works in connection with the Nested Vectored Interrupt Controller (NVIC). When the CPU enters Deep-sleep, Power-down, or Deep power-down mode, the NVIC sends a mask of the current interrupt situation to the WIC.This mask includes all of the interrupts that are both enabled and of sufficient priority to be serviced immediately. With this information, the WIC simply notices when one of the interrupts has occurred and then it wakes up the CPU.

The WIC eliminates the need to periodically wake up the CPU and poll the interrupts resulting in additional power savings.

7.33.5 Peripheral power control

A power control for peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

7.33.6 Power domains

The LPC178x/7x provide two independent power domains that allow the bulk of the device to have power removed while maintaining operation of the RTC and the backup registers.

On the LPC178x/7x, I/O pads are powered by $V_{DD(3V3)}$, while $V_{DD(REG)(3V3)}$ powers the on-chip voltage regulator which in turn provides power to the CPU and most of the peripherals.

Depending on the LPC178x/7x application, a design can use two power options to manage power consumption.

10. Static characteristics

Table 13. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supply pins							
$V_{DD(3V3)}$	supply voltage (3.3 V)	external rail	[2]	2.4	3.3	3.6	V
$V_{DD(REG)(3V3)}$	regulator supply voltage (3.3 V)			2.4	3.3	3.6	V
V_{DDA}	analog 3.3 V pad supply voltage		[3]	2.7	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[4]	2.1	3.0	3.6	V
$V_{i(VREFP)}$	input voltage on pin VREFP		[3]	2.7	3.3	V_{DDA}	V
$I_{DD(REG)(3V3)}$	regulator supply current (3.3 V)	active mode; code `while(1){}` executed from flash; all peripherals disabled PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]	-	7	-	mA
		CCLK = 120 MHz; PLL enabled	[5][7]	-	51	-	mA
		active mode; code `while(1){}` executed from flash; all peripherals enabled; PCLK = CCLK/4					
		CCLK = 12 MHz; PLL disabled	[5][6]		14		
		CCLK = 120 MHz; PLL enabled	[5][7]		100		mA
		Sleep mode	[5][8]	-	5	-	mA
		Deep-sleep mode	[5][9]	-	550	-	µA
		Power-down mode	[5][9]	-	280	-	µA
I_{BAT}	battery supply current	RTC running; part powered down; $V_{DD(REG)(3V3)}$ =0 V; $V_{i(VBAT)}$ = 3.0 V; $V_{DD(3V3)}$ = 0 V.	[10]	-	1	-	µA
		part powered; $V_{DD(REG)(3V3)}$ = 3.3 V; $V_{i(VBAT)}$ = 3.0 V	[11]		<10		nA

Table 17. Dynamic characteristics: Static external memory interface *…continued*

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
t_{deact}	deactivation time	WR_8; PB = 0; PB = 1	[3]	−2.7	−3.4	−4.7	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	WR_9; PB = 0	[3]	2.8 + $T_{cy(clk)}$ × (1 + WAITWEN)	3.7 + $T_{cy(clk)}$ × (1 + WAITWEN)	5.1 + $T_{cy(clk)}$ × (1 + WAITWEN)	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	WR_{10}; PB = 0	[3]	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 2.6	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 3.4	(WAITWR − WAITWEN + 3) × $T_{cy(clk)}$ − 4.9	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	WR_{11}; PB = 0	[3][6]	2.6 + $T_{cy(clk)}$	3.3 + $T_{cy(clk)}$	4.4 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	WR12; PB = 0	[3]	2.7 + $T_{cy(clk)}$	3.6 + $T_{cy(clk)}$	4.8 + $T_{cy(clk)}$	ns

[1] Parameters are shown as RD_n or WD_n in Figure 16 as indicated in the Conditions column.

[2] Parameters specified for 40 % of $V_{DD(3V3)}$ for rising edges and 60 % of $V_{DD(3V3)}$ for falling edges.

[3] $T_{cy(clk)}$ = 1/EMC_CLK (see *LPC178x/7x User manual UM10470*).

[4] Latest of address valid, $\overline{EMC\_CSx}$ LOW, $\overline{EMC\_OE}$ LOW, $\overline{EMC\_BLSx}$ LOW (PB = 1).

[5] After End Of Read (EOR): Earliest of $\overline{EMC\_CSx}$ HIGH, $\overline{EMC\_OE}$ HIGH, $\overline{EMC\_BLSx}$ HIGH (PB = 1), address invalid.

[6] End Of Write (EOW): Earliest of address invalid, $\overline{EMC\_CSx}$ HIGH, $\overline{EMC\_BLSx}$ HIGH (PB = 1).

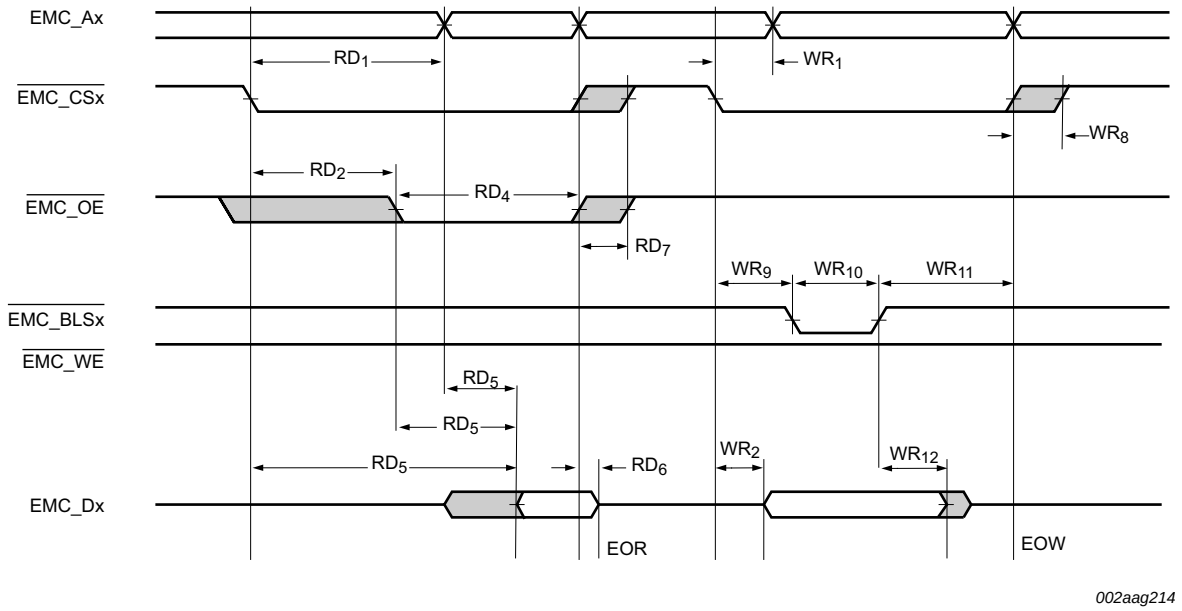


Fig 16. External static memory read/write access (PB = 0)

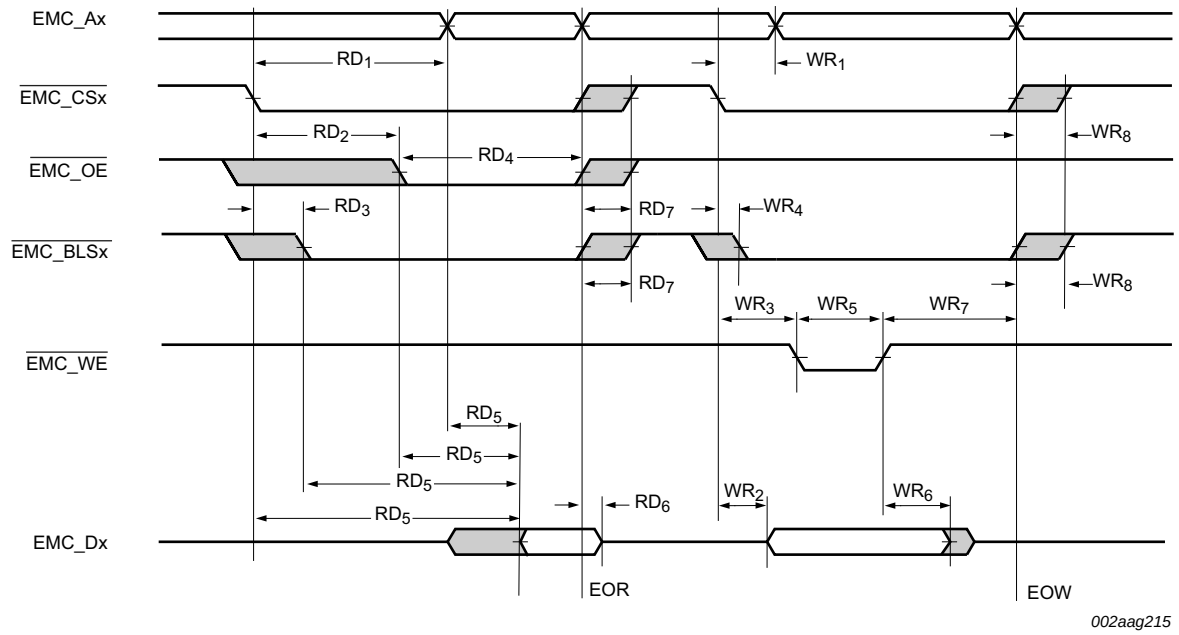


Fig 17. External static memory read/write access (PB =1)

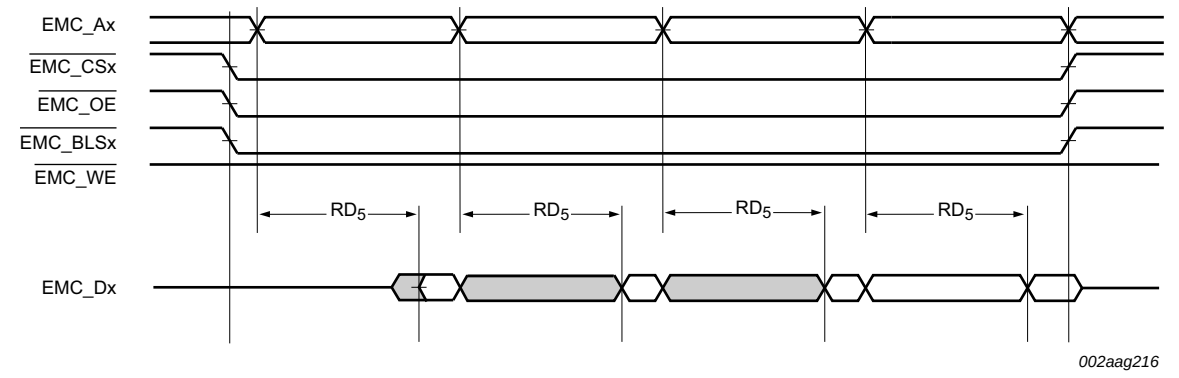


Fig 18. External static memory burst read cycle

Table 18. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 00
C_L = 10 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(3V3)}$ = 3.0 V to 3.6 V. Values guaranteed by design. t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling; $t_{clk0dly}$ is programmable delay value for the EMC_CLKOUT0 output; $t_{clk1dly}$ is programmable delay value for the EMC_CLKOUT1 output.

Symbol	Parameter		Min	Typ	Max	Unit
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	12.5	-	-	ns
$t_{d(SV)}$	chip select valid delay time	[2]	-	$t_{clkndly}$ + 4.2	$t_{clk0dly}$ + 6.2	ns
$t_{h(S)}$	chip select hold time	[2]	$t_{clkndly}$ + 1.2	$t_{clkndly}$ + 1.8	-	ns
$t_{d(RASV)}$	row address strobe valid delay time	[2]	-	$t_{clkndly}$ + 4.2	$t_{clkndly}$ + 6.2	ns
$t_{h(RAS)}$	row address strobe hold time	[2]	$t_{clkndly}$+ 1.3	$t_{clkndly}$ + 1.9	-	ns
$t_{d(CASV)}$	column address strobe valid delay time	[2]	-	$t_{clkndly}$ + 4.2	$t_{clkndly}$ + 6.2	ns
$t_{h(CAS)}$	column address strobe hold time	[2]	$t_{clkndly}$ + 1.3	$t_{clkndly}$ + 1.9	-	ns
$t_{d(WV)}$	write valid delay time	[2]	-	$t_{clkndly}$ + 5.2	$t_{clkndly}$ + 7.7	ns
$t_{h(W)}$	write hold time	[2]	$t_{clkndly}$ + 1.6	$t_{clkndly}$ + 2.4		ns
$t_{d(AV)}$	address valid delay time	[2]	-	$t_{clkndly}$ + 5.0	$t_{clkndly}$ + 7.4	ns
$t_{h(A)}$	address hold time	[2]	$t_{clkndly}$ + 1.1	$t_{clkndly}$ + 1.7	-	ns
Read cycle parameters when EMC_CLKOUT0 used						
$t_{su(D)}$	data input set-up time		7.1 - t_{fbdly}	4.8 - t_{fbdly}	-	ns
$t_{h(D)}$	data input hold time		-1.9 + t_{fbdly}	-2.5 + t_{fbdly}	-	ns
Read cycle parameters when EMC_CLKOUT1 used						
$t_{su(D)}$	data input set-up time		7.1 - t_{fbdly} + ($t_{clk1dly}$ - $t_{clk0dly}$)	4.8 - t_{fbdly} + ($t_{clk1dly}$ - $t_{clk0dly}$)	-	ns
$t_{h(D)}$	data input hold time		-1.9 + t_{fbdly} - ($t_{clk1dly}$ - $t_{clk0dly}$)	-2.5 + t_{fbdly} - ($t_{clk1dly}$ - $t_{clk0dly}$)	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time	[2]	-	$t_{clkndly}$ + 5.8	$t_{clkndly}$ + 8.7	ns
$t_{h(Q)}$	data output hold time	[2]	$t_{clkndly}$ + 0.4	$t_{clkndly}$ + 0.6	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] $t_{clkndly}$ represents $t_{clk0dly}$ when EMC_CLKOUT0 clocks SDRAM. $t_{clkndly}$represents $t_{clk1dly}$ when EMC_CLKOUT1 clocks SDRAM.

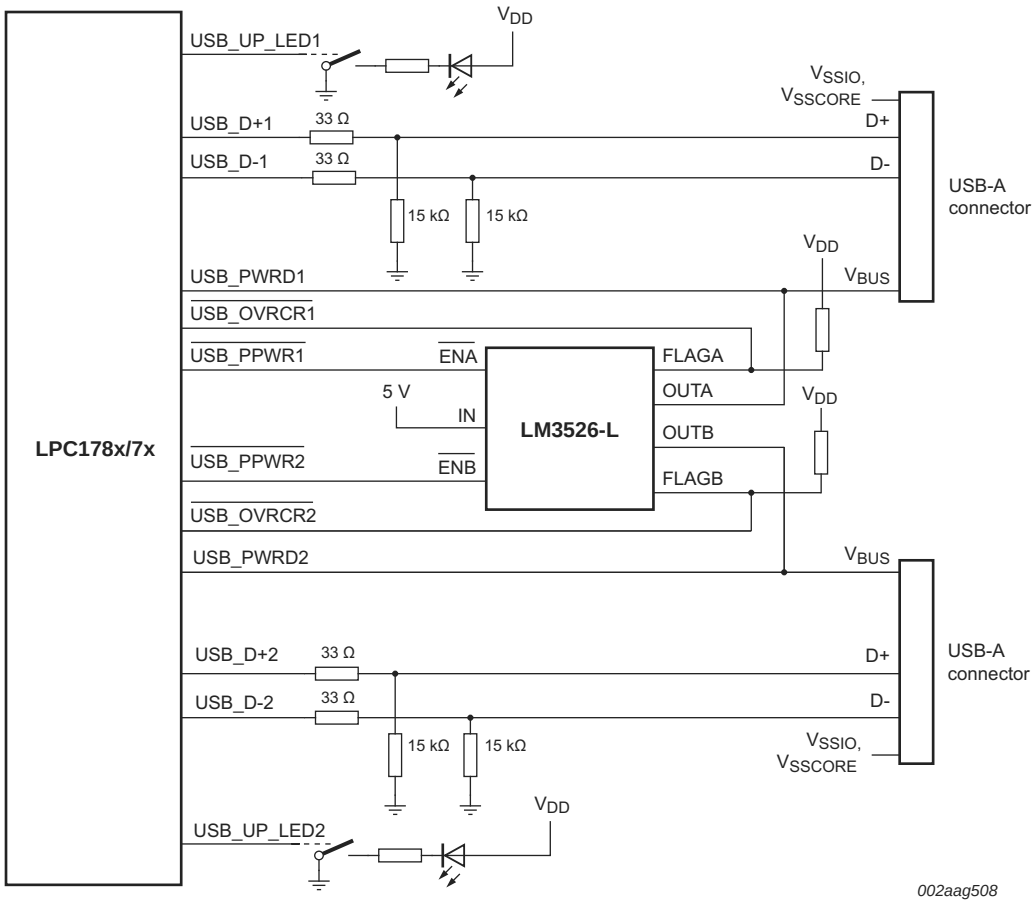


Fig 34. USB host port configuration: port 1 and port 2 as hosts

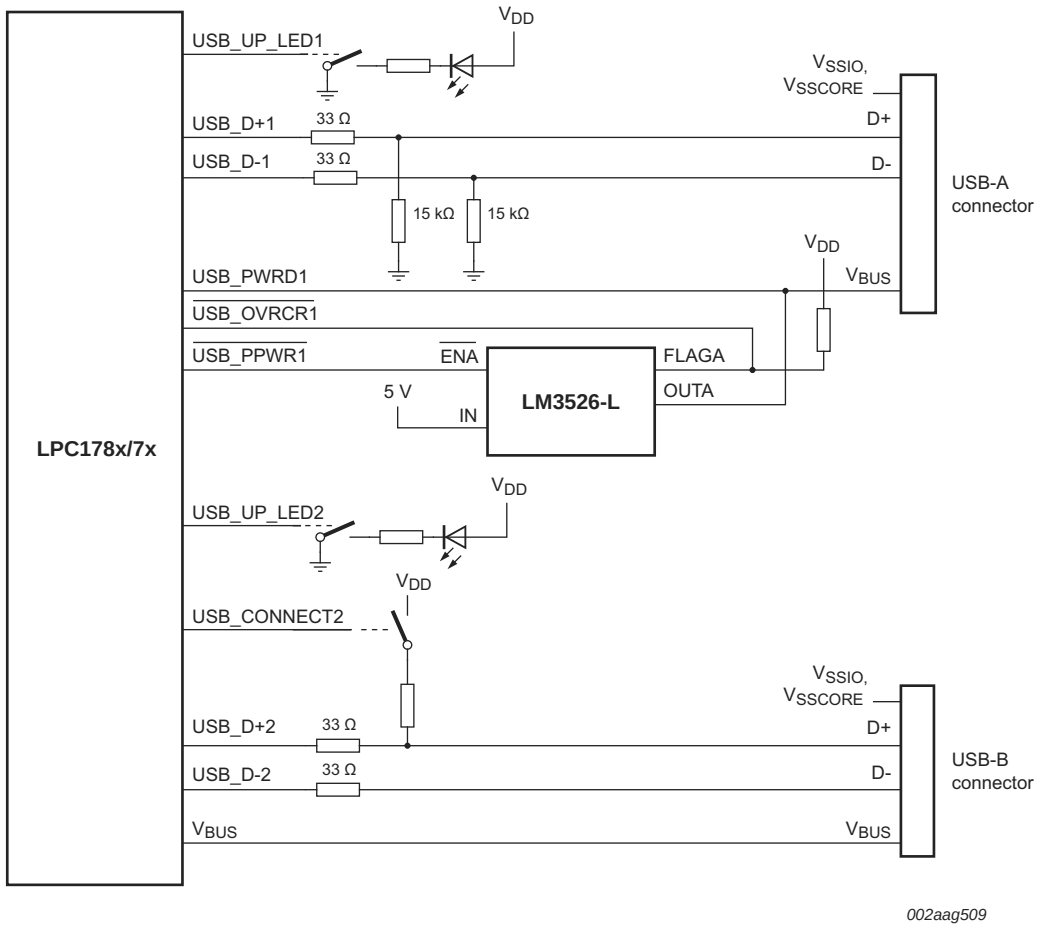


Fig 35. USB device port configuration: port 1 host and port 2 device

14.2 Crystal oscillator XTAL input and component selection

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

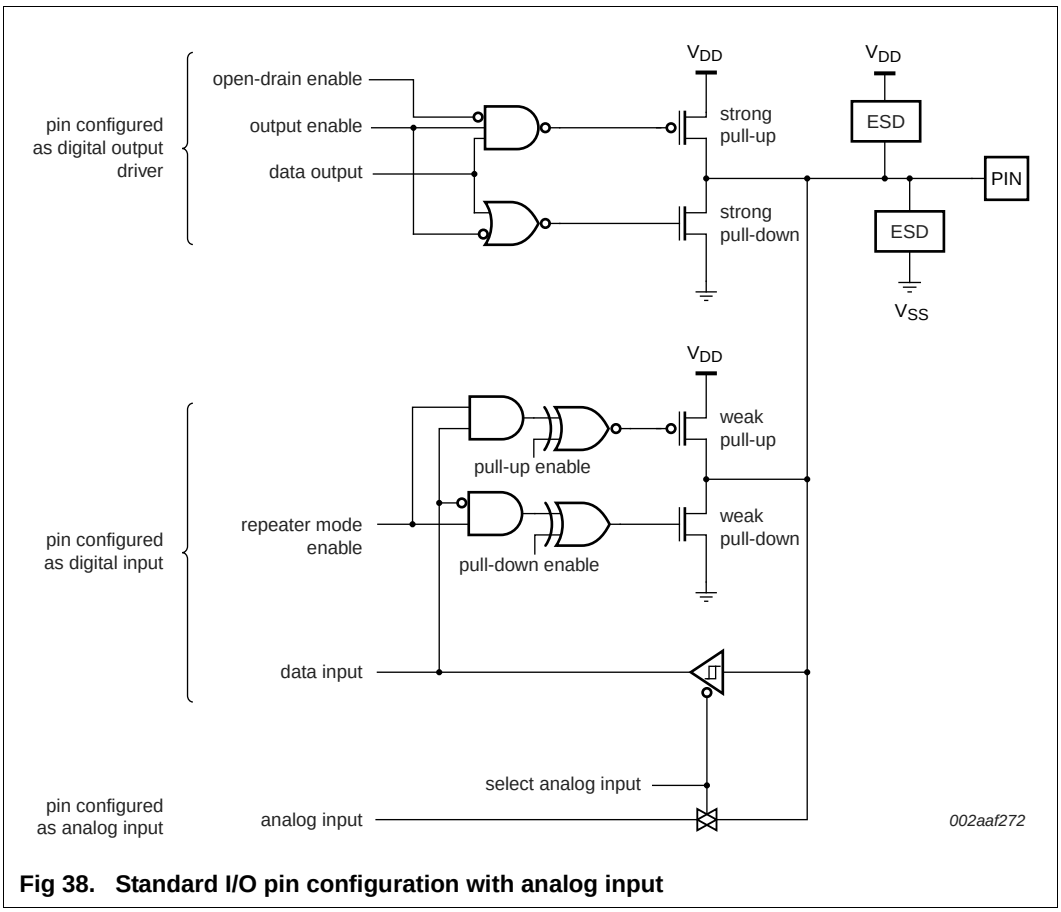


Fig 38. Standard I/O pin configuration with analog input

14.5 Reset pin configuration

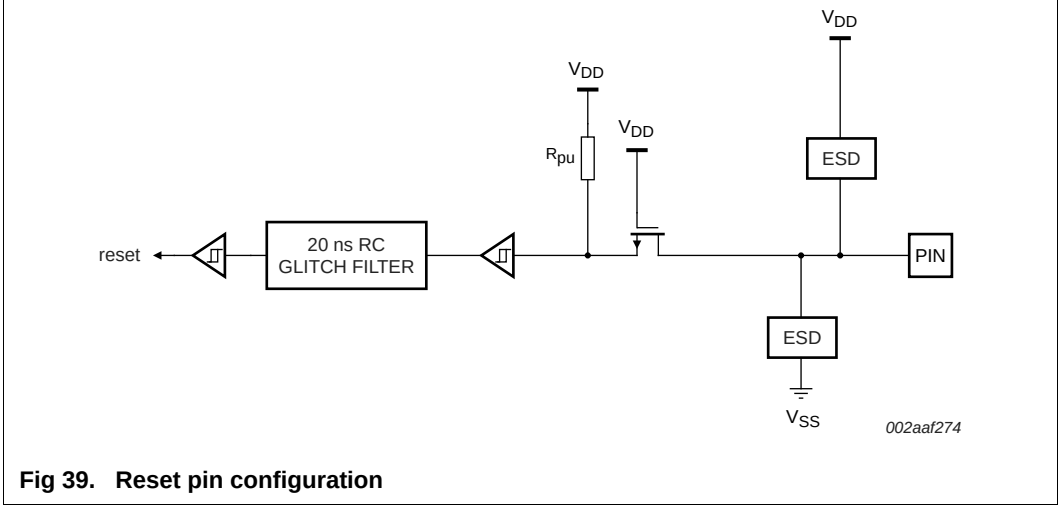
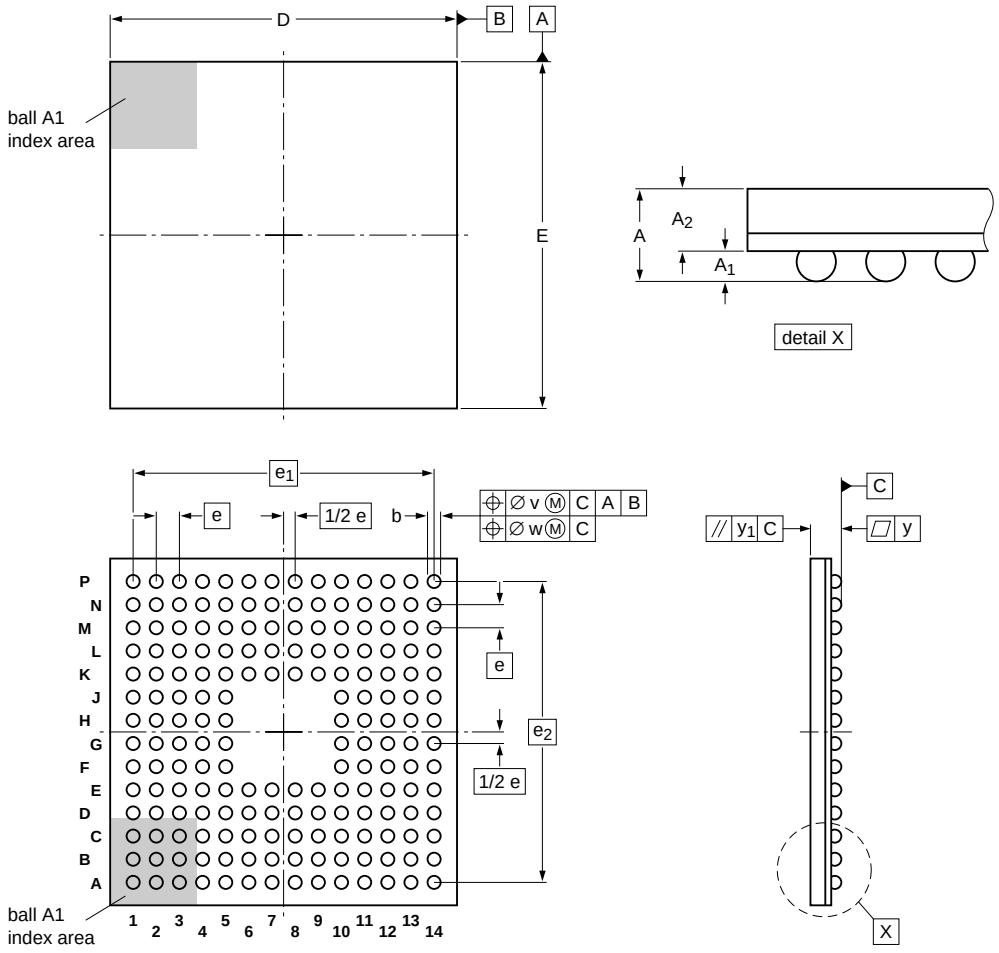


Fig 39. Reset pin configuration

14.6 Reset pin configuration for RTC operation

Under certain circumstances, the RTC may temporarily pause and lose fractions of a second during the rising and falling edges of the RESET signal.

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 43. TFBGA180 package

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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