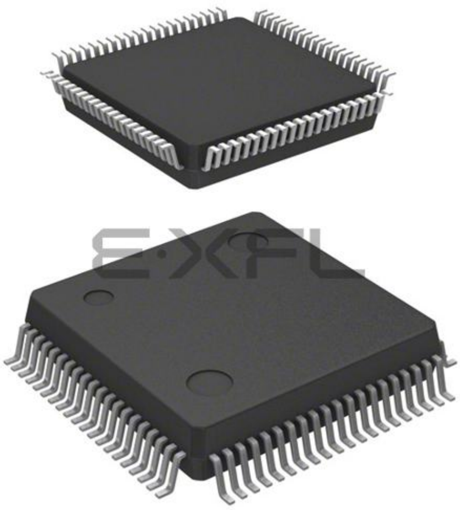

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	55
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38324hwv

1.3 Pin Arrangement and Functions

1.3.1 Pin Arrangement

The pin arrangements of the H8/3827R Group, H8/3827S Group, H8/38327 Group, and H8/38427 Group are shown in figures 1.2 and 1.3 (figure 1.3 only applies to the H8/3827R Group). The bonding pad location diagram of the H8/3827R Group (mask ROM version) is shown in figure 1.4, and the bonding pad coordinates are given in table 1.2. The bonding pad location diagram of the H8/3827S Group (mask ROM version) is shown in figure 1.5, and the bonding pad coordinates are given in table 1.3. The bonding pad location diagram of the HCD64F38327 and HCD64F38427 is shown in figure 1.6, and the bonding pad coordinates are given in table 1.4. The bonding pad location diagram of the H8/38327 Group (mask ROM version) and H8/38427 Group (mask ROM version) is shown in figure 1.7, and the bonding pad coordinates are given in table 1.5.

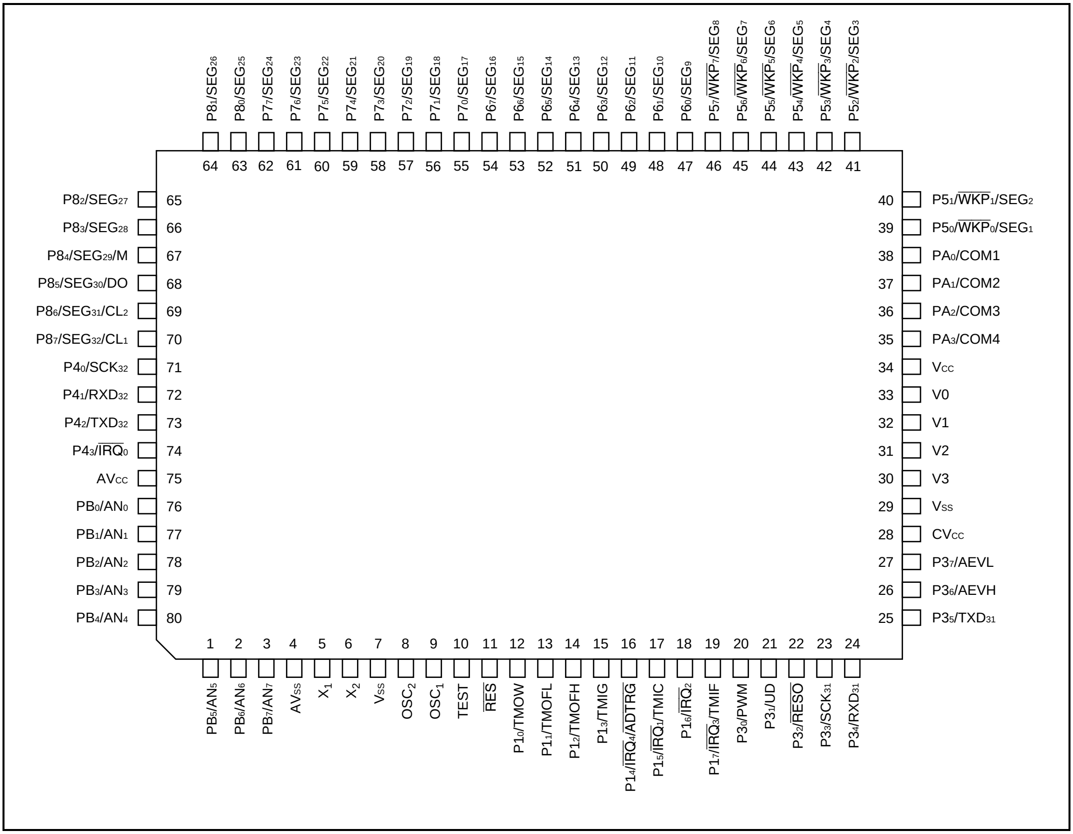


Figure 1.3 Pin Arrangement (FP-80B: Top View)

2.3.1 Data Formats in General Registers

Data of all the sizes above can be stored in general registers as shown in figure 2.3.

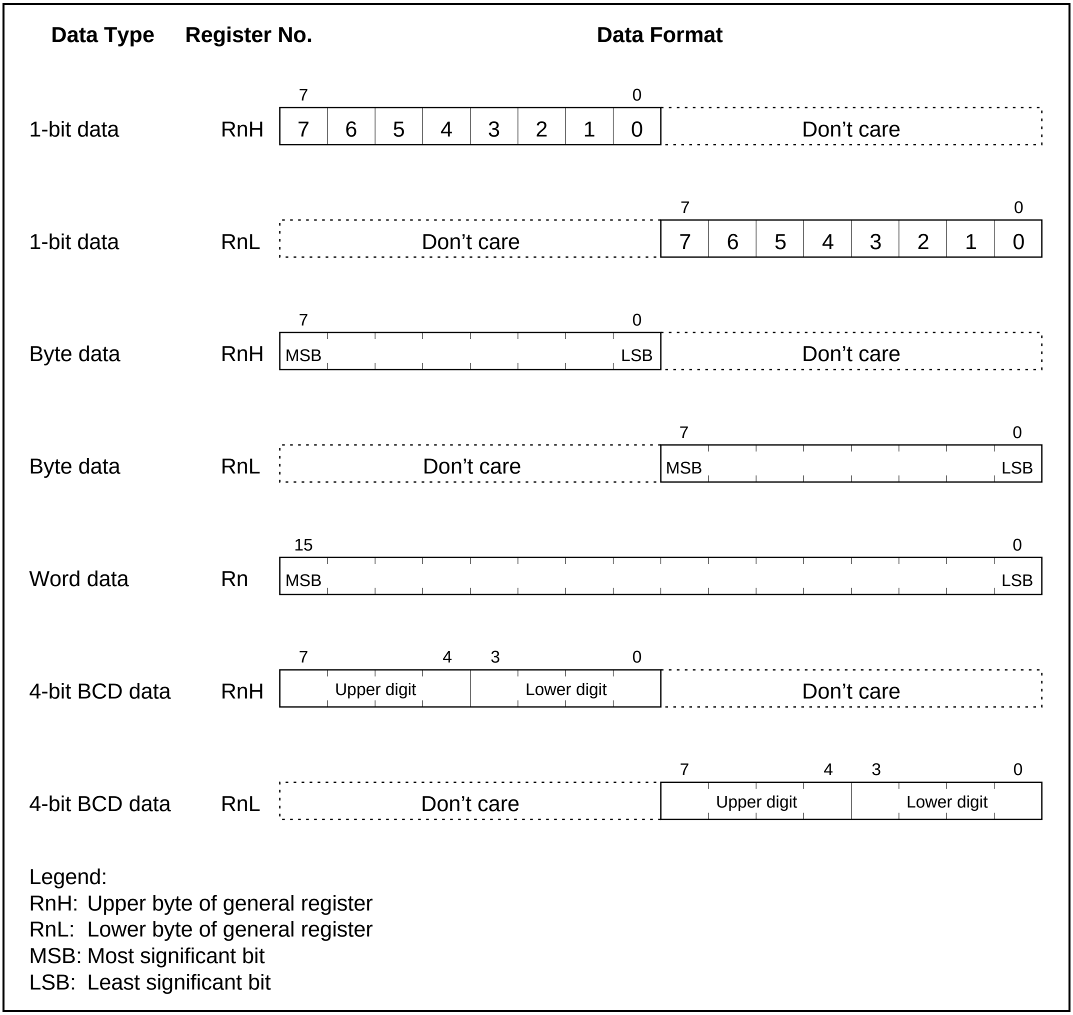
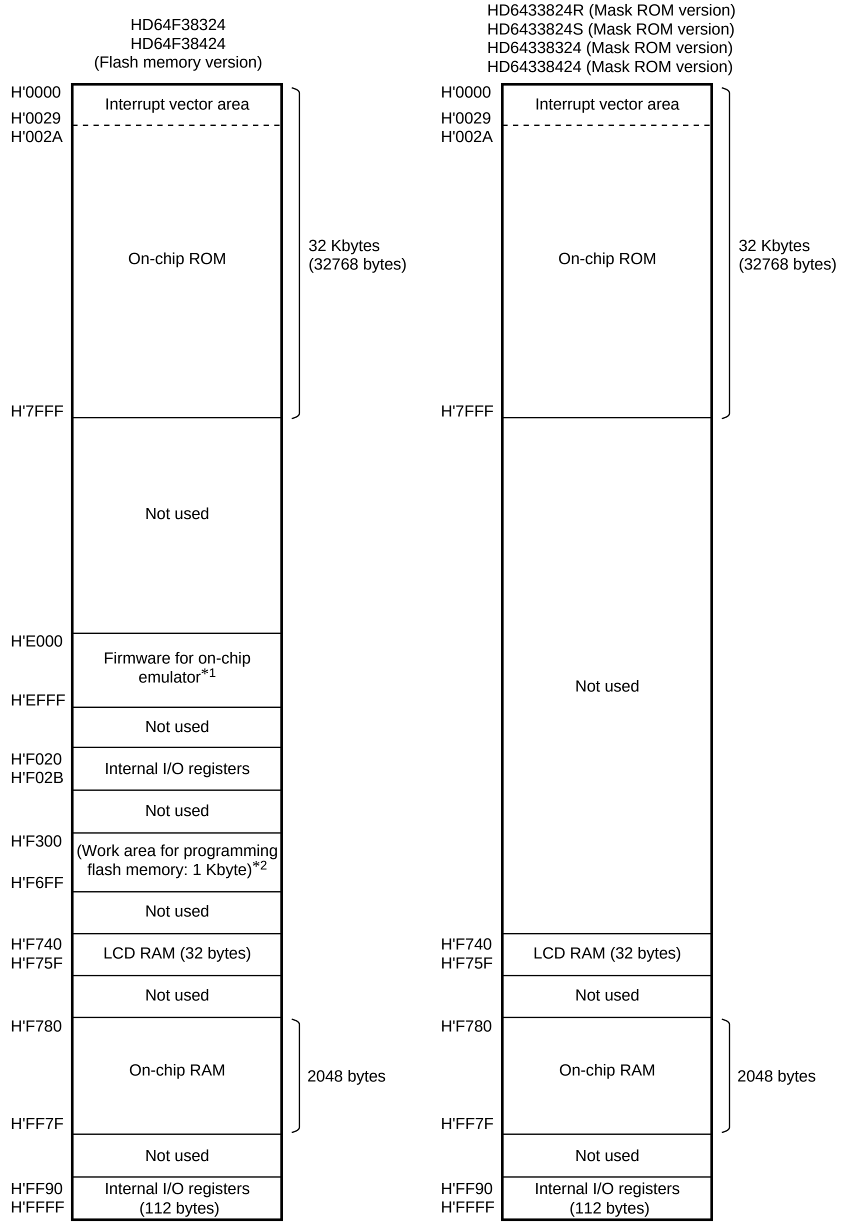


Figure 2.3 Register Data Formats



Notes: 1. Not accessible by the user when the on-chip emulator is used.
2. A programming control program is used to program flash memory. Do not use a user program to perform programming when the on-chip emulator is used. This area is not used in the mask ROM version.

Figure 2.16 (3) H8/3824R, H8/3824S, H8/38324, and H8/38424 Memory Map

Bits 1 and 0: Active (medium-speed) mode clock select (MA1, MA0)

Bits 1 and 0 choose $\phi_{OSC}/128$, $\phi_{OSC}/64$, $\phi_{OSC}/32$, or $\phi_{OSC}/16$ as the operating clock in active (medium-speed) mode and sleep (medium-speed) mode. MA1 and MA0 should be written in active (high-speed) mode or subactive mode.

Bit 1 MA1	Bit 0 MA0	Description	
0	0	$\phi_{OSC}/16$	
0	1	$\phi_{OSC}/32$	
1	0	$\phi_{OSC}/64$	
1	1	$\phi_{OSC}/128$	(initial value)

2. System Control Register 2 (SYSCR2)

Bit	7	6	5	4	3	2	1	0
	—	—	—	NESEL	DTON	MSON	SA1	SA0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

SYSCR2 is an 8-bit read/write register for power-down mode control.

Bits 7 to 5: Reserved bits

These bits are reserved; they are always read as 1, and cannot be modified.

Bit 4: Noise elimination sampling frequency select (NESEL)

This bit selects the frequency at which the watch clock signal (ϕ_W) generated by the subclock pulse generator is sampled, in relation to the oscillator clock (ϕ_{OSC}) generated by the system clock pulse generator. When ϕ_{OSC} = 2 to 16 MHz, clear NESEL to 0.

Bit 4 NESEL	Description	
0	Sampling rate is $\phi_{OSC}/16$	
1	Sampling rate is $\phi_{OSC}/4$	(initial value)

2. Time for Direct Transition from Active (Medium-Speed) Mode to Active (High-Speed) Mode

A direct transition from active (medium-speed) mode to active (high-speed) mode is performed by executing a SLEEP instruction in active (medium-speed) mode while bits SSBY and LSON are both cleared to 0 in SYSCR1, and bit MSON is cleared to 0 and bit DTON is set to 1 in SYSCR2. The time from execution of the SLEEP instruction to the end of interrupt exception handling (the direct transition time) is given by equation (2) below.

Direct transition time = { (Number of SLEEP instruction execution states) + (number of internal processing states) } × (tcyc before transition) + (number of interrupt exception handling execution states) × (tcyc after transition) .... (2)

Example: Direct transition time = (2 + 1) × 16tosc + 14 × 2tosc = 76tosc (when φ/8 is selected as the CPU operating clock)

Notation:
tosc: OSC clock cycle time
tcyc: System clock (φ) cycle time

3. Time for Direct Transition from Subactive Mode to Active (High-Speed) Mode

A direct transition from subactive mode to active (high-speed) mode is performed by executing a SLEEP instruction in subactive mode while bit SSBY is set to 1 and bit LSON is cleared to 0 in SYSCR1, bit MSON is cleared to 0 and bit DTON is set to 1 in SYSCR2, and bit TMA3 is set to 1 in TMA. The time from execution of the SLEEP instruction to the end of interrupt exception handling (the direct transition time) is given by equation (3) below.

Direct transition time = { (Number of SLEEP instruction execution states) + (number of internal processing states) } × (tsubcyc before transition) + { (wait time set in STS2 to STS0) + (number of interrupt exception handling execution states) } × (tcyc after transition) .... (3)

Example: Direct transition time = (2 + 1) × 8tw + (8192 + 14) × 2tosc = 24tw + 16412tosc (when φw/8 is selected as the CPU operating clock, and wait time = 8192 states)

Notation:
tosc: OSC clock cycle time
tw: Watch clock cycle time
tcyc: System clock (φ) cycle time
tsubcyc: Subclock (ϕ_{SUB}) cycle time

H8/3827R			EPROM socket	
FP-80A, TFP-80C	FP-80B	Pin	Pin	HN27C101 (32-pin)
9	11	RES	V_{PP}	1
45	47	$P6_0$	EO_0	13
46	48	$P6_1$	EO_1	14
47	49	$P6_2$	EO_2	15
48	50	$P6_3$	EO_3	17
49	51	$P6_4$	EO_4	18
50	52	$P6_5$	EO_5	19
51	53	$P6_6$	EO_6	20
52	54	$P6_7$	EO_7	21
68	70	$P8_7$	EA_0	12
67	69	$P8_6$	EA_1	11
66	68	$P8_5$	EA_2	10
65	67	$P8_4$	EA_3	9
64	66	$P8_3$	EA_4	8
63	65	$P8_2$	EA_5	7
62	64	$P8_1$	EA_6	6
61	63	$P8_0$	EA_7	5
53	55	$P7_0$	EA_8	27
72	74	$P4_3$	EA_9	26
55	57	$P7_2$	EA_{10}	23
56	58	$P7_3$	EA_{11}	25
57	59	$P7_4$	EA_{12}	4
58	60	$P7_5$	EA_{13}	28
59	61	$P7_6$	EA_{14}	29
14	16	$P1_4$	EA_{15}	3
15	17	$P1_5$	EA_{16}	2
60	62	$P7_7$	$\overline{CE}$	22
54	56	$P7_1$	$\overline{OE}$	24
13	15	$P1_3$	$\overline{PGM}$	31
32, 26	34, 28	V_{CC}, CV_{CC}	V_{CC}	32
73	75	AV_{CC}		
8	10	TEST		
3	5	X_1		
80	2	PB_6		
11	13	$P1_1$		
12	14	$P1_2$		
16	18	$P1_6$		
5, 27	7, 29	V_{SS}	V_{SS}	16
2	4	AV_{SS}		
78	80	PB_4		
79	1	PB_5		

Note: Pins not indicated in the figure should be left open.

Figure 6.2 Socket Adapter Pin Correspondence (with HN27C101)

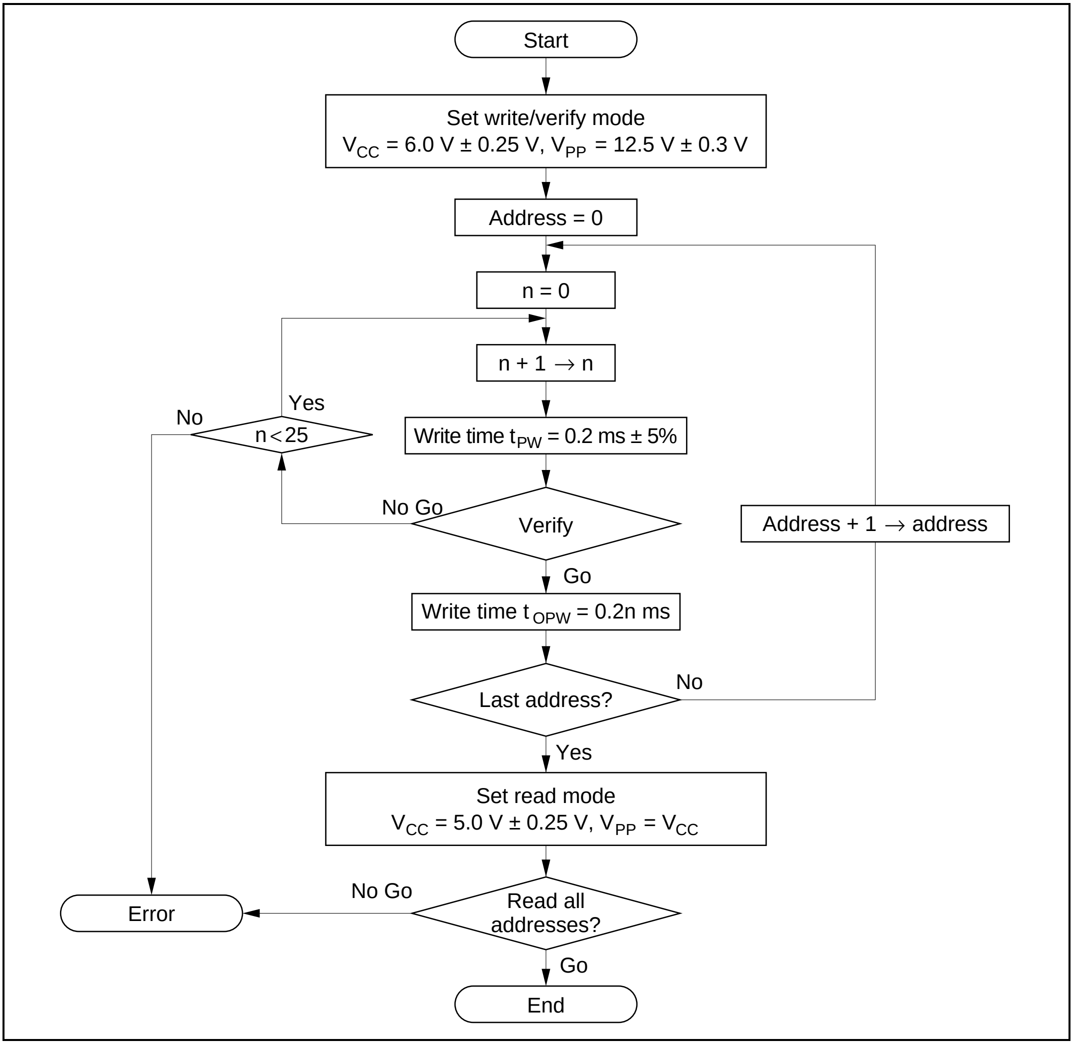


Figure 6.4 High-Speed, High-Reliability Programming Flow Chart

3. Port Pull-Up Control Register 3 (PUCR3)

Bit	7	6	5	4	3	2	1	0
	$PUCR3_7$	$PUCR3_6$	$PUCR3_5$	$PUCR3_4$	$PUCR3_3$	$PUCR3_2$	$PUCR3_1$	$PUCR3_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PUCR3 controls whether the MOS pull-up of each of the port 3 pins $P3_7$ to $P3_0$ is on or off. When a PCR3 bit is cleared to 0, setting the corresponding PUCR3 bit to 1 turns on the MOS pull-up for the corresponding pin, while clearing the bit to 0 turns off the MOS pull-up.

Upon reset, PUCR3 is initialized to H'00.

4. Port Mode Register 3 (PMR3)

Bit	7	6	5	4	3	2	1	0
	AEVL	AEVH	WDCKS	NCS	IRQ0	RESO*	UD	PWM
Initial value	0	0	0	0	0	1	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: * The RESO bit is not implemented in the H8/38327 Group and H8/38427 Group.

PMR3 is an 8-bit read/write register, controlling the selection of pin functions for port 3 pins.

Upon reset, PMR3 is initialized to H'04.

Bit 7: $P3_7$/AEVL pin function switch (AEVL)

This bit selects whether pin $P3_7$/AEVL is used as $P3_7$ or as AEVL.

Bit 7 AEVL	Description	
0	Functions as $P3_7$ I/O pin	(initial value)
1	Functions as AEVL input pin	

RENESAS

2. Timer Counter C (TCC)

Bit	7	6	5	4	3	2	1	0
	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

TCC is an 8-bit read-only up-counter, which is incremented by internal clock or external event input. The clock source for input to this counter is selected by bits TMC2 to TMC0 in timer mode register C (TMC). TCC values can be read by the CPU at any time.

When TCC overflows from H'FF to H'00 or to the value set in TLC, or underflows from H'00 to H'FF or to the value set in TLC, the IRRTC bit in IRR2 is set to 1.

TCC is allocated to the same address as TLC.

Upon reset, TCC is initialized to H'00.

3. Timer Load Register C (TLC)

Bit	7	6	5	4	3	2	1	0
	TLC7	TLC6	TLC5	TLC4	TLC3	TLC2	TLC1	TLC0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

TLC is an 8-bit write-only register for setting the reload value of timer counter C (TCC).

When a reload value is set in TLC, the same value is loaded into timer counter C as well, and TCC starts counting up from that value. When TCC overflows or underflows during operation in auto-reload mode, the TLC value is loaded into TCC. Accordingly, overflow/underflow periods can be set within the range of 1 to 256 input clocks.

The same address is allocated to TLC as to TCC.

Upon reset, TLC is initialized to H'00.

2. Block Diagram

Figure 9.3 shows a block diagram of timer F.

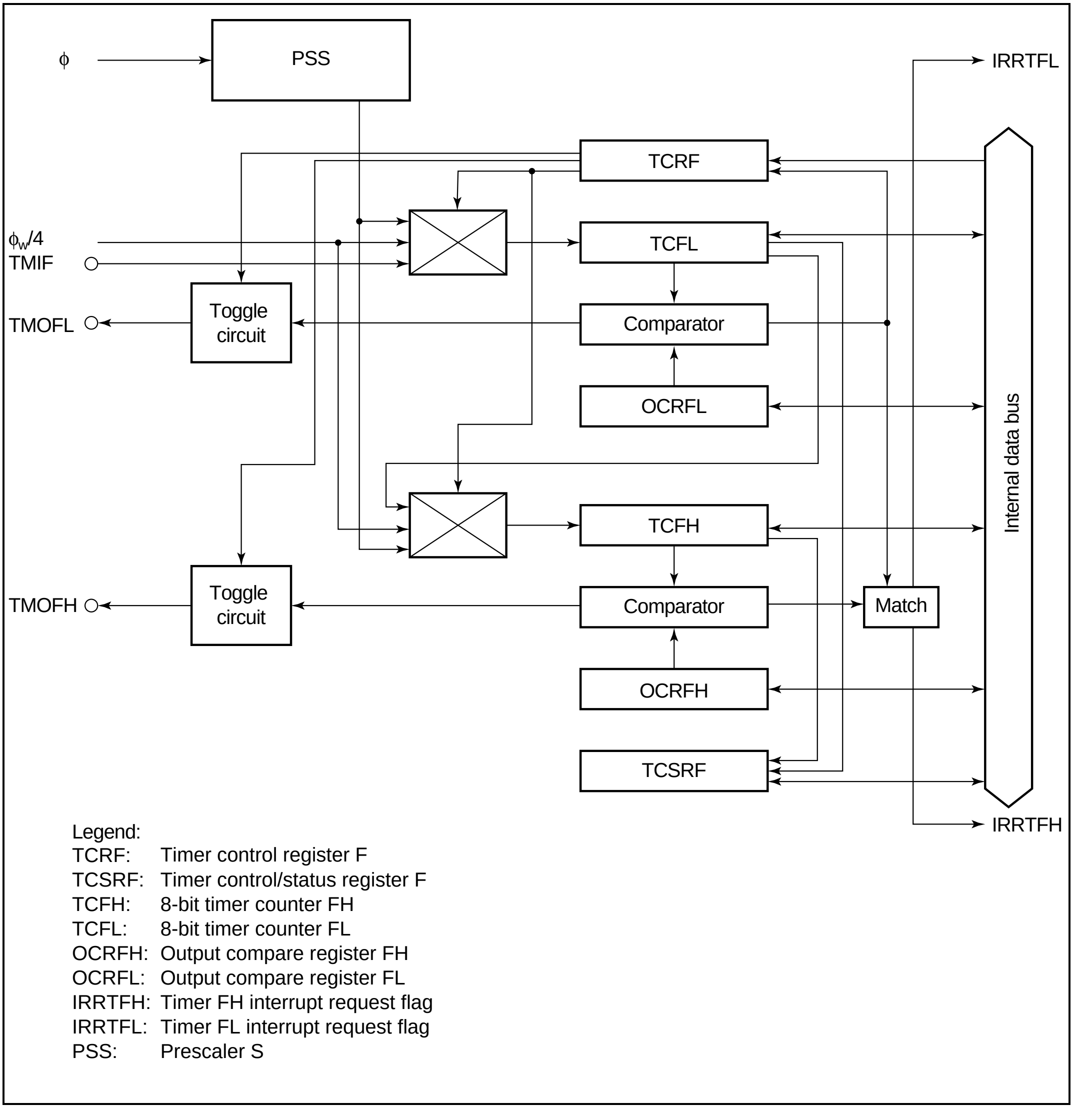


Figure 9.3 Block Diagram of Timer F

Bit 7: Counter overflow flag H (OVH)

Bit 7 is a status flag indicating that ECH has overflowed from H'FF to H'00. This flag is set when ECH overflows. It is cleared by software but cannot be set by software. OVH is cleared by reading it when set to 1, then writing 0.

When ECH and ECL are used as a 16-bit event counter with CH2 cleared to 0, OVH functions as a status flag indicating that the 16-bit event counter has overflowed from H'FFFF to H'0000.

Bit 7 OVH	Description	
0	ECH has not overflowed Clearing condition: After reading OVH = 1, cleared by writing 0 to OVH	(initial value)
1	ECH has overflowed Setting condition: Set when ECH overflows from H’FF to H’00	

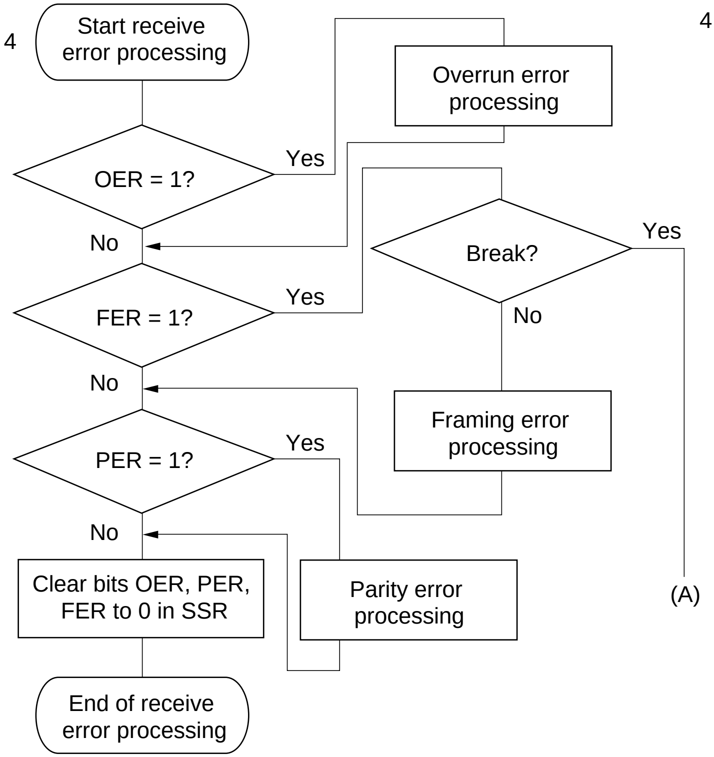
Bit 6: Counter overflow flag L (OVL)

Bit 6 is a status flag indicating that ECL has overflowed from H'FF to H'00. This flag is set when ECL overflows. It is cleared by software but cannot be set by software. OVL is cleared by reading it when set to 1, then writing 0.

Bit 6 OVL	Description	
0	ECL has not overflowed Clearing condition: After reading OVL = 1, cleared by writing 0 to OVL	(initial value)
1	ECL has overflowed Setting condition: Set when ECL overflows from H'FF to H'00 while CH2 is set to 1	

Bit 5: Reserved bit

Bit 5 is reserved; it can be read and written, and is initialized to 0 upon reset.



4. If a receive error has occurred, read bits OER, PER, and FER in SSR to identify the error, and after carrying out the necessary error processing, ensure that bits OER, PER, and FER are all cleared to 0. Reception cannot be resumed if any of these bits is set to 1. In the case of a framing error, a break can be detected by reading the value of the RXD_{3x} pin.

Figure 10.8 Example of Data Reception Flowchart (Asynchronous Mode) (cont)

Bit 4: Display data control (DISP)

Bit 4 specifies whether the LCD RAM contents are displayed or blank data is displayed regardless of the LCD RAM contents.

Bit 4 DISP	Description	
0	Blank data is displayed	(initial value)
1	LCD RAM data is display	

Bits 3 to 0: Frame frequency select 3 to 0 (CKS3 to CKS0)

Bits 3 to 0 select the operating clock and the frame frequency. In subactive mode, watch mode, and subsleep mode, the system clock (ϕ) is halted, and therefore display operations are not performed if one of the clocks from ϕ/2 to ϕ/256 is selected. If LCD display is required in these modes, ϕw, ϕw/2, or ϕw/4 must be selected as the operating clock.

Bit 3	Bit 2	Bit 1	Bit 0		Frame Frequency*2	
CKS3	CKS2	CKS1	CKS0	Operating Clock	ϕ = 2 MHz	ϕ = 250 kHz*1
0	*	0	0	ϕw	128 Hz*3 (initial value)	
0	*	0	1	ϕw/2	64 Hz*3	
0	*	1	*	ϕw/4	32 Hz*3	
1	0	0	0	ϕ/2	—	244 Hz
1	0	0	1	ϕ/4	977 Hz	122 Hz
1	0	1	0	ϕ/8	488 Hz	61 Hz
1	0	1	1	ϕ/16	244 Hz	30.5 Hz
1	1	0	0	ϕ/32	122 Hz	—
1	1	0	1	ϕ/64	61 Hz	—
1	1	1	0	ϕ/128	30.5 Hz	—
1	1	1	1	ϕ/256	—	—

*: Don’t care

Notes: 1. This is the frame frequency in active (medium-speed, ϕosc/16) mode when ϕ = 2 MHz.
2. When 1/3 duty is selected, the frame frequency is 4/3 times the value shown.
3. This is the frame frequency when ϕw = 32.768 kHz.

13.3.2 Relationship between LCD RAM and Display

The relationship between the LCD RAM and the display segments differs according to the duty cycle. LCD RAM maps for the different duty cycles when segment external expansion is not used are shown in figures 13.5 to 13.8, and LCD RAM maps when segment external expansion is used in figures 13.9 to 13.12.

After setting the registers required for display, data is written to the part corresponding to the duty using the same kind of instruction as for ordinary RAM, and display is started automatically when turned on. Word- or byte-access instructions can be used for RAM setting.

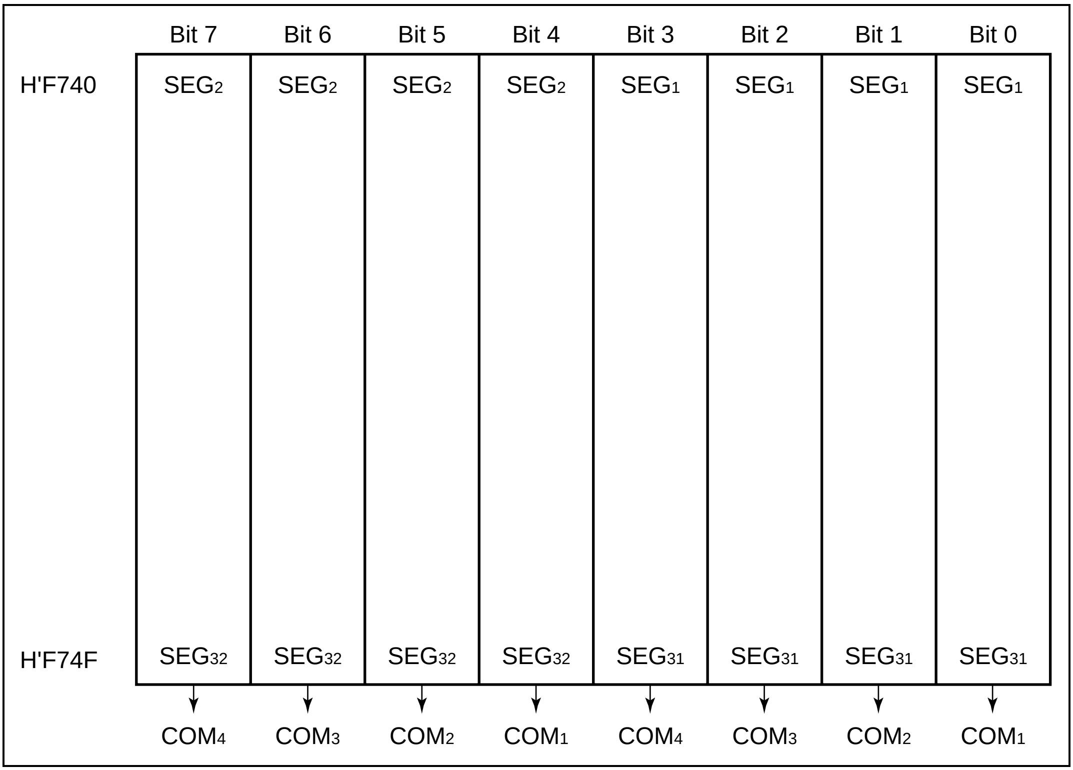


Figure 13.5 LCD RAM Map when Not Using Segment External Expansion (1/4 Duty)

15.2.5 LCD Characteristics

Table 15.6 shows the LCD characteristics.

Table 15.6 LCD Characteristics

V_{CC} = 1.8 V to 5.5 V, AV_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C*3 (including subactive mode) unless otherwise specified.

Item	Symbol	Applicable Pins	Test Conditions	Values Min	Typ	Max	Unit	Notes
Segment driver drop voltage	V_{DS}	SEG_1 to SEG_{32}	I_D = 2 μA V_1 = 2.7 to 5.5 V	—	—	0.6	V	*1
Common driver drop voltage	V_{DC}	COM_1 to COM_4	I_D = 2 μA V_1 = 2.7 to 5.5 V	—	—	0.3	V	*1
LCD power supply split-resistance	R_{LCD}		Between V_1 and V_{SS}	0.5	3.0	9.0	MΩ	
Liquid crystal display voltage	V_{LCD}	V_1		2.2	—	5.5	V	*2

Notes: 1. The voltage drop from power supply pins V_1, V_2, V_3, and V_{SS} to each segment pin or common pin.

2. When the liquid crystal display voltage is supplied from an external power source, ensure that the following relationship is maintained: $V_1 \geq V_2 \geq V_3 \geq V_{SS}$.

3. The guaranteed temperature as an electrical characteristic for Die products is 75°C.

Item	Symbol	Applicable Pins	Values			Unit	Test Condition	Notes
			Min	Typ	Max			
Output low voltage	V_{OL}	$P1_0$ to $P1_7$, $P4_0$ to $P4_2$	—	—	0.6	V	V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
		$P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	—	—	0.5		I_{OL} = 0.4 mA	
		$P3_0$ to $P3_7$	—	—	1.5		V_{CC} = 4.0 V to 5.5 V I_{OL} = 10 mA	
			—	—	0.6		V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
Input/output leakage current	$\| I_{IL} \|$	$\overline{RES}$, $P4_3$	—	—	20.0	μA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	*2
			—	—	1.0			*1
		OSC_1, X_1, $P1_0$ to $P1_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	—	—	1.0	μA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7	—	—	1.0		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	
Pull-up MOS current	$-I_p$	$P1_0$ to $P1_7$, $P3_0$ to $P3_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$	50.0	—	300.0	μA	V_{CC} = 5 V, V_{IN} = 0 V	
			—	35.0	—		V_{CC} = 2.7 V, V_{IN} = 0 V	Reference value

SSR31—Serial Status Register31 H'9C SCI3

Bit	7	6	5	4	3	2	1	0
	TDRE31	RDRF31	OER31	FER31	PER31	TEND31	MPBR31	MPBT31
Initial value	1	0	0	0	0	1	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/W

Multiprocessor bit transfer

0	A 0 multiprocessor bit is transmitted
1	A 1 multiprocessor bit is transmitted

Multiprocessor bit receive

0	Data in which the multiprocessor bit is 0 has been received
1	Data in which the multiprocessor bit is 1 has been received

Transmit end

0	Transmission in progress [Clearing conditions] • After reading TDRE31 = 1, cleared by writing 0 to TDRE • When data is written to TDR31 by an instruction
1	Transmission ended [Setting conditions] • When bit TE in serial control register 31 (SCR31) is cleared to 0 • When bit TDRE31 is set to 1 when the last bit of a transmit character is sent

Parity error

0	Reception in progress or completed normally [Clearing condition] After reading PER31 = 1, cleared by writing 0 to PER31
1	A parity error has occurred during reception [Setting condition] When the number of 1 bits in the receive data plus parity bit does not match the parity designated by the parity mode bit (PM31) in the serial mode register (SMR31)

Framing error

0	Reception in progress or completed normally [Clearing condition] After reading FER31 = 1, cleared by writing 0 to FER31
1	A framing error has occurred during reception [Setting condition] When the stop bit at the end of the receive data is checked for a value of 1 at completion of reception, and the stop bit is 0

Overrun error

0	Reception in progress or completed [Clearing condition] After reading OER31 = 1, cleared by writing 0 to OER31
1	An overrun error has occurred during reception [Setting condition] When the next serial reception is completed with RDRF31 set to 1

Receive data register full

0	There is no receive data in RDR31 [Clearing conditions] • After reading RDRF31 = 1, cleared by writing 0 to RDRF31 • When RDR31 data is read by an instruction
1	There is receive data in RDR31 [Setting condition] When reception ends normally and receive data is transferred from RSR31 to RDR31

Transmit data register empty

0	Transmit data written in TDR31 has not been transferred to TSR31 [Clearing conditions] • After reading TDRE31 = 1, cleared by writing 0 to TDRE31 • When data is written to TDR31 by an instruction
1	Transmit data has not been written to TDR31, or transmit data written in TDR31 has been transferred to TSR31 [Setting conditions] • When bit TE in serial control register 31 (SCR31) is cleared to 0 • When data is transferred from TDR31 to TSR31

Note: * Only a write of 0 for flag clearing is possible.

SMR32—Serial Mode Register 32 **H'A8** **SCI32**

Bit	7	6	5	4	3	2	1	0
	COM32	CHR32	PE32	PM32	STOP32	MP32	CKS321	CKS320
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Clock select (bits 1–0)

0	0	φ clock
0	1	φw/2 clock
1	0	φ/16 clock
1	1	φ/64 clock

Multiprocessor mode (bit 2)

0	Multiprocessor communication function disabled
1	Multiprocessor communication function enabled

Stop bit length (bit 3)

0	1 stop bit
1	2 stop bits

Parity mode (bit 4)

0	Even parity
1	Odd parity

Parity enable (bit 5)

0	Parity bit addition and checking disabled
1	Parity bit addition and checking enabled

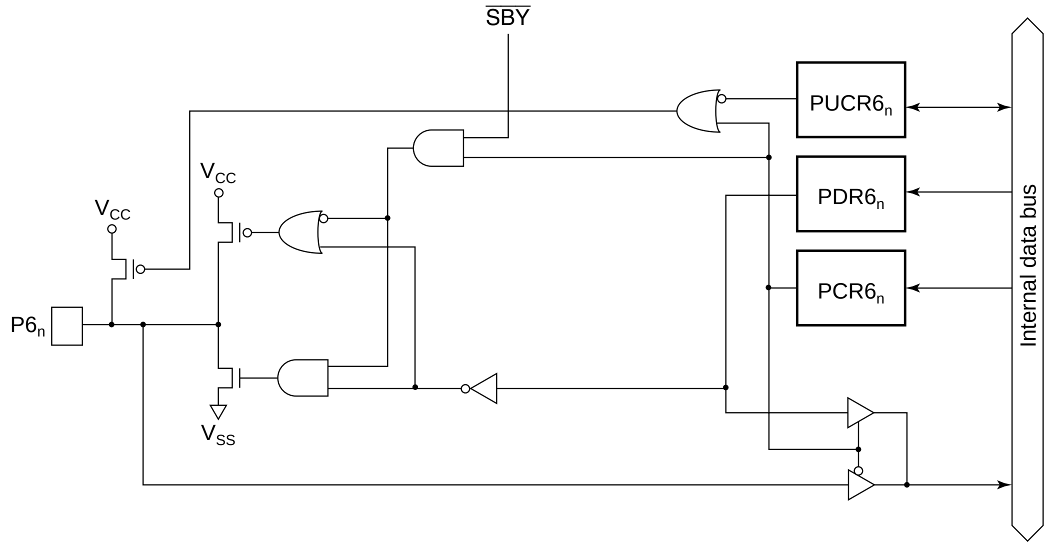
Character length (bit 6)

0	8-bit data/5-bit data
1	7-bit data/5-bit data

Communication mode (bit 7)

0	Asynchronous mode
1	Synchronous mode

C.5 Block Diagram of Port 6



PDR6: Port data register 6
PCR6: Port control register 6
PUCR6: Port pull-up control register 6
n = 7 to 0

Figure C.5 Port 6 Block Diagram