Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	55
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38324wwv

Section 9 Timers

1.2 Internal Block Diagram

Figure 1.1(1) shows a block diagram of the H8/3827R Group and H8/3827S Group.

Figure 1.1(2) shows a block diagram of the H8/38327 Group and H8/38427 Group.

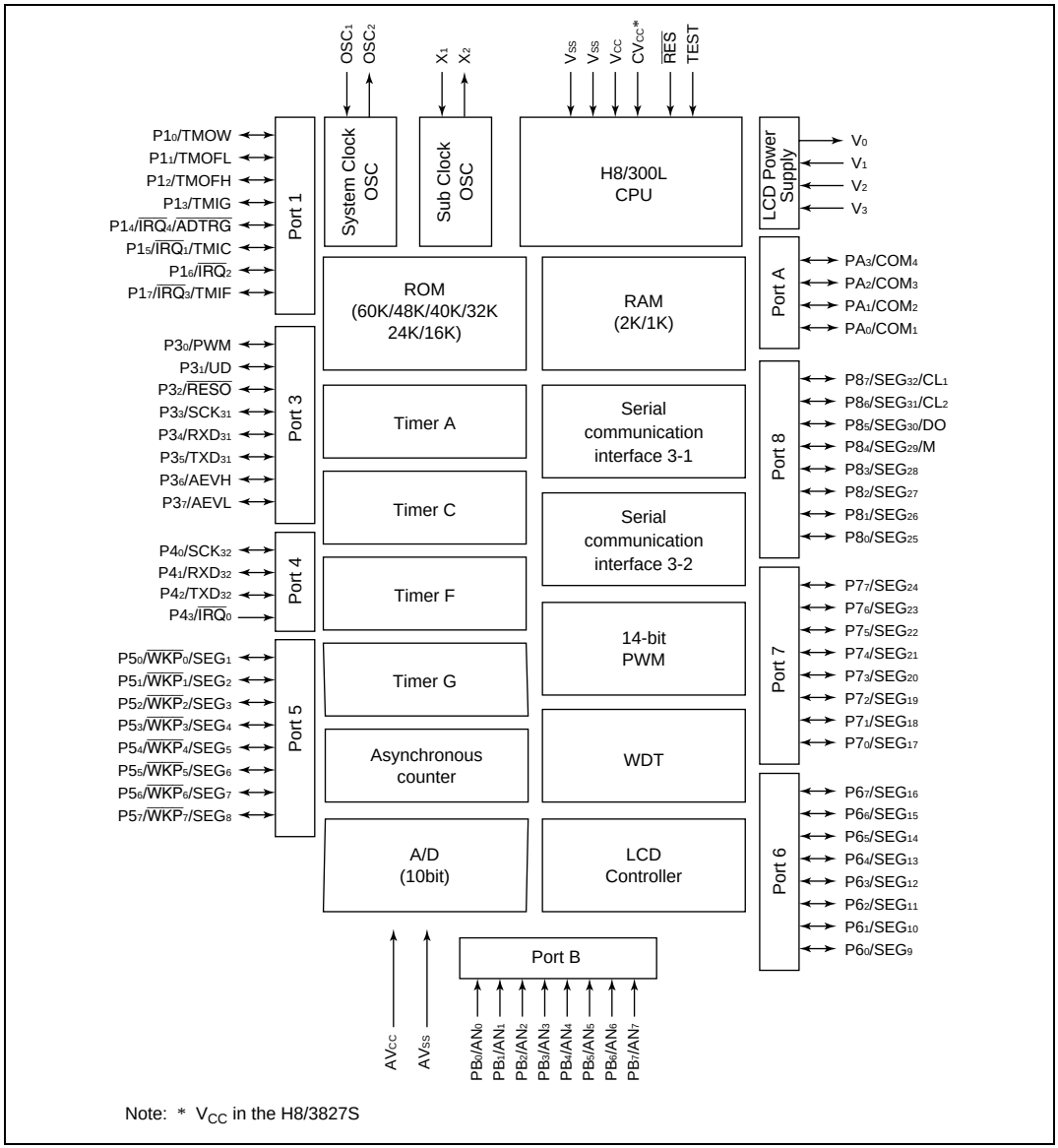


Figure 1.1(1) Block Diagram (H8/3827R Group and H8/3827S Group)

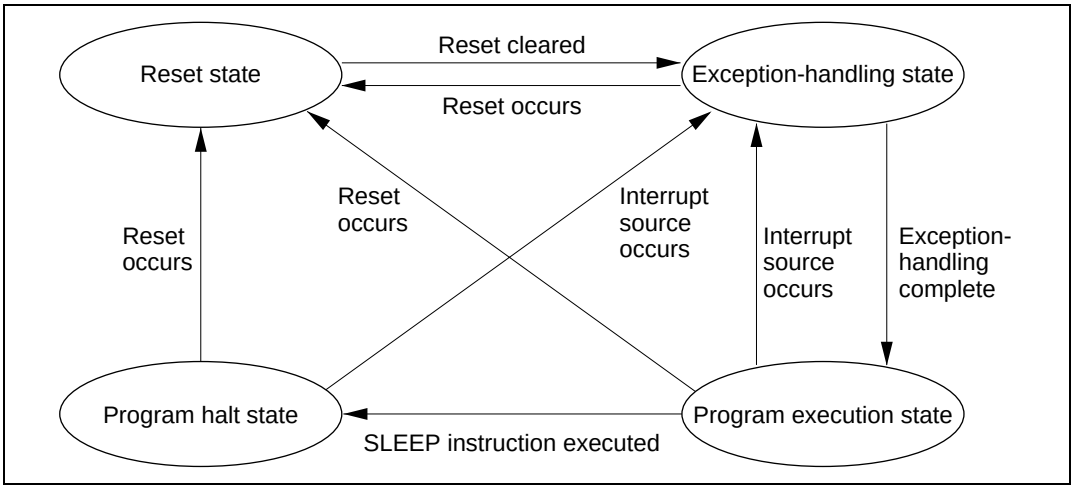


Figure 2.15 State Transitions

2.7.2 Program Execution State

In the program execution state the CPU executes program instructions in sequence.

There are three modes in this state, two active modes (high speed and medium speed) and one subactive mode. Operation is synchronized with the system clock in active mode (high speed and medium speed), and with the subclock in subactive mode. See section 5, Power-Down Modes for details on these modes.

2.7.3 Program Halt State

In the program halt state there are five modes: two sleep modes (high speed and medium speed), standby mode, watch mode, and subsleep mode. See section 5, Power-Down Modes for details on these modes.

2.7.4 Exception-Handling State

The exception-handling state is a transient state occurring when exception handling is started by a reset or interrupt and the CPU changes its normal processing flow. In exception handling caused by an interrupt, SP (R7) is referenced and the PC and CCR values are saved on the stack.

For details on interrupt handling, see section 3.3, Interrupts.

2. Interrupts IRQ_4 to IRQ_0

Interrupts IRQ_4 to IRQ_0 are requested by input signals to pins $\overline{IRQ_4}$ to $\overline{IRQ_0}$. These interrupts are detected by either rising edge sensing or falling edge sensing, depending on the settings of bits IEG4 to IEG0 in IEGR.

When these pins are designated as pins $\overline{IRQ_4}$ to $\overline{IRQ_0}$ in port mode register 3 and 1 and the designated edge is input, the corresponding bit in IRR1 is set to 1, requesting an interrupt. Recognition of these interrupt requests can be disabled individually by clearing bits IEN4 to IEN0 to 0 in IENR1. These interrupts can all be masked by setting the I bit to 1 in CCR.

When IRQ_4 to IRQ_0 interrupt exception handling is initiated, the I bit is set to 1 in CCR. Vector numbers 8 to 4 are assigned to interrupts IRQ_4 to IRQ_0. The order of priority is from IRQ_0 (high) to IRQ_4 (low). Table 3.2 gives details.

3.3.4 Internal Interrupts

There are 23 internal interrupts that can be requested by the on-chip peripheral modules. When a peripheral module requests an interrupt, the corresponding bit in IRR1 or IRR2 is set to 1. Recognition of individual interrupt requests can be disabled by clearing the corresponding bit in IENR1 or IENR2. All these interrupts can be masked by setting the I bit to 1 in CCR. When internal interrupt handling is initiated, the I bit is set to 1 in CCR. Vector numbers from 20 to 11 are assigned to these interrupts. Table 3.2 shows the order of priority of interrupts from on-chip peripheral modules.

5.4.4 Notes on External Input Signal Changes before/after Watch Mode

See section 5.3.5, Notes on External Input Signal Changes before/after Standby Mode.

5.5 Subsleep Mode

5.5.1 Transition to Subsleep Mode

The system goes from subactive mode to subsleep mode when a SLEEP instruction is executed while the SSBY bit in SYSCR1 is cleared to 0, LSON bit in SYSCR1 is set to 1, and TMA3 bit in TMA is set to 1. In subsleep mode, operation of on-chip peripheral modules other than the A/D converter WDT and PWM is halted. As long as a minimum required voltage is applied, the contents of CPU registers, the on-chip RAM and some registers of the on-chip peripheral modules are retained. I/O ports keep the same states as before the transition.

5.5.2 Clearing Subsleep Mode

Subsleep mode is cleared by an interrupt (timer A, timer C, timer F, timer G, asynchronous counter, SCI3-2, SCI3-1, IRQ_4 to IRQ_0, WKP_7 to WKP_0) or by a low input at the $\overline{RES}$ pin.

- Clearing by interrupt

  When an interrupt is requested, subsleep mode is cleared and interrupt exception handling starts. Subsleep mode is not cleared if the I bit of CCR is set to 1 or the particular interrupt is disabled in the interrupt enable register.

  Interrupt signal and system clock are mutually asynchronous. Synchronization error time in a maximum is $2/\phi_{SUB}$ (s).

- Clearing by $\overline{RES}$ input

  Clearing by $\overline{RES}$ pin is the same as for standby mode; see 2. Clearing by $\overline{RES}$ pin in section 5.3.2, Clearing Standby Mode.

6.7 On-Board Programming Modes

There are two modes for programming/erasing of the flash memory; boot mode, which enables on-board programming/erasing, and programmer mode, in which programming/erasing is performed with a PROM programmer. On-board programming/erasing can also be performed in user program mode. At reset-start in reset mode, this LSI changes to a mode depending on the TEST pin settings, P32 pin settings, and input level of each port, as shown in table 6.8. The input level of each pin must be defined four states before the reset ends.

When changing to boot mode, the boot program built into this LSI is initiated. The boot program transfers the programming control program from the externally-connected host to on-chip RAM via SCI32. After erasing the entire flash memory, the programming control program is executed. This can be used for programming initial values in the on-board state or for a forcible return when programming/erasing can no longer be done in user program mode. In user program mode, individual blocks can be erased and programmed by branching to the user program/erase control program prepared by the user.

Table 6.8 Setting Programming Modes

TEST	P32	P86	PB0	PB1	PB2	LSI State after Reset End
0	1	X	X	X	X	User Mode
0	0	1	X	X	X	Boot Mode
1	X	X	0	0	0	Programmer Mode

X: Don't care

6.7.1 Boot Mode

Table 6.9 shows the boot mode operations between reset end and branching to the programming control program. The device uses SCI32 in the boot mode.

1. When boot mode is used, the flash memory programming control program must be prepared in the host beforehand. Prepare a programming control program in accordance with the description in section 6.8, Flash Memory Programming/Erasing.
2. SCI3 should be set to asynchronous mode, and the transfer format as follows: 8-bit data, 1 stop bit, and no parity. The inversion function of TXD and RXD pins by the SPCR register is set to "Not to be inverted," so do not put the circuit for inverting a value between the host and this LSI.
3. When the boot program is initiated, the chip measures the low-level period of asynchronous SCI communication data (H'00) transmitted continuously from the host. The chip then

8.2.3 Pin Functions

Table 8.3 shows the port 1 pin functions.

Table 8.3 Port 1 Pin Functions

Pin	Pin Functions and Selection Method
$P1_7/\overline{IRQ_3}$/TMIF	The pin function depends on bit IRQ3 in PMR1, bits CKSL2 to CKSL0 in TCRF, and bit $PCR1_7$ in PCR1.

IRQ_3	0		1	
$PCR1_7$	0	1	*	
CKSL2 to CKSL0	*		Not 0**	0**
Pin function	$P1_7$ input pin	$P1_7$ output pin	$\overline{IRQ_3}$ input pin	$\overline{IRQ_3}$/TMIF input pin

Note: When this pin is used as the TMIF input pin, clear bit IEN3 to 0 in IENR1 to disable the IRQ_3 interrupt.

$P1_6/\overline{IRQ_2}$	The pin function depends on bits IRQ2 in PMR1 and bit $PCR1_6$ in PCR1.

IRQ2	0		1
$PCR1_6$	0	1	*
Pin function	$P1_6$ input pin	$P1_6$ output pin	$\overline{IRQ_2}$ input pin

$P1_5/\overline{IRQ_1}$ TMIC	The pin function depends on bit IRQ1 in PMR1, bits TMC2 to TMC0 in TMC, and bit $PCR1_5$ in PCR1.

IRQ1	0		1	
$PCR1_5$	0	1	*	
TMC2 to TMC0	*		Not 111	111
Pin function	$P1_5$ input pin	$P1_5$ output pin	$\overline{IRQ_1}$ input pin	$\overline{IRQ_1}$/TMIC input pin

Note: When this pin is used as the TMIC input pin, clear bit IEN1 to 0 in IENR1 to disable the IRQ_1 interrupt.

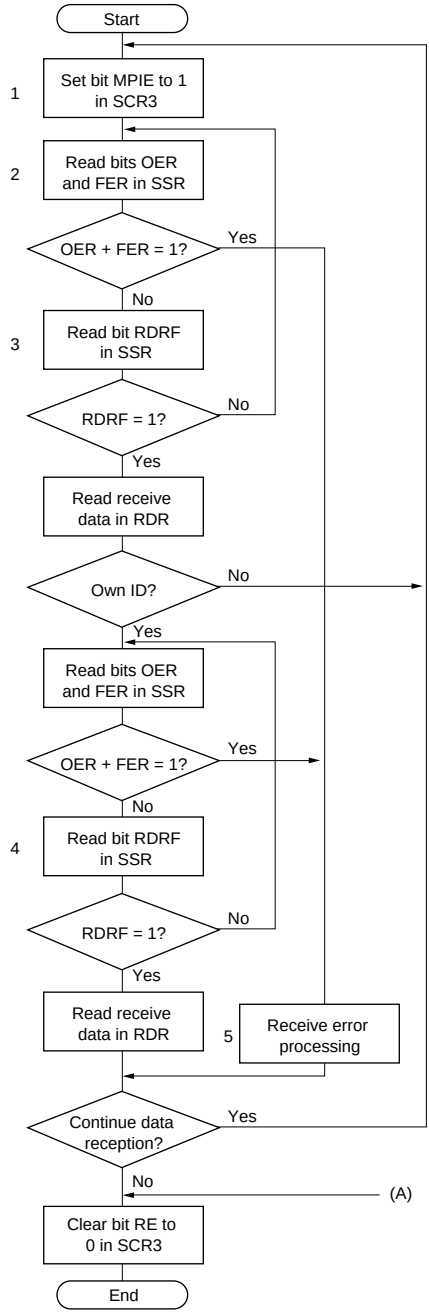
8.9.3 Pin Functions

Table 8.24 shows the port A pin functions.

Table 8.24 Port A Pin Functions

Pin	Pin Functions and Selection Method			
PA_3/COM_4	The pin function depends on bit $PCRA_3$ in PCRA and bits SGS3 to SGS0.			
	SEGS3 to SEGS0	0000	0000	Not 0000
	$PCRA_3$	0	1	*
	Pin function	PA_3 input pin	PA_3 output pin	COM_4 output pin
PA_2/COM_3	The pin function depends on bit $PCRA_2$ in PCRA and bits SGS3 to SGS0.			
	SEGS3 to SEGS0	0000	0000	Not 0000
	$PCRA_2$	0	1	*
	Pin function	PA_2 input pin	PA_2 output pin	COM_3 output pin
PA_1/COM_2	The pin function depends on bit $PCRA_1$ in PCRA and bits SGS3 to SGS0.			
	SEGS3 to SEGS0	0000	0000	Not 0000
	$PCRA_1$	0	1	*
	Pin function	PA_1 input pin	PA_1 output pin	COM_2 output pin
PA_0/COM_1	The pin function depends on bit $PCRA_0$ in PCRA and bits SGS3 to SGS0.			
	SEGS3 to SEGS0	0000		Not 0000
	$PCRA_0$	0	1	*
	Pin function	PA_0 input pin	PA_0 output pin	COM_1 output pin

*: Don't care



1. Set bit MPIE to 1 in SCR3.
2. Read bits OER and FER in the serial status register (SSR) to determine if there is an error. If a receive error has occurred, execute receive error processing.
3. Read SSR and check that bit RDRF is set to 1. If it is, read the receive data in RDR and compare it with this receiver's own ID. If the ID is not this receiver's, set bit MPIE to 1 again. When the RDR data is read, bit RDRF is cleared to 0 automatically.
4. Read SSR and check that bit RDRF is set to 1, then read the data in RDR.
5. If a receive error has occurred, read bits OER and FER in SSR to identify the error, and after carrying out the necessary error processing, ensure that bits OER and FER are both cleared to 0. Reception cannot be resumed if either of these bits is set to 1. In the case of a framing error, a break can be detected by reading the value of the RXD_{3x} pin.

Figure 10.19 Example of Multiprocessor Data Reception Flowchart

Bit 7: A/D start flag (ADSF)

Bit 7 controls and indicates the start and end of A/D conversion.

Bit 7 ADSF	Description	
0	Read: Indicates the completion of A/D conversion	(initial value)
	Write: Stops A/D conversion	
1	Read: Indicates A/D conversion in progress	
	Write: Starts A/D conversion	

Bits 6 to 0: Reserved bits

Bits 6 to 0 are reserved; they are always read as 1, and cannot be modified.

12.2.4 Clock Stop Register 1 (CKSTPR1)

Bit	7	6	5	4	3	2	1	0
	—	S31CKSTP	S32CKSTP	ADCKSTP	TGCKSTP	TFCKSTP	TCCKSTP	TACKSTP
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CKSTPR1 is an 8-bit read/write register that performs module standby mode control for peripheral modules. Only the bit relating to the A/D converter is described here. For details of the other bits, see the sections on the relevant modules.

Bit 4: A/D converter module standby mode control (ADCKSTP)

Bit 4 controls setting and clearing of module standby mode for the A/D converter.

ADCKSTP	Description	
0	A/D converter is set to module standby mode	
1	A/D converter module standby mode is cleared	(initial value)

15.5 H8/3827S Group Absolute Maximum Ratings

Table 15.15 lists the absolute maximum ratings.

Table 15.15 Absolute Maximum Ratings

Item		Symbol	Value	Unit	Notes
Power supply voltage		V_{CC}	–0.3 to +4.3	V	*1
Analog power supply voltage		AV_{CC}	–0.3 to +4.3	V	
Input voltage	Ports other than Port B	V_{in}	–0.3 to V_{CC} +0.3	V	
	Port B	AV_{in}	–0.3 to AV_{CC} +0.3	V	
Operating temperature		T_{opr}	–20 to +75 (Regular specifications)	°C	
			–40 to +85 (wide-range specifications)		
			+75 (products shipped as chips)*2		
Storage temperature		T_{stg}	–55 to +125	°C	

Notes: 1. Permanent damage may occur to the chip if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.
2. Power may be applied when the temperature is between –20 and –75°C.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input capacitance	C_{IN}	All input pins except power supply	—	—	15.0	pF	f = 1MHz, V_{IN} =0 V, T_a = 25°C	
Active mode current dissipation	I_{OPE1}	V_{CC}	—	0.4	*3	mA	Active (high-speed) mode V_{CC} = 1.8 V, f_{OSC} = 2 MHz	*1 *2
			—	1.4	*3		Active (high-speed) mode V_{CC} = 3 V, f_{OSC} = 4 MHz	
			—	3.5	5.5		Active (high-speed) mode V_{CC} = 3 V, f_{OSC} = 10 MHz	
	I_{OPE2}	V_{CC}	—	0.1	*3		Active (medium-speed) mode V_{CC} = 1.8 V, f_{OSC} = 2 MHz ϕ_{OSC}/128	
			—	0.3	*3		Active (medium-speed) mode V_{CC} = 3 V, f_{OSC} = 4 MHz ϕ_{OSC}/128	
			—	0.7	1.6		Active (medium-speed) mode V_{CC} = 3 V, f_{OSC} = 10 MHz ϕ_{OSC}/128	
Sleep mode current dissipation	I_{SLEEP}	V_{CC}	—	0.2	*3	mA	V_{CC} = 1.8 V, f_{OSC} = 2 MHz	*1 *2
			—	0.6	*3		V_{CC} = 3 V, f_{OSC} = 4 MHz	
			—	1.4	2.9		V_{CC} = 3 V, f_{OSC} = 10 MHz	

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Active mode current consumption	I_{OPE2}	V_{CC}	—	0.4	—	mA	Active (medium-speed) mode V_{CC} = 2.7 V, f_{OSC} = 2 MHz, ϕ_{OSC}/128	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.7	—			*2 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.5	—		Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 2 MHz, ϕ_{OSC}/128	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	1.0	—			*2 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.8	—		Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 4 MHz, ϕ_{OSC}/128	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	1.2	—			*2 *3 *4
			—	1.2	3.0		Active (medium-speed) mode V_{CC} = 5 V, f_{OSC} = 10 MHz, ϕ_{OSC}/128	*1 *3 *4
			—	1.7	3.0			*2 *3 *4

Appendix B Internal I/O Registers

B.1 Addresses

Upper Address: H'F0

Lower Address	Register Name	Bit Names								Module Name
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'20	FLMCR1	—	SWE	ESU	PSU	EV	PV	E	P	ROM
H'21	FLMCR2	FLER	—	—	—	—	—	—	—	
H'22	FLPWCR	PDWND	—	—	—	—	—	—	—	
H'23	EBR	EB7	EB6	EB5	EB4	EB3	EB2	EB1	EB0	
H'24										
H'25										
H'26										
H'27										
H'28										
H'29										
H'2A										
H'2B	FENR	FLSHE	—	—	—	—	—	—	—	
H'2C										
H'2D										
H'2E										
H'2F										

TCRF—Timer Control Register F H'B6 Timer F

Bit	7	6	5	4	3	2	1	0
	TOLH	CKSH2	CKSH1	CKSH0	TOLL	CKSL2	CKSL1	CKSL0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Clock select L

0	*	*	Counting on external event (TMIF) rising/falling edge
1	0	0	Internal clock φ/32
1	0	1	Internal clock φ/16
1	1	0	Internal clock φ/4
1	1	1	Internal clock φw/4

Toggle output level L

0	Low level
1	High level

Clock select H

0	*	*	16-bit mode, counting on TCFL overflow signal
1	0	0	Internal clock φ/32
1	0	1	Internal clock φ/16
1	1	0	Internal clock φ/4
1	1	1	Internal clock φw/4

* : Don't care

Toggle output level H

0	Low level
1	High level

ADSR—A/D Start Register **H'C7** **A/D converter**

Bit	7	6	5	4	3	2	1	0
	ADSF	—	—	—	—	—	—	—
Initial value	0	1	1	1	1	1	1	1
Read/Write	R/W	—	—	—	—	—	—	—

A/D status flag

0	Read	Indicates completion of A/D conversion
	Write	Stops A/D conversion
1	Read	Indicates A/D conversion in progress
	Write	Starts A/D conversion

PMR1—Port Mode Register 1 H'C8 I/O port

Bit	7	6	5	4	3	2	1	0
	IRQ3	IRQ2	IRQ1	IRQ4	TMIG	TMOFH	TMOFL	TMOW
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

$P1_0$/TMOW pin function switch

0	Functions as $P1_0$ I/O pin
1	Functions as TMOW output pin

$P1_1$/TMOFL pin function switch

0	Functions as $P1_1$ I/O pin
1	Functions as TMOFL output pin

$P1_2$/TMOFH pin function switch

0	Functions as $P1_2$ I/O pin
1	Functions as TMOFH output pin

$P1_3$/TMIG pin function switch

0	Functions as $P1_3$ I/O pin
1	Functions as TMIG input pin

$P1_4$/$\overline{IRQ_4}$/$\overline{ADTRG}$ pin function switch

0	Functions as $P1_4$ I/O pin
1	Functions as $\overline{IRQ_4}$/$\overline{ADTRG}$ input pin

$P1_5$/$\overline{IRQ_1}$/TMIC pin function switch

0	Functions as $P1_5$ I/O pin
1	Functions as $\overline{IRQ_1}$/TMIC input pin

$P1_6$/$\overline{IRQ_2}$ pin function switch

0	Functions as $P1_6$ I/O pin
1	Functions as $\overline{IRQ_2}$ input pin

$P1_7$/$\overline{IRQ_3}$/TMIF pin function switch

0	Functions as $P1_7$ I/O pin
1	Functions as $\overline{IRQ_3}$/TMIF input pin

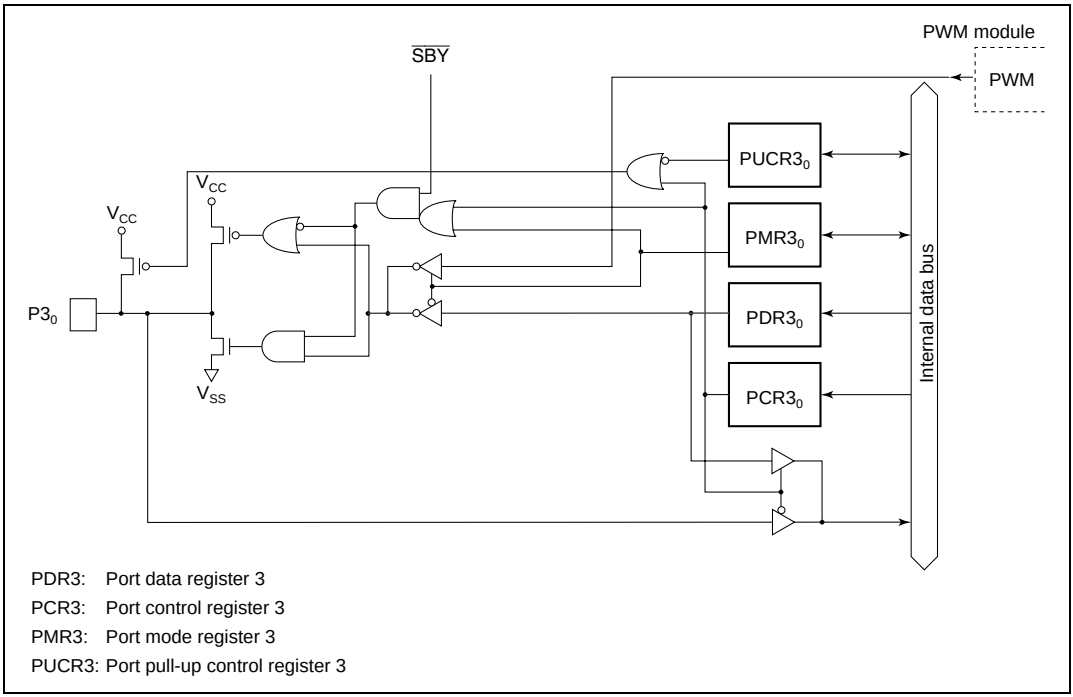


Figure C.2 (g) Port 3 Block Diagram (Pin $P3_0$)

Appendix D Port States in the Different Processing States

Table D.1 Port States Overview

Port	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P1_7$ to $P1_0$	High impedance	Retained	Retained	High impedance*1	Retained	Functions	Functions
$P3_7$ to $P3_0$	High impedance*2	Retained	Retained	High impedance*1	Retained	Functions	Functions
$P4_3$ to $P4_0$	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
$P5_7$ to $P5_0$	High impedance	Retained	Retained	High impedance*1	Retained	Functions	Functions
$P6_7$ to $P6_0$	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
$P7_7$ to $P7_0$	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
$P8_7$ to $P8_0$	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
PA_3 to PA_0	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
PB_7 to PB_0	High impedance	High impedance	High impedance	High impedance	High impedance	High impedance	High impedance

Notes: 1. High level output when MOS pull-up is in on state.

2. Reset output from $P3_2$ pin only (H8/3827R Group and H8/3827S Group).
On-chip pull-up MOS turns on for pin $P3_2$ only (F-ZTAT Version of the H8/38327 Group and H8/38427 Group).