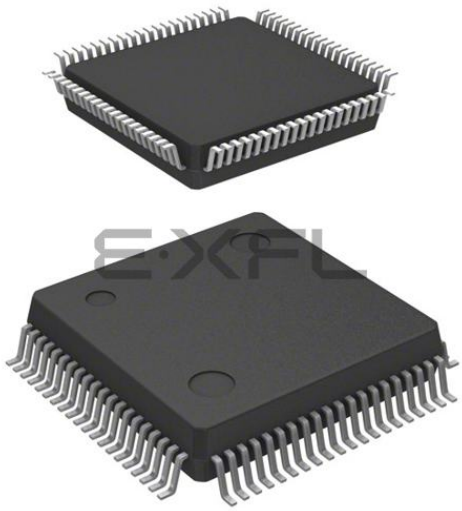

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	55
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38327hv

2.9 Application Notes

2.9.1 Notes on Data Access

1. Access to Empty Areas:

   The address space of the H8/300L CPU includes empty areas in addition to the RAM, registers, and ROM areas available to the user. If these empty areas are mistakenly accessed by an application program, the following results will occur.

   Data transfer from CPU to empty area:

   The transferred data will be lost. This action may also cause the CPU to misoperate.

   Data transfer from empty area to CPU:

   Unpredictable data is transferred.

2. Access to Internal I/O Registers:

   Internal data transfer to or from on-chip modules other than the ROM and RAM areas makes use of an 8-bit data width. If word access is attempted to these areas, the following results will occur.

   Word access from CPU to I/O register area:

   Upper byte: Will be written to I/O register.

   Lower byte: Transferred data will be lost.

   Word access from I/O register to CPU:

   Upper byte: Will be written to upper part of CPU register.

   Lower byte: Unpredictable data will be written to lower part of CPU register.

Byte size instructions should therefore be used when transferring data to or from I/O registers other than the on-chip ROM and RAM areas. Figure 2.17 shows the data size and number of states in which on-chip peripheral modules can be accessed.

Bits 4 to 0: IRQ_4 to IRQ_0 interrupt request flags (IRRI4 to IRRI0)

Bit n IRRIn	Description	
0	Clearing condition:	(initial value)
	When IRRIn = 1, it is cleared by writing 0	
1	Setting condition:	
	When pin $\overline{IRQ}$n is designated for interrupt input and the designated signal edge is input	

(n = 4 to 0)

5. Interrupt Request Register 2 (IRR2)

Bit	7	6	5	4	3	2	1	0
	IRRDT	IRRAD	—	IRRTG	IRRTFH	IRRTFL	IRRTC	IRREC
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W*	R/W*	R/W	R/W*	R/W*	R/W*	R/W*	R/W*

Note: * Only a write of 0 for flag clearing is possible

IRR2 is an 8-bit read/write register, in which a corresponding flag is set to 1 when a direct transfer, A/D converter, Timer G, Timer FH, Timer FC, or Timer C interrupt is requested. The flags are not cleared automatically when an interrupt is accepted. It is necessary to write 0 to clear each flag.

Bit 7: Direct transfer interrupt request flag (IRRDT)

Bit 7 IRRDT	Description	
0	Clearing condition:	(initial value)
	When IRRDT = 1, it is cleared by writing 0	
1	Setting condition:	
	When a direct transfer is made by executing a SLEEP instruction while DTON = 1 in SYSCR2	

Bits 1 and 0: Active (medium-speed) mode clock select (MA1, MA0)

Bits 1 and 0 choose $\phi_{OSC}/128$, $\phi_{OSC}/64$, $\phi_{OSC}/32$, or $\phi_{OSC}/16$ as the operating clock in active (medium-speed) mode and sleep (medium-speed) mode. MA1 and MA0 should be written in active (high-speed) mode or subactive mode.

Bit 1 MA1	Bit 0 MA0	Description	
0	0	$\phi_{OSC}/16$	
0	1	$\phi_{OSC}/32$	
1	0	$\phi_{OSC}/64$	
1	1	$\phi_{OSC}/128$	(initial value)

2. System Control Register 2 (SYSCR2)

Bit	7	6	5	4	3	2	1	0
	—	—	—	NESEL	DTON	MSON	SA1	SA0
Initial value	1	1	1	1	0	0	0	0
Read/Write	—	—	—	R/W	R/W	R/W	R/W	R/W

SYSCR2 is an 8-bit read/write register for power-down mode control.

Bits 7 to 5: Reserved bits

These bits are reserved; they are always read as 1, and cannot be modified.

Bit 4: Noise elimination sampling frequency select (NESEL)

This bit selects the frequency at which the watch clock signal (ϕ_W) generated by the subclock pulse generator is sampled, in relation to the oscillator clock (ϕ_{OSC}) generated by the system clock pulse generator. When ϕ_{OSC} = 2 to 16 MHz, clear NESEL to 0.

Bit 4 NESEL	Description	
0	Sampling rate is $\phi_{OSC}/16$	
1	Sampling rate is $\phi_{OSC}/4$	(initial value)

6.3.2 Programming Precautions

- Use the specified programming voltage and timing.

  The programming voltage in PROM mode (V_{PP}) is 12.5 V. Use of a higher voltage can permanently damage the chip. Be especially careful with respect to PROM programmer overshoot.

  Setting the PROM programmer to Renesas specifications for the HN27C101 will result in correct V_{PP} of 12.5 V.
- Make sure the index marks on the PROM programmer socket, socket adapter, and chip are properly aligned. If they are not, the chip may be destroyed by excessive current flow. Before programming, be sure that the chip is properly mounted in the PROM programmer.
- Avoid touching the socket adapter or chip while programming, since this may cause contact faults and write errors.
- Take care when setting the programming mode, as page programming is not supported.
- When programming with a PROM programmer, be sure to specify addresses from H'0000 to H'EDFF. If programming is inadvertently performed from H'EE00 onward, it may not be possible to continue PROM programming and verification. When programming, H'FF should be set as the data in address area H'EE00 to H'1FFFF.

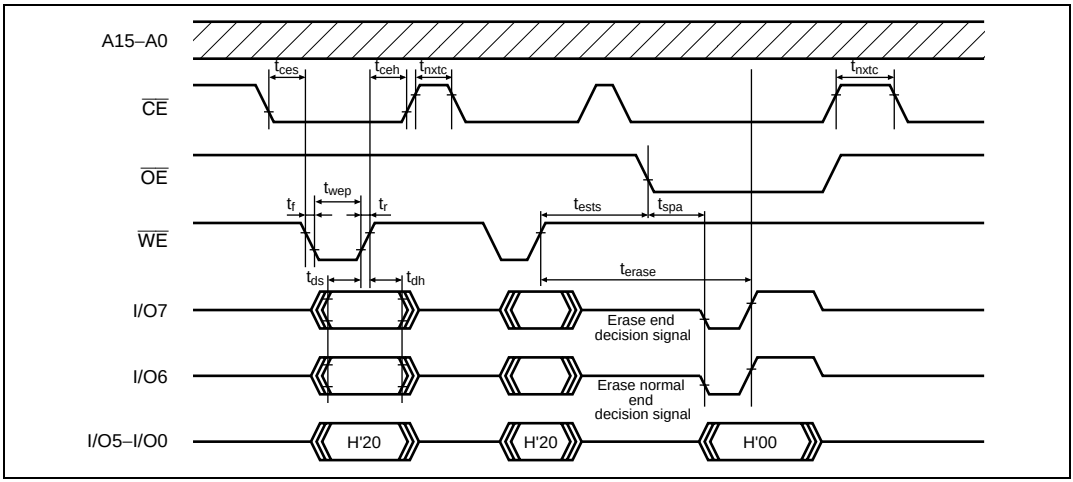


Figure 6.18 Auto-Erase Mode Timing Waveforms

6.10.6 Status Read Mode

1. Status read mode is provided to identify the kind of abnormal end. Use this mode when an abnormal end occurs in auto-program mode or auto-erase mode.
2. The return code is retained until a command write other than a status read mode command write is executed.
3. Table 6.20 shows the AC characteristics and 6.21 shows the return codes.

Bit 3: Toggle output level L (TOLL)

Bit 3 sets the TMOFL pin output level. The output level is effective immediately after this bit is written.

Bit 3 TOLL	Description	
0	Low level	(initial value)
1	High level	

Bits 2 to 0: Clock select L (CKSL2 to CKSL0)

Bits 2 to 0 select the clock input to TCFL from among four internal clock sources or external event input.

Bit 2 CKSL2	Bit 1 CKSL1	Bit 0 CKSL0	Description
0	0	0	Counting on external event (TMIF) rising/falling edge* (initial value)
0	0	1	
0	1	0	
0	1	1	Use prohibited
1	0	0	Internal clock: Counting on $\phi/32$
1	0	1	Internal clock: Counting on $\phi/16$
1	1	0	Internal clock: Counting on $\phi/4$
1	1	1	Internal clock: Counting on $\phi w/4$

Note: * External event edge selection is set by IEG3 in the IRQ edge select register (IEGR). For details, see 1. IRQ edge select register (IEGR) in section 3.3.2.

Note that the timer F counter may increment if the setting of IRQ3 in port mode register 1 (PMR1) is changed from 0 to 1 while the TMIF pin is low in order to change the TMIF pin function.

4. Timer Control/Status Register F (TCSRF)

Bit	7	6	5	4	3	2	1	0
	OVFH	CMFH	OVIEH	CCLRH	OVFL	CMFL	OVIEL	CCLRL
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W*	R/W*	R/W	R/W	R/W*	R/W*	R/W	R/W

Note: * Bits 7, 6, 3, and 2 can only be written with 0, for flag clearing.

TCSRF is an 8-bit read/write register that performs counter clear selection, overflow flag setting, and compare match flag setting, and controls enabling of overflow interrupt requests.

TCSRF is initialized to H'00 upon reset.

Bit 7: Timer overflow flag H (OVFH)

Bit 7 is a status flag indicating that TCFH has overflowed from H'FF to H'00. This flag is set by hardware and cleared by software. It cannot be set by software.

Bit 7 OVFH	**Description**	
0	Clearing condition: After reading OVFH = 1, cleared by writing 0 to OVFH	(initial value)
1	Setting condition: Set when TCFH overflows from H'FF to H'00	

Bit 6: Compare match flag H (CMFH)

Bit 6 is a status flag indicating that TCFH has matched OCRFH. This flag is set by hardware and cleared by software. It cannot be set by software.

Bit 6 CMFH	**Description**	
0	Clearing condition: After reading CMFH = 1, cleared by writing 0 to CMFH	(initial value)
1	Setting condition: Set when the TCFH value matches the OCRFH value	

Bit 5: Timer overflow interrupt enable H (OVIEH)

Bit 5 selects enabling or disabling of interrupt generation when TCFH overflows.

Bit 5 OVIEH	Description	
0	TCFH overflow interrupt request is disabled	(initial value)
1	TCFH overflow interrupt request is enabled	

Bit 4: Counter clear H (CCLRH)

In 16-bit mode, bit 4 selects whether TCF is cleared when TCF and OCRF match.

In 8-bit mode, bit 4 selects whether TCFH is cleared when TCFH and OCRFH match.

Bit 4 CCLRH	Description	
0	16-bit mode: TCF clearing by compare match is disabled	
	8-bit mode: TCFH clearing by compare match is disabled	(initial value)
1	16-bit mode: TCF clearing by compare match is enabled	
	8-bit mode: TCFH clearing by compare match is enabled	

Bit 3: Timer overflow flag L (OVFL)

Bit 3 is a status flag indicating that TCFL has overflowed from H'FF to H'00. This flag is set by hardware and cleared by software. It cannot be set by software.

Bit 3 OVFL	Description	
0	Clearing condition:	(initial value)
	After reading OVFL = 1, cleared by writing 0 to OVFL	
1	Setting condition:	
	Set when TCFL overflows from H'FF to H'00	

Figure 9.4 shows an example in which H'AA55 is written to TCF.

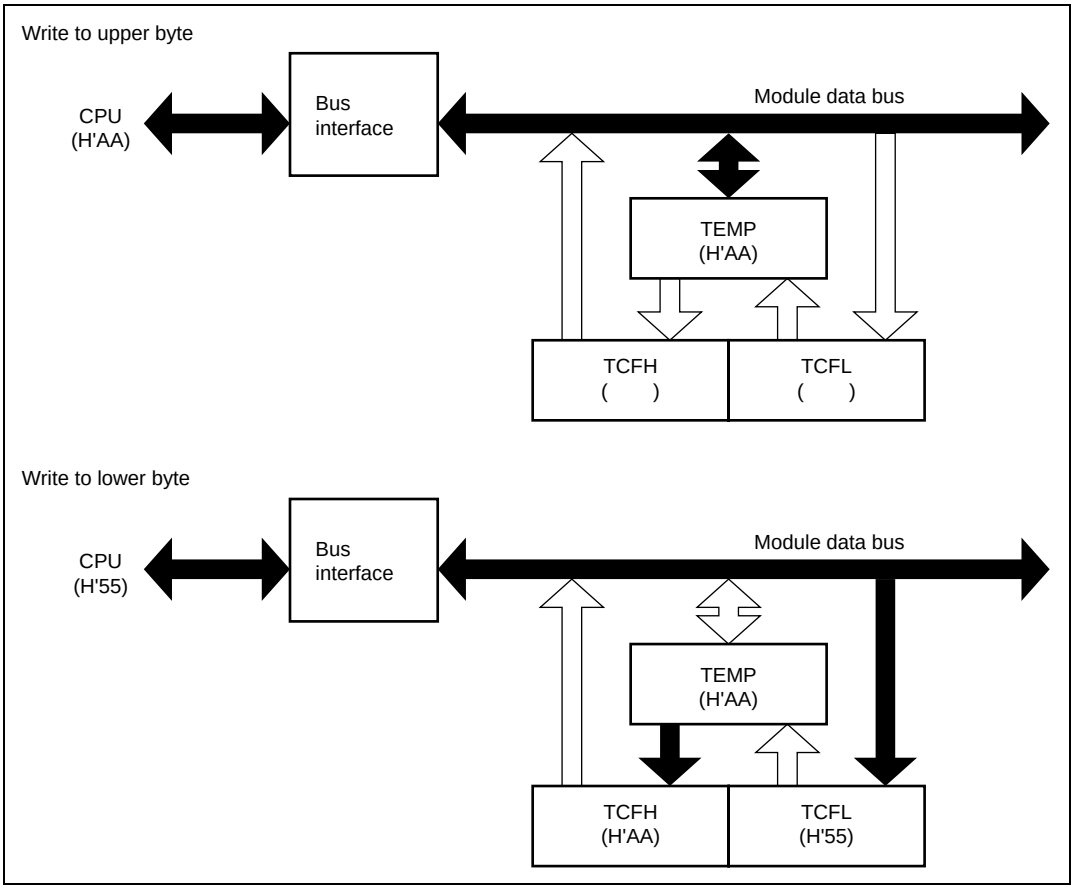


Figure 9.4 Write Access to TCR (CPU → TCF)

Bit 6: Timer counter W write enable (TCWE)

Bit 6 controls the writing of data to TCW.

Bit 6 TCWE	Description	
0	Data cannot be written to TCW	(initial value)
1	Data can be written to TCW	

Bit 5: Bit 4 write inhibit (B4WI)

Bit 5 controls the writing of data to bit 4 in TCSRW.

Bit 5 B4WI	Description	
0	Bit 4 is write-enabled	
1	Bit 4 is write-protected	(initial value)

This bit is always read as 1. Data written to this bit is not stored.

Bit 4: Timer control/status register W write enable (TCSRWE)

Bit 4 controls the writing of data to TCSRW bits 2 and 0.

Bit 4 TCSRWE	Description	
0	Data cannot be written to bits 2 and 0	(initial value)
1	Data can be written to bits 2 and 0	

Bit 3: Bit 2 write inhibit (B2WI)

Bit 3 controls the writing of data to bit 2 in TCSRW.

Bit 3 B2WI	Description	
0	Bit 2 is write-enabled	
1	Bit 2 is write-protected	(initial value)

This bit is always read as 1. Data written to this bit is not stored.

1. Data Transfer Format

The general data transfer format in asynchronous communication is shown in figure 10.10.

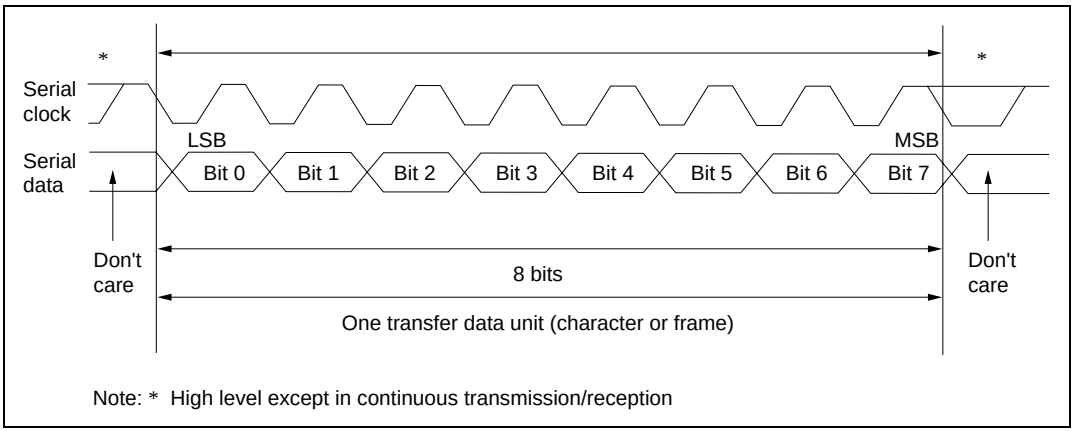


Figure 10.10 Data Format in Synchronous Communication

In synchronous communication, data on the communication line is output from one falling edge of the serial clock until the next falling edge. Data confirmation is guaranteed at the rising edge of the serial clock.

One transfer data character begins with the LSB and ends with the MSB. After output of the MSB, the communication line retains the MSB state.

When receiving in synchronous mode, SCI3 latches receive data at the rising edge of the serial clock.

The data transfer format uses a fixed 8-bit data length.

Parity and multiprocessor bits cannot be added.

2. Clock

Either an internal clock generated by the baud rate generator or an external clock input at the SCK_{3x} pin can be selected as the SCI3 serial clock. The selection is made by means of bit COM in SMR and bits CKE1 and CKE0 in SCR3. See table 10.9 for details on clock source selection.

When SCI3 operates on an internal clock, the serial clock is output at the SCK_{3x} pin. Eight pulses of the serial clock are output in transmission or reception of one character, and when SCI3 is not transmitting or receiving, the clock is fixed at the high level.

d. LCD drive power supply setting

With the H8/3827R Group, there are two ways of providing LCD power: by using the on-chip power supply circuit, or by using an external circuit.

When the on-chip power supply circuit is used for the LCD drive power supply, the V_0 and V_1 pins should be interconnected externally, as shown in figure 13.4 (a).

When an external power supply circuit is used for the LCD drive power supply, connect the external power supply to the V_1 pin, and short the V_0 pin to V_{CC} externally, as shown in figure 13.4 (b).

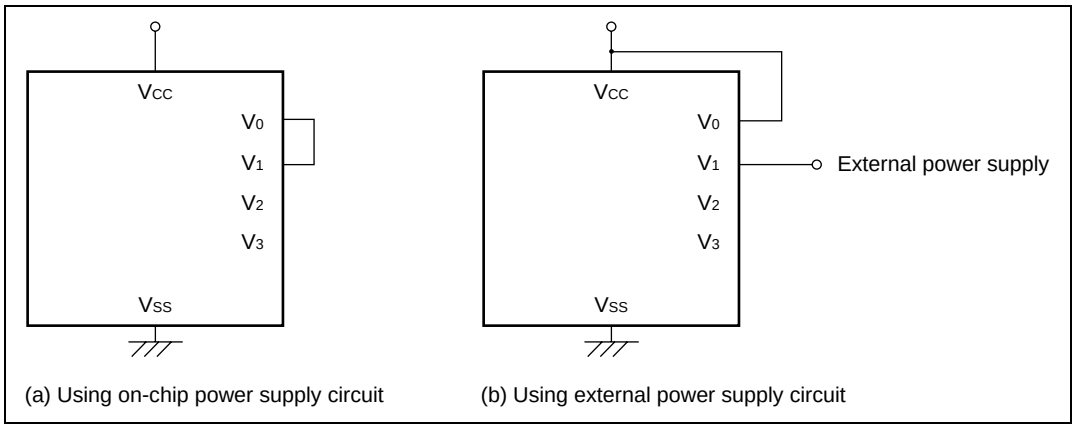


Figure 13.4 Examples of LCD Power Supply Pin Connections

e. Low-power-consumption LCD drive system

Use of a low-power-consumption LCD drive system enables the power consumption required for LCD drive to be optimized. For details, see section 13.3.4, Low-Power-Consumption LCD Drive System.

f. Segment external expansion

The number of segments can be increased by connecting an HD66100 externally. For details, see section 13.3.7, Connection to HD66100.

13.3.2 Relationship between LCD RAM and Display

The relationship between the LCD RAM and the display segments differs according to the duty cycle. LCD RAM maps for the different duty cycles when segment external expansion is not used are shown in figures 13.5 to 13.8, and LCD RAM maps when segment external expansion is used in figures 13.9 to 13.12.

After setting the registers required for display, data is written to the part corresponding to the duty using the same kind of instruction as for ordinary RAM, and display is started automatically when turned on. Word- or byte-access instructions can be used for RAM setting.

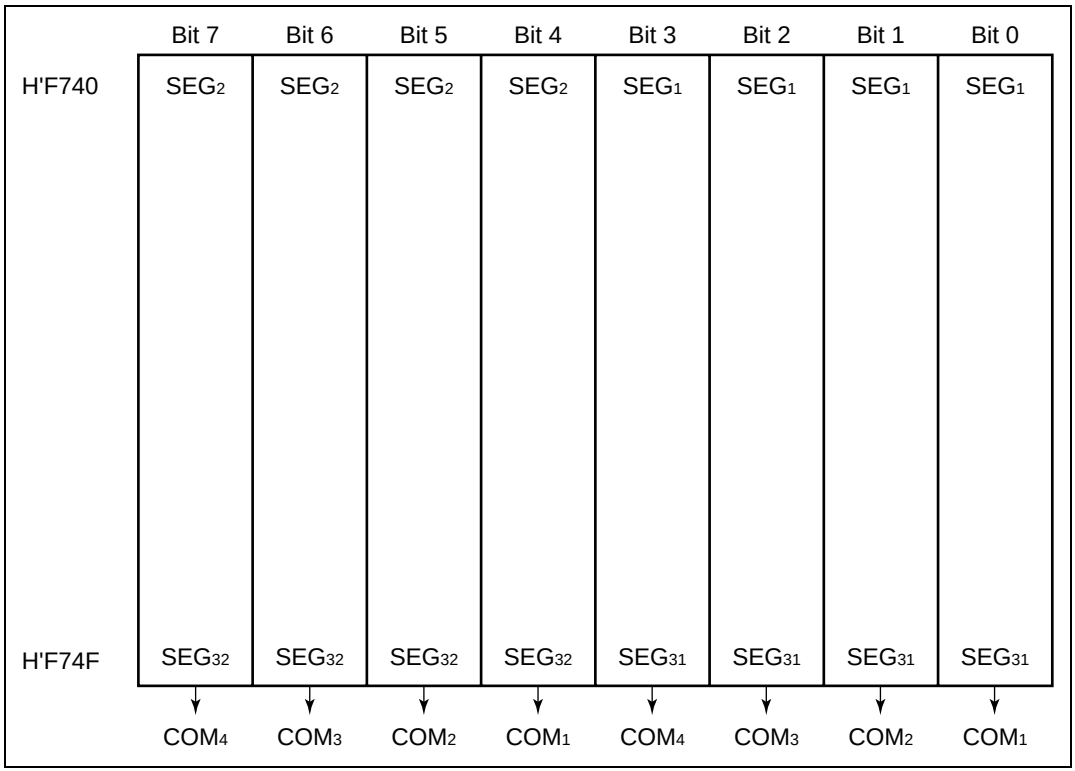


Figure 13.5 LCD RAM Map when Not Using Segment External Expansion (1/4 Duty)

Table 13.4 Power-Down Modes and Display Operation

Mode		Reset	Active	Sleep	Watch	Sub-active	Sub-sleep	Standby	Module Standby
Clock	φ	Runs	Runs	Runs	Stops	Stops	Stops	Stops	Stops*4
	φw	Runs	Runs	Runs	Runs	Runs	Runs	Stops*1	Stops*4
Display operation	ACT = "0"	Stops	Stops	Stops	Stops	Stops	Stops	Stops*2	Stops
	ACT = "1"	Stops	Functions	Functions	Functions *3	Functions *3	Functions *3	Stops*2	Stops

Notes: 1. The subclock oscillator does not stop, but clock supply is halted.
2. The LCD drive power supply is turned off regardless of the setting of the PSW bit.
3. Display operation is performed only if φw, φw/2, or φw/4 is selected as the operating clock.
4. The clock supplied to the LCD stops.

13.3.6 Boosting the LCD Drive Power Supply

When a large panel is driven, the on-chip power supply capacity may be insufficient. If the power supply capacity is insufficient when V_{CC} is used as the power supply, the power supply impedance must be reduced. This can be done by connecting bypass capacitors of around 0.1 to 0.3 µF to pins V_1 to V_3, as shown in figure 13.17, or by adding a split-resistance externally.

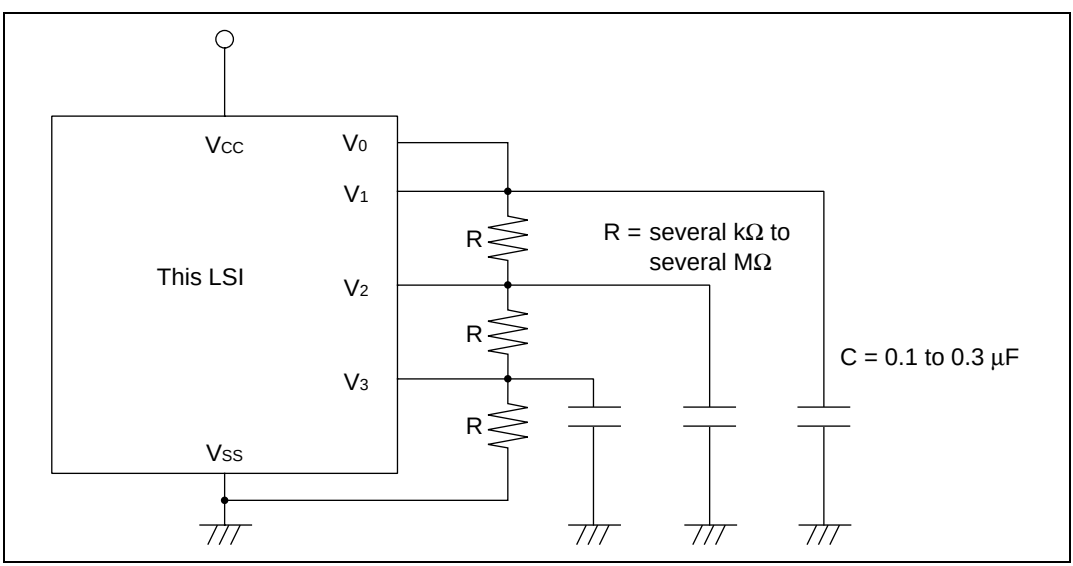
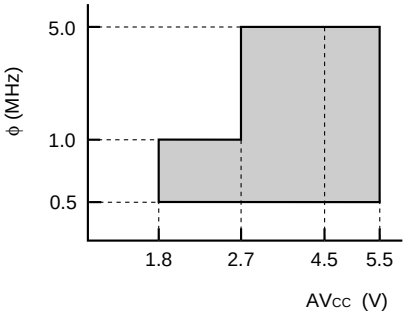
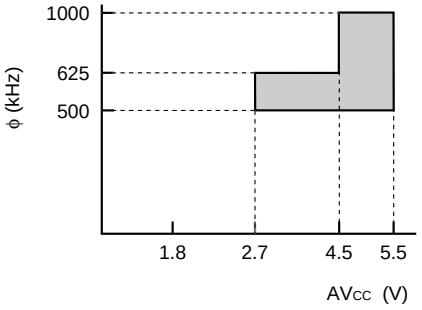


Figure 13.17 Connection of External Split-Resistance

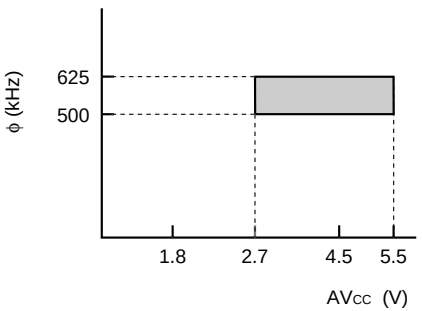
3. Analog Power Supply Voltage and A/D Converter Operating Range



- Active (high-speed) mode
- Sleep (high-speed) mode
- Internal power supply step-down circuit not used and used



- Active (medium-speed) mode
- Sleep (medium-speed) mode
- Internal power supply step-down circuit not used



- Active (medium-speed) mode
- Sleep (medium-speed) mode
- Internal power supply step-down circuit used

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Watch mode current dissipation	I_{WATCH}	V_{CC}	—	2.8	6	µA	V_{CC} = 2.7 V 3 2 kHz crystal oscillator LCD not used	*3 *4 *5
Standby mode current dissipation	I_{STBY}	V_{CC}	—	1.0	5.0	µA	32 kHz crystal oscillator not used	*3 *4
RAM data retaining voltage	V_{RAM}	V_{CC}	1.5	—	—	V		*3 *4
Allowable output low current (per pin)	I_{OL}	Output pins except port 3	—	—	2.0	mA	V_{CC} = 4.0 V to 5.5 V	
		Port 3	—	—	10.0		V_{CC} = 4.0 V to 5.5 V	
		All output pins	—	—	0.5			
Allowable output low current (total)	ΣI_{OL}	Output pins except port 3	—	—	40.0	mA	V_{CC} = 4.0 V to 5.5 V	
		Port 3	—	—	80.0		V_{CC} = 4.0 V to 5.5 V	
		All output pins	—	—	20.0			
Allowable output high current (per pin)	$-I_{OH}$	All output pins	—	—	2.0	mA	V_{CC} = 4.0 V to 5.5 V	
			—	—	0.2		Except the above	
Allowable output high current (total)	$\Sigma - I_{OH}$	All output pins	—	—	15.0	mA	V_{CC} = 4.0 V to 5.5 V	
			—	—	10.0		Except the above	

Notes: 1. Applies to the Mask ROM products.
2. Applies to the HD6473827R.

15.4.4 A/D Converter Characteristics

Table 15.12 shows the A/D converter characteristics of the H8/3827R.

Table 15.12 A/D Converter Characteristics

V_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –40°C to +85°C unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Analog power supply voltage	AV_{CC}	AV_{CC}	1.8	—	5.5	V		*1
Analog input voltage	AV_{IN}	AN_0 to AN_7	– 0.3	—	AV_{CC} + 0.3	V		
Analog power supply current	AI_{OPE}	AV_{CC}	—	—	1.5	mA	AV_{CC} = 5 V	
	AI_{STOP1}	AV_{CC}	—	600	—	µA		*2 Reference value
	AI_{STOP2}	AV_{CC}	—	—	5	µA		*3
Analog input capacitance	C_{AIN}	AN_0 to AN_7	—	—	15.0	pF		
Allowable signal source impedance	R_{AIN}		—	—	10.0	kΩ		
Resolution (data length)			—	—	10	bit		
Nonlinearity error			—	—	±2.5	LSB	AV_{CC} = 2.7 V to 5.5 V V_{CC} = 2.7 V to 5.5 V	*4
			—	—	±5.5		AV_{CC} = 2.0 V to 5.5 V V_{CC} = 2.0 V to 5.5 V	
			—	—	±7.5		Except the above	*5
Quantization error			—	—	±0.5	LSB		

PMR3—Port Mode Register 3 H'CA I/O port

Bit	7	6	5	4	3	2	1	0
	AEVL	AEVH	WDCKS	NCS	IRQ0	RESO*	UD	PWM
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

$P3_0$/PWM pin function switch

0	Functions as $P3_0$ I/O pin
1	Functions as PWM output pin

$P3_1$/UD pin function switch

0	Functions as $P3_1$ I/O pin
1	Functions as UD input pin

$P3_2$/RESO pin function switch

0	Functions as $P3_2$ I/O pin
1	Functions as $\overline{\text{RESO}}$ I/O pin

$P4_3$/$\overline{\text{IRQ}_0}$ pin function switch

0	Functions as $P4_3$ I/O pin
1	Functions as $\overline{\text{IRQ}_0}$ input pin

TMIG noise canceler select

0	Noise cancellation function not used
1	Noise cancellation function used

Watchdog timer switch

0	ϕ8192
1	$\phi_W/4$

$P3_6$/AEVH pin function switch

0	Functions as $P3_6$ I/O pin
1	Functions as AEVH input pin

$P3_7$/AEVL pin function switch

0	Functions as $P3_7$ I/O pin
1	Functions as AEVL input pin

Note: * In the H8/38327 Group and H8/38427 Group this bit is reserved and cannot be written to.

PWDRU—PWM Data Register U **H'D1** **14-bit PWM**

Bit	7	6	5	4	3	2	1	0
	—	—	PWDRU5	PWDRU4	PWDRU3	PWDRU2	PWDUR1	PWDRU0
Initial value	1	1	0	0	0	0	0	0
Read/Write	—	—	W	W	W	W	W	W

Upper 6 bits of data for generating PWM waveform

PWDRL—PWM Data Register L **H'D2** **14-bit PWM**

Bit	7	6	5	4	3	2	1	0
	PWDRL7	PWDRL6	PWDRL5	PWDRL4	PWDRL3	PWDRL2	PWDRL1	PWDRL0
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Lower 8 bits of data for generating PWM waveform

PDR1—Port Data Register 1 **H'D4** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	$P1_7$	$P1_6$	$P1_5$	$P1_4$	$P1_3$	$P1_2$	$P1_1$	$P1_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 1 pins

PDR3—Port Data Register 3 **H'D6** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Data for port 3 pins

Product Type				Product Code	Mark Code	Package (Package Code)
H8/3827S Group	H8/3826S	Mask ROM versions	Regular products	HD6433826SH	HD6433826S(***)H	80-pin QFP (FP-80A)
				HD6433826SW	HD6433826S(***)W	80-pin TQFP (TFP-80C)
				HCD6433826S	—	Die
			Wide-range specification products	HD6433826SD	HD6433826S(***)H	80-pin QFP (FP-80A)
				HD6433826SWI	HD6433826S(***)W	80-pin TQFP (TFP-80C)
	H8/3827S	Mask ROM versions	Regular products	HD6433827SH	HD6433827S(***)H	80-pin QFP (FP-80A)
				HD6433827SW	HD6433827S(***)W	80-pin TQFP (TFP-80C)
				HCD6433827S	—	Die
			Wide-range specification products	HD6433827SD	HD6433827S(***)H	80-pin QFP (FP-80A)
				HD6433827SWI	HD6433827S(***)W	80-pin TQFP (TFP-80C)
H8/38327 Group	H8/38322	Mask ROM versions	Regular products	HD64338322H	38322H	80-pin QFP (FP-80A)
				HD64338322W	38322W	80-pin TQFP (TFP-80C)
				HCD64338322	—	Die
			Wide-range specification products	HD64338322HW	38322H	80-pin QFP (FP-80A)
				HD64338322WW	38322W	80-pin TQFP (TFP-80C)
	H8/38323	Mask ROM versions	Regular products	HD64338323H	38323H	80-pin QFP (FP-80A)
				HD64338323W	38323W	80-pin TQFP (TFP-80C)
				HCD64338323	—	Die
			Wide-range specification products	HD64338323HW	38323H	80-pin QFP (FP-80A)
				HD64338323WW	38323W	80-pin TQFP (TFP-80C)
	H8/38324	Mask ROM versions	Regular products	HD64338324H	38324H	80-pin QFP (FP-80A)
				HD64338324W	38324W	80-pin TQFP (TFP-80C)
				HCD64338324	—	Die
			Wide-range specification products	HD64338324HW	38324H	80-pin QFP (FP-80A)
				HD64338324WW	38324W	80-pin TQFP (TFP-80C)
		F-ZTAT versions	Regular products	HD64F38324H	F38324H	80-pin QFP (FP-80A)
				HD64F38324W	F38324W	80-pin TQFP (TFP-80C)
			Wide-range specification products	HD64F38324HW	F38324H	80-pin QFP (FP-80A)
				HD64F38324WW	F38324W	80-pin TQFP (TFP-80C)