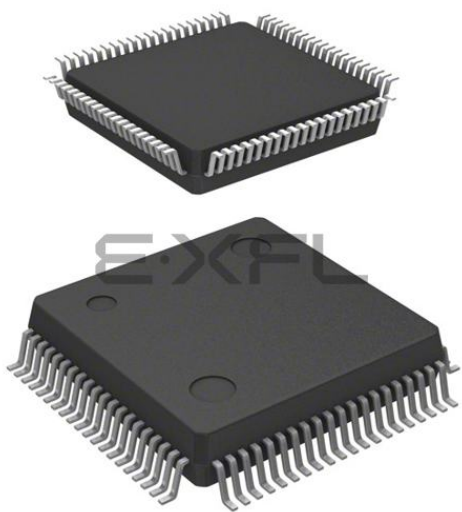




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Details

Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	55
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38327hwv

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2.5 Instruction Set

The H8/300L Series can use a total of 55 instructions, which are grouped by function in table 2.3.

Table 2.3 Instruction Set

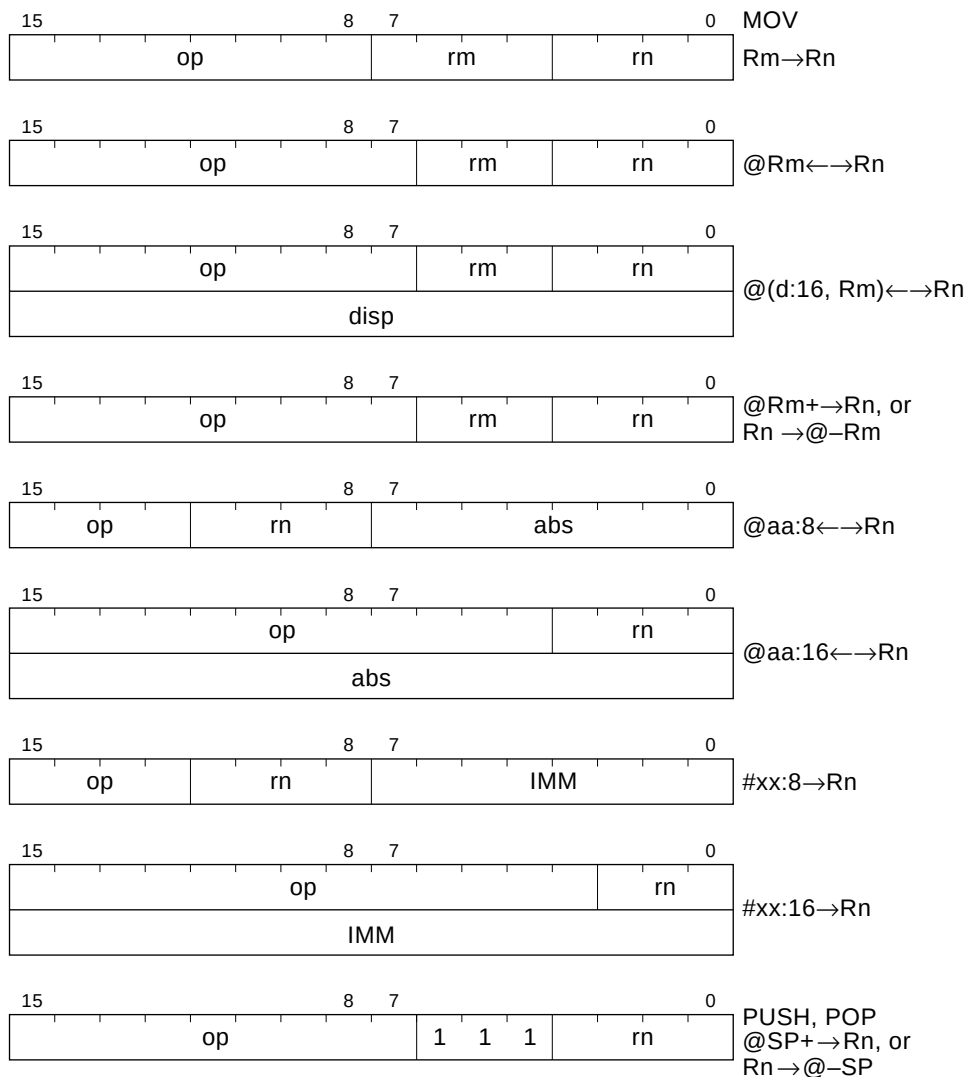
Function	Instructions	Number
Data transfer	MOV, PUSH* ¹ , POP* ¹	1
Arithmetic operations	ADD, SUB, ADDX, SUBX, INC, DEC, ADDS, SUBS, DAA, DAS, MULXU, DIVXU, CMP, NEG	14
Logic operations	AND, OR, XOR, NOT	4
Shift	SHAL, SHAR, SHLL, SHLR, ROTL, ROTR, ROTXL, ROTXR	8
Bit manipulation	BSET, BCLR, BNOT, BTST, BAND, BIAND, BOR, BIOR, BXOR, BIXOR, BLD, BILD, BST, BIST	14
Branch	Bcc* ² , JMP, BSR, JSR, RTS	5
System control	RTE, SLEEP, LDC, STC, ANDC, ORC, XORC, NOP	8
Block data transfer	EEPMOV	1
		Total: 55

Notes: 1. PUSH Rn is equivalent to MOV.W Rn, @-SP.

POP Rn is equivalent to MOV.W @SP+, Rn. The same applies to the machine language.

2. Bcc is a conditional branch instruction in which cc represents a condition code.

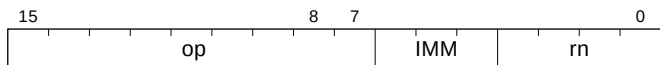
The following sections give a concise summary of the instructions in each category, and indicate the bit patterns of their object code. The notation used is defined next.



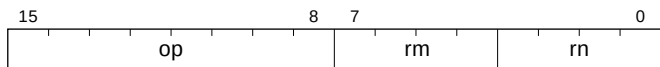
Legend:

op: Operation field
rm, rn: Register field
disp: Displacement
abs: Absolute address
IMM: Immediate data

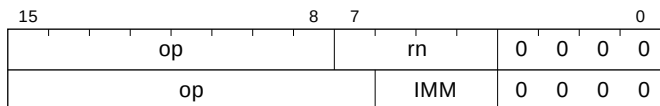
Figure 2.5 Data Transfer Instruction Codes

BSET, BCLR, BNOT, BTST

Operand: register direct (Rn)
Bit No.: immediate (#xx:3)

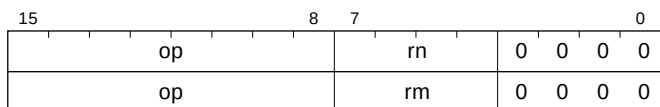


Operand: register direct (Rn)
Bit No.: register direct (Rm)



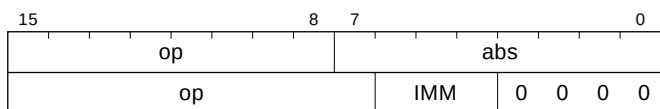
Operand: register indirect (@Rn)

Bit No.: immediate (#xx:3)



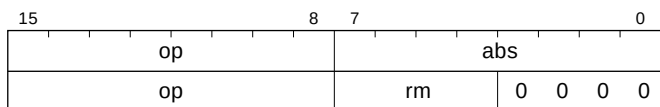
Operand: register indirect (@Rn)

Bit No.: register direct (Rm)



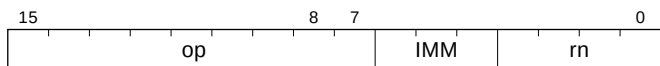
Operand: absolute (@aa:8)

Bit No.: immediate (#xx:3)

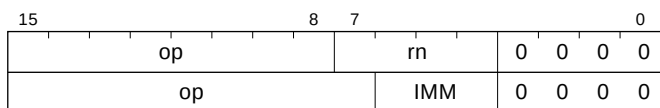


Operand: absolute (@aa:8)

Bit No.: register direct (Rm)

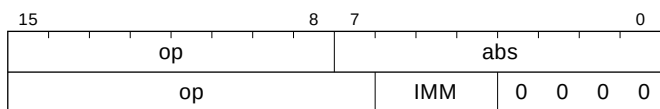
BAND, BOR, BXOR, BLD, BST

Operand: register direct (Rn)
Bit No.: immediate (#xx:3)



Operand: register indirect (@Rn)

Bit No.: immediate (#xx:3)



Operand: absolute (@aa:8)

Bit No.: immediate (#xx:3)

Legend:

op: Operation field
rm, rn: Register field
abs: Absolute address
IMM: Immediate data

Figure 2.7 Bit Manipulation Instruction Codes

2.5.6 Branching Instructions

Table 2.9 describes the branching instructions. Figure 2.8 shows their object code formats.

Table 2.9 Branching Instructions

Instruction	Size	Function
Bcc	—	Branches to the designated address if condition cc is true. The branching conditions are given below.
Mnemonic	Description	Condition
BRA (BT)	Always (true)	Always
BRN (BF)	Never (false)	Never
BHI	High	$C \vee Z = 0$
BLS	Low or same	$C \vee Z = 1$
BCC (BHS)	Carry clear (high or same)	$C = 0$
BCS (BLO)	Carry set (low)	$C = 1$
BNE	Not equal	$Z = 0$
BEQ	Equal	$Z = 1$
BVC	Overflow clear	$V = 0$
BVS	Overflow set	$V = 1$
BPL	Plus	$N = 0$
BMI	Minus	$N = 1$
BGE	Greater or equal	$N \oplus V = 0$
BLT	Less than	$N \oplus V = 1$
BGT	Greater than	$Z \vee (N \oplus V) = 0$
BLE	Less or equal	$Z \vee (N \oplus V) = 1$
JMP	—	Branches unconditionally to a specified address
BSR	—	Branches to a subroutine at a specified address
JSR	—	Branches to a subroutine at a specified address
RTS	—	Returns from a subroutine

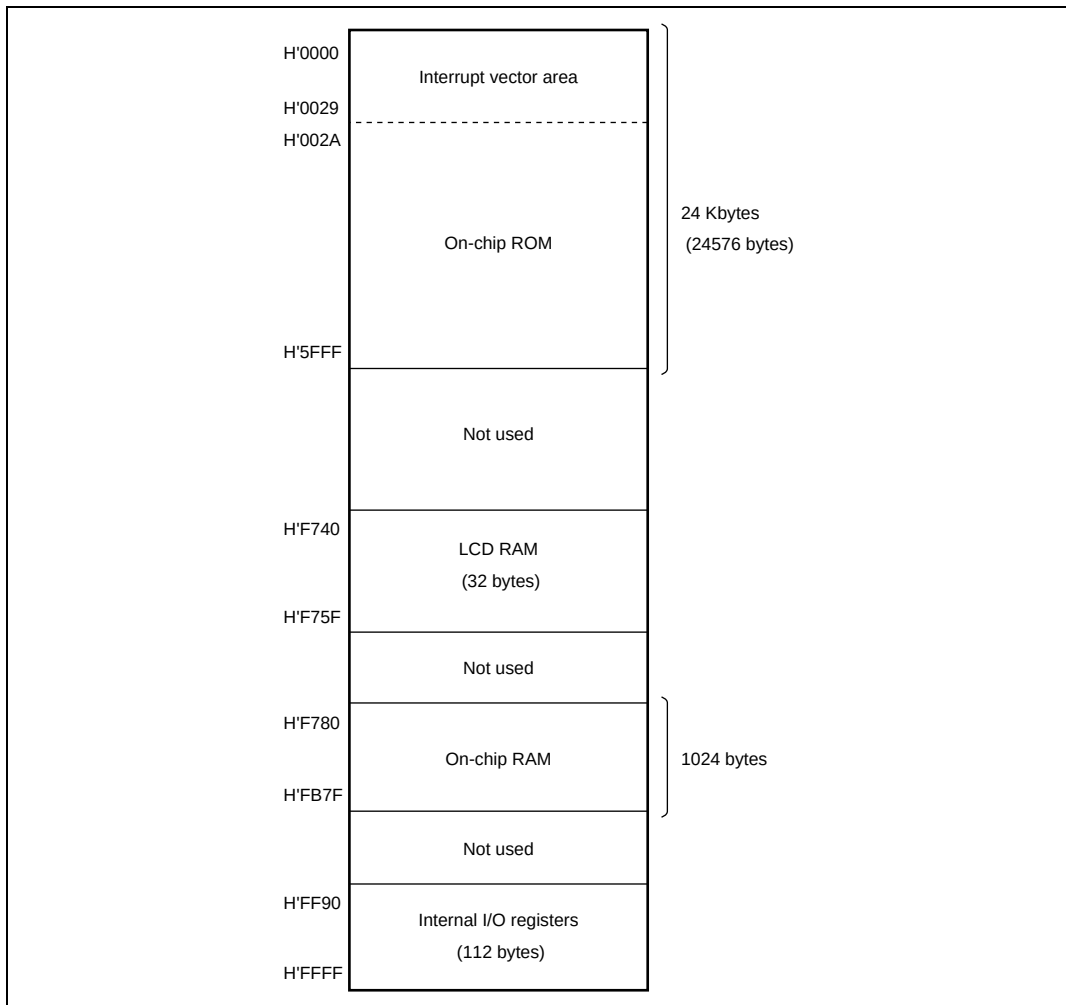


Figure 2.16 (2) H8/3823R, H8/38323, and H8/38423 Memory Map

Section 4 Clock Pulse Generators

4.1 Overview

Clock oscillator circuitry (CPG: clock pulse generator) is provided on-chip, including both a system clock pulse generator and a subclock pulse generator. The system clock pulse generator consists of a system clock oscillator and system clock dividers. The subclock pulse generator consists of a subclock oscillator circuit and a subclock divider.

4.1.1 Block Diagram

Figure 4.1 shows a block diagram of the clock pulse generators.

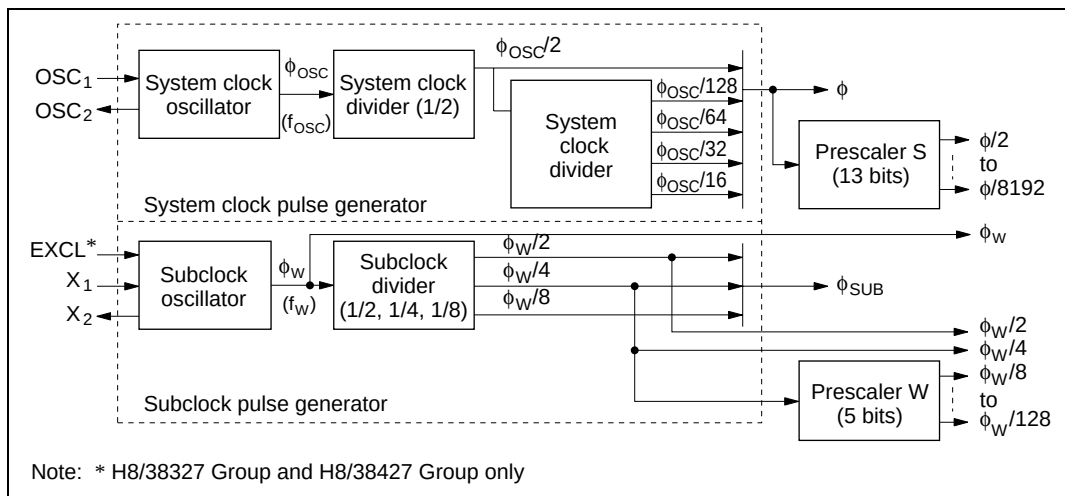


Figure 4.1 Block Diagram of Clock Pulse Generators

4.1.2 System Clock and Subclock

The basic clock signals that drive the CPU and on-chip peripheral modules are ϕ and ϕ_{SUB} . Four of the clock signals have names: ϕ is the system clock, ϕ_{SUB} is the subclock, ϕ_{OSC} is the oscillator clock, and ϕ_W is the watch clock.

The clock signals available for use by peripheral modules are $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$, $\phi/256$, $\phi/512$, $\phi/1024$, $\phi/2048$, $\phi/4096$, $\phi/8192$, ϕ_W , $\phi_W/2$, $\phi_W/4$, $\phi_W/8$, $\phi_W/16$, $\phi_W/32$, $\phi_W/64$, and $\phi_W/128$. The clock requirements differ from one module to another.

5.9 Module Standby Mode

5.9.1 Setting Module Standby Mode

Module standby mode is set for individual peripheral functions. All the on-chip peripheral modules can be placed in module standby mode. When a module enters module standby mode, the system clock supply to the module is stopped and operation of the module halts. This state is identical to standby mode.

Module standby mode is set for a particular module by setting the corresponding bit to 0 in clock stop register 1 (CKSTPR1) or clock stop register 2 (CKSTPR2). (See table 5.5.)

5.9.2 Clearing Module Standby Mode

Module standby mode is cleared for a particular module by setting the corresponding bit to 1 in clock stop register 1 (CKSTPR1) or clock stop register 2 (CKSTPR2). (See table 5.5.)

Following a reset, clock stop register 1 (CKSTPR1) and clock stop register 2 (CKSTPR2) are both initialized to H'FF.

6.10.8 Programmer Mode Transition Time

Commands cannot be accepted during the oscillation stabilization period or the programmer mode setup time. After the programmer mode setup time, a transition is made to memory read mode.

Table 6.23 Stipulated Transition Times to Command Wait State

Item	Symbol	Min	Max	Unit	Notes
Oscillation stabilization time(crystal oscillator)	T_{osc1}	10	—	ms	Figure 6.20
Oscillation stabilization time(ceramic oscillator)	T_{osc1}	5	—	ms	
Programmer mode setup time	T_{bmV}	10	—	ms	
Vcc hold time	T_{dwn}	0	—	ms	

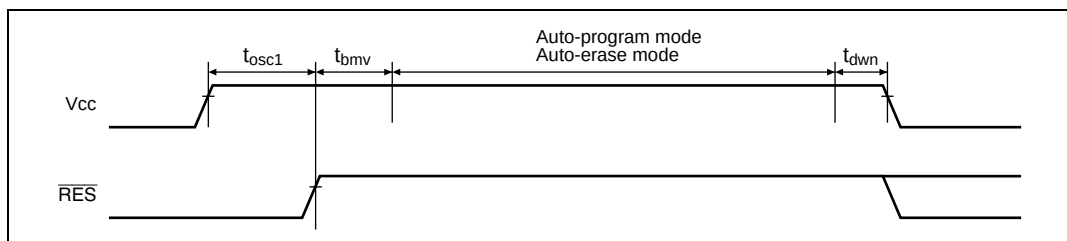


Figure 6.20 Oscillation Stabilization Time, Boot Program Transfer Time, and Power-Down Sequence

6.10.9 Notes on Memory Programming

1. When performing programming using programmer mode on a chip that has been programmed/erased in an on-board programming mode, auto-erasing is recommended before carrying out auto-programming.
2. The flash memory is initially in the erased state when the device is shipped by Renesas Technology. For other chips for which the erasure history is unknown, it is recommended that auto-erasing be executed to check and supplement the initialization (erase) level.

2. Input Capture Register GF (ICRGF)

Bit	7	6	5	4	3	2	1	0
	ICRGF7	ICRGF6	ICRGF5	ICRGF4	ICRGF3	ICRGF2	ICRGF1	ICRGF0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

ICRGF is an 8-bit read-only register. When a falling edge of the input capture input signal is detected, the current TCG value is transferred to ICRGF. If IIEGS in TMG is 1 at this time, IRRTG is set to 1 in IRR2, and if IENTG in IENR2 is 1, an interrupt request is sent to the CPU.

For details of the interrupt, see section 3.3, Interrupts.

To ensure dependable input capture operation, the pulse width of the input capture input signal must be at least 2ϕ or $2\phi_{\text{SUB}}$ (when the noise canceler is not used).

ICRGF is initialized to H'00 upon reset.

3. Input Capture Register GR (ICRGR)

Bit	7	6	5	4	3	2	1	0
	ICRGR7	ICRGR6	ICRGR5	ICRGR4	ICRGR3	ICRGR2	ICRGR1	ICRGR0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R

ICRGR is an 8-bit read-only register. When a rising edge of the input capture input signal is detected, the current TCG value is transferred to ICRGR. If IIEGS in TMG is 1 at this time, IRRTG is set to 1 in IRR2, and if IENTG in IENR2 is 1, an interrupt request is sent to the CPU.

For details of the interrupt, see section 3.3, Interrupts.

To ensure dependable input capture operation, the pulse width of the input capture input signal must be at least 2ϕ or $2\phi_{\text{SUB}}$ (when the noise canceler is not used).

ICRGR is initialized to H'00 upon reset.

5. TGC Clear Timing

TCG can be cleared by the rising edge, falling edge, or both edges of the input capture input signal.

Figure 9.14 shows the timing for clearing by both edges.

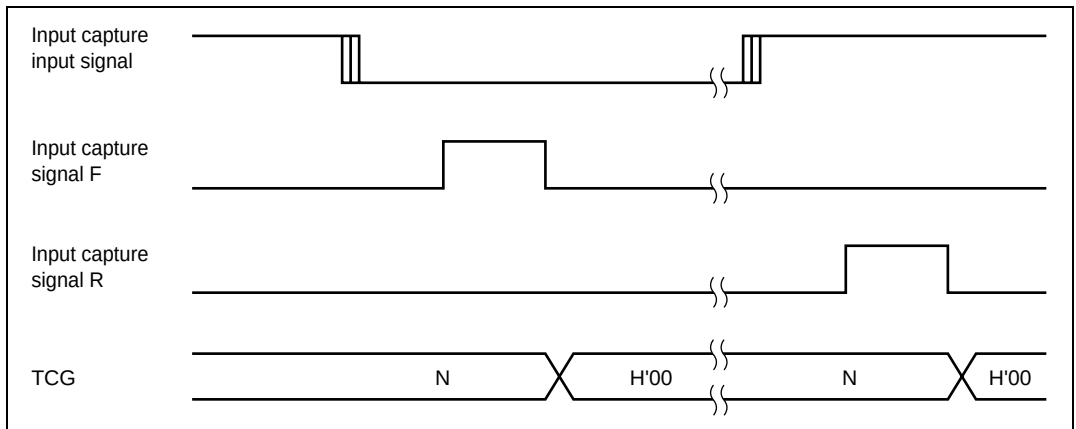
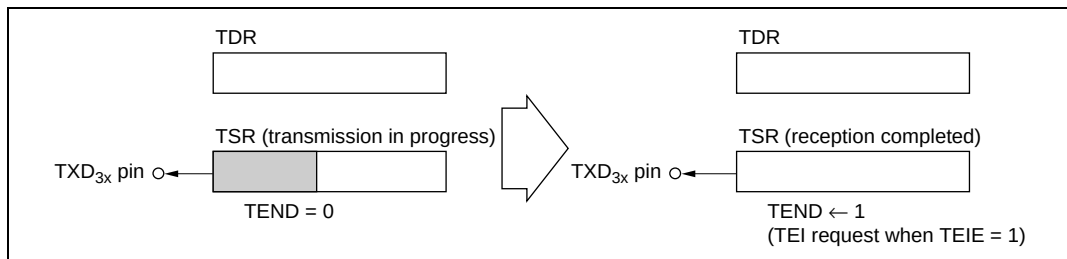
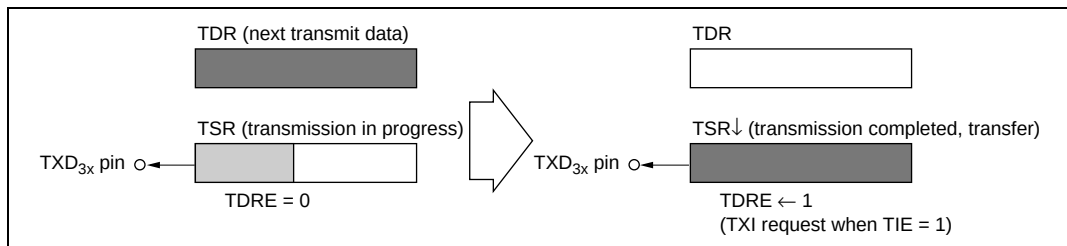
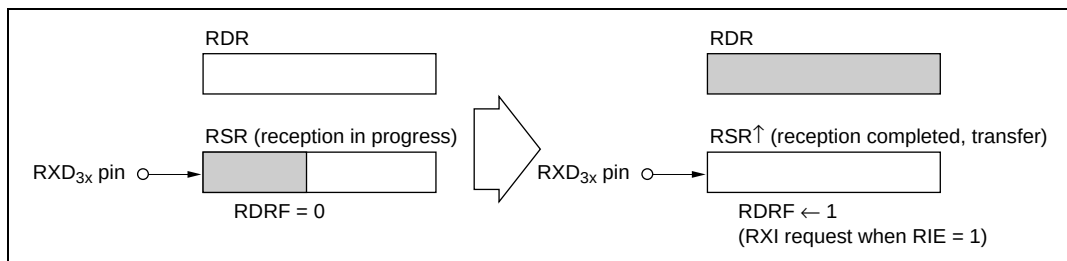
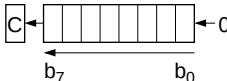
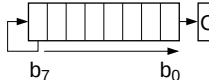
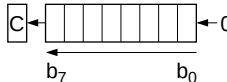
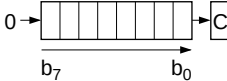
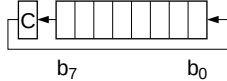


Figure 9.14 TCG Clear Timing



Item	Symbol	Applicable Pins	Values			Unit	Test Condition	Notes
			Min	Typ	Max			
Input low voltage	V_{IL}	$\overline{RES}$, WKP_0 to WKP_7 , $\overline{IRQ_0}$ to $\overline{IRQ_4}$, $AEVL$, $AEVH$, $TMIC$, $TMIF$, $TMIG$ SCK_{31} , SCK_{32} , $ADTRG$	-0.3	—	$0.2 V_{CC}$	V	$V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$	
			-0.3	—	$0.1 V_{CC}$		Except the above	
		RXD_{31} , RXD_{32} , UD	-0.3	—	$0.3 V_{CC}$	V	$V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$	
			-0.3	—	$0.2 V_{CC}$		Except the above	
		OSC_1	-0.3	—	0.2		When internal step-down circuit is used.	
			-0.3	—	$0.2 V_{CC}$	V	$V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$	
			-0.3	—	$0.1 V_{CC}$		Except the above	
		X_1	-0.3	—	$0.1 V_{CC}$	V	$V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$	
		$P1_0$ to $P1_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3 , PB_0 to PB_7	-0.3	—	$0.3 V_{CC}$	V	$V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$	
			-0.3	—	$0.2 V_{CC}$		Except the above	
Output high voltage	V_{OH}	$P1_0$ to $P1_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$	$V_{CC} - 1.0$	—	—	V	$V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$ $-I_{OH} = 1.0 \text{ mA}$	
		$P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	$V_{CC} - 0.5$	—	—		$V_{CC} = 4.0 \text{ V to } 5.5 \text{ V}$ $-I_{OH} = 0.5 \text{ mA}$	
			$V_{CC} - 0.3$	—	—		$-I_{OH} = 0.1 \text{ mA}$	

Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (bytes)								Condition Code						No. of States	
			#xx: 8/16	Rn	@Rn	@ (d:16, Rn)	@-Rn/@Rn+	@aa: 8/16	@ (d:8, PC)	@@aa	Implied	Condition Code						
												I	H	N	Z	V		C
MULXU.B Rs, Rd	B	$Rd8 \times Rs8 \rightarrow Rd16$		2								—	—	—	—	—	14	
DIVXU.B Rs, Rd	B	$Rd16 \div Rs8 \rightarrow Rd16$ (RdH: remainder, RdL: quotient)		2								—	—	(5)	(6)	—	14	
AND.B #xx:8, Rd	B	$Rd8 \wedge \#xx:8 \rightarrow Rd8$	2									—	—	↓	↓	0	2	
AND.B Rs, Rd	B	$Rd8 \wedge Rs8 \rightarrow Rd8$		2								—	—	↓	↓	0	2	
OR.B #xx:8, Rd	B	$Rd8 \vee \#xx:8 \rightarrow Rd8$	2									—	—	↓	↓	0	2	
OR.B Rs, Rd	B	$Rd8 \vee Rs8 \rightarrow Rd8$		2								—	—	↓	↓	0	2	
XOR.B #xx:8, Rd	B	$Rd8 \oplus \#xx:8 \rightarrow Rd8$	2									—	—	↓	↓	0	2	
XOR.B Rs, Rd	B	$Rd8 \oplus Rs8 \rightarrow Rd8$		2								—	—	↓	↓	0	2	
NOT.B Rd	B	$\overline{Rd} \rightarrow Rd$		2								—	—	↓	↓	0	2	
SHAL.B Rd	B			2								—	—	↓	↓	↓	2	
SHAR.B Rd	B			2								—	—	↓	↓	0	↓	2
SHLL.B Rd	B			2								—	—	↓	↓	0	↓	2
SHLR.B Rd	B			2								—	—	0	↓	0	↓	2
ROTXL.B Rd	B			2								—	—	↓	↓	0	↓	2
ROTXR.B Rd	B			2								—	—	↓	↓	0	↓	2

TMA—Timer Mode Register A

H'B0

Timer A

Bit	7	6	5	4	3	2	1	0
	TMA7	TMA6	TMA5	—	TMA3	TMA2	TMA1	TMA0
Initial value	0	0	0	1	0	0	0	0
Read/Write	R/W	R/W	R/W	—	R/W	R/W	R/W	R/W

Internal clock select

TMA3	TMA2	TMA1	TMA0	Prescaler and Divider Ratio or Overflow Period		Function	
0	0	0	0	PSS	$\phi/8192$	Interval timer	
			1	PSS	$\phi/4096$		
		1	0	PSS	$\phi/2048$		
			1	PSS	$\phi/512$		
	1	0	0	PSS	$\phi/256$		
			1	PSS	$\phi/128$		
		1	0	PSS	$\phi/32$		
			1	PSS	$\phi/8$		
1	0	0	0	PSW	1 s	Time base (when using 32.768 kHz)	
			1	PSW	0.5 s		
		1	0	PSW	0.25 s		
			1	PSW	0.03125 s		
	1	0	0	PSW and TCA are reset			
			1				
		1	0				
			1				

Clock output select*

0	0	0	$\phi/32$
		1	$\phi/16$
	1	0	$\phi/8$
		1	$\phi/4$
1	0	0	$\phi_W/32$
		1	$\phi_W/16$
	1	0	$\phi_W/8$
		1	$\phi_W/4$

Note: * Values when the CWOS bit in CWOSR is cleared to 0.
 When the CWOS bit is set to 1, ϕ_W is output regardless of the value of bits TMA7 to TMA5.

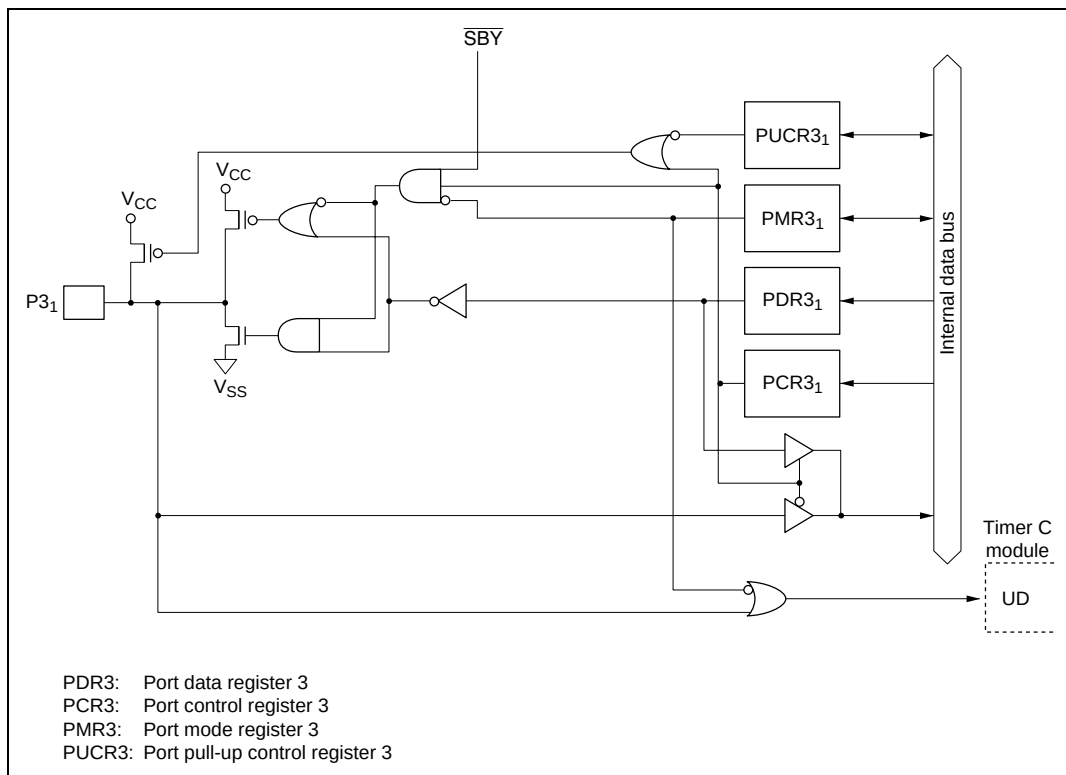


Figure C.2 (f-1) Port 3 Block Diagram (Pin P3₁, H8/3827R Group and H8/3827S Group)

C.7 Block Diagrams of Port 8

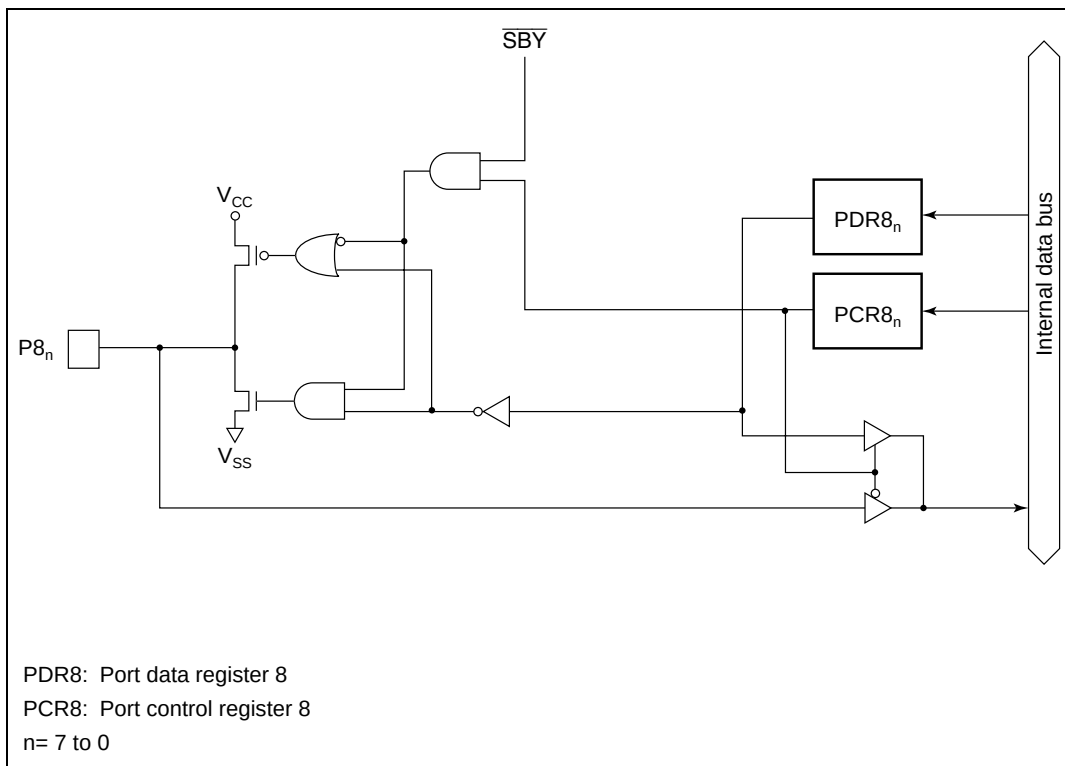


Figure C.7 Port 8 Block Diagram

Appendix D Port States in the Different Processing States

Table D.1 Port States Overview

Port	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
P1 ₇ to P1 ₀	High impedance	Retained	Retained	High impedance* ¹	Retained	Functions	Functions
P3 ₇ to P3 ₀	High impedance* ²	Retained	Retained	High impedance* ¹	Retained	Functions	Functions
P4 ₃ to P4 ₀	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
P5 ₇ to P5 ₀	High impedance	Retained	Retained	High impedance* ¹	Retained	Functions	Functions
P6 ₇ to P6 ₀	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
P7 ₇ to P7 ₀	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
P8 ₇ to P8 ₀	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
PA ₃ to PA ₀	High impedance	Retained	Retained	High impedance	Retained	Functions	Functions
PB ₇ to PB ₀	High impedance	High impedance	High impedance	High impedance	High impedance	High impedance	High impedance

Notes: 1. High level output when MOS pull-up is in on state.
 2. Reset output from P3₂ pin only (H8/3827R Group and H8/3827S Group).
 On-chip pull-up MOS turns on for pin P3₂ only (F-ZTAT Version of the H8/38327 Group and H8/38427 Group).