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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	55
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38327wv

Item	Page	Revision (See Manual for Details)
8.3.4 Pin States Table 8.7 Port 3 Pin States	211	Table and notes amended

Pins	Reset	Sleep	Subsleep	Standby	Watch	Subactive	Active
$P3_7$/AEVL $P3_6$/AEVH $P3_5$/TXD_{31} $P3_4$/RXD_{31} $P3_3$/SCK_{31}	High-impedance	Retains previous state	Retains previous state	High-impedance*1	Retains previous state	Functional	Functional
$P3_2$/$\overline{RESO}$*2	RESO output						
$P3_2$*4	Pull-up MOS on						
$P3_2$*3 $P3_1$/UD*2 $P3_1$/UD/EXCL*3*4 $P3_0$/PWM	High-impedance						

Notes: 1. A high-level signal is output when the MOS pull-up is in the on state.
2. Applies to H8/3827R Group and H8/3827S Group.
3. Applies to the mask ROM version of the H8/38327 Group and H8/38427 Group.
4. Applies to the F-ZTAT version of the H8/38327 Group and H8/38427 Group.

8.12.1 The Management of the Un-Use Terminal	236	Description amended • If an unused pin is an output pin, handle it in one of the following ways: — Set the output of the unused pin to high and pull it up to V_{CC} with an external resistor of approximately 100 kΩ. — Set the output of the unused pin to low and pull it down to Vss with an external resistor of approximately 100 kΩ.
C.2 Block Diagrams of Port 3 Figure C.2 (e-2) Port 3 Block Diagram (Pin $P3_2$ in the Mask ROM Version of the H8/38327 Group and H8/38427 Group)	593	Figure title amended
Figure C.2 (e-3) Port 3 Block Diagram (Pin $P3_2$ in the F-ZTAT Version of the H8/38327 Group and H8/38427 Group)	594	Newly added

2.5.5 Bit Manipulations

Table 2.8 describes the bit-manipulation instructions. Figure 2.7 shows their object code formats.

Table 2.8 Bit-Manipulation Instructions

Instruction	Size*	Function
BSET	B	1 → (<bit-No.> of <EAd>) Sets a specified bit in a general register or memory to 1. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BCLR	B	0 → (<bit-No.> of <EAd>) Clears a specified bit in a general register or memory to 0. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BNOT	B	~ (<bit-No.> of <EAd>) → (<bit-No.> of <EAd>) Inverts a specified bit in a general register or memory. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BTST	B	~ (<bit-No.> of <EAd>) → Z Tests a specified bit in a general register or memory and sets or clears the Z flag accordingly. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BAND	B	C ∧ (<bit-No.> of <EAd>) → C ANDs the C flag with a specified bit in a general register or memory, and stores the result in the C flag.
BIAND	B	C ∧ [~ (<bit-No.> of <EAd>)] → C ANDs the C flag with the inverse of a specified bit in a general register or memory, and stores the result in the C flag. The bit number is specified by 3-bit immediate data.
BOR	B	C ∨ (<bit-No.> of <EAd>) → C ORs the C flag with a specified bit in a general register or memory, and stores the result in the C flag.
BIOR	B	C ∨ [~ (<bit-No.> of <EAd>)] → C ORs the C flag with the inverse of a specified bit in a general register or memory, and stores the result in the C flag. The bit number is specified by 3-bit immediate data.

Instruction	Size*	Function
BXOR	B	C ⊕ (<bit-No.> of <EAd>) → C XORs the C flag with a specified bit in a general register or memory, and stores the result in the C flag.
BIXOR	B	C ⊕ [~(<bit-No.> of <EAd>)] → C XORs the C flag with the inverse of a specified bit in a general register or memory, and stores the result in the C flag. The bit number is specified by 3-bit immediate data.
BLD	B	(<bit-No.> of <EAd>) → C Copies a specified bit in a general register or memory to the C flag.
BILD	B	~ (<bit-No.> of <EAd>) → C Copies the inverse of a specified bit in a general register or memory to the C flag. The bit number is specified by 3-bit immediate data.
BST	B	C → (<bit-No.> of <EAd>) Copies the C flag to a specified bit in a general register or memory.
BIST	B	~ C → (<bit-No.> of <EAd>) Copies the inverse of the C flag to a specified bit in a general register or memory. The bit number is specified by 3-bit immediate data.

Note: * Size: Operand size
B: Byte

Certain precautions are required in bit manipulation. See section 2.9.2, Notes on Bit Manipulation, for details.

5. Port Mode Register 2 (PMR2)

Bit	7	6	5	4	3	2	1	0
	EXCL	—	—	—	—	—	—	—
Initial value	0	1	0	1	1	0	0	0
Read/Write	R/W	R	R/W	R	R	R/W	R/W	R/W

PMR2 is an 8-bit read/write register that controls external clock input to pin $P3_1$.

Upon reset, PMR2 is initialized to H'58. The information on this register applies to the H8/38327 Group and H8/38427 Group.

Bit 7: $P3_1$/UD/EXCL pin function switch (EXCL)

This bit selects whether pin $P3_1$/UD/EXCL is used as $P3_1$/UD or as EXCL. When the pin is used as EXCL an external clock should be input to it. See section 4, Clock Pulse Generators, for a connection example.

Bit 7 EXCL	Description	
0	Functions as $P3_1$/UD I/O pin	(initial value)
1	Functions as EXCL input pin	

Bit 6: Reserved bit

Bit 6 is a reserved bit. It is always read as 1 and cannot be modified.

Bit 5: Reserved bit

Bit 5 is a readable/writable reserved bit.

Bits 4 and 3: Reserved bits

Bits 4 and 3 are reserved bits. They are always read as 1 and cannot be modified.

Bits 2 to 0: Reserved bits

Bits 2 to 0 are readable/writable reserved bits.

Bit 5: Parity enable (PE)

Bit 5 selects whether a parity bit is to be added during transmission and checked during reception in asynchronous mode. In synchronous mode parity bit addition and checking is not performed, irrespective of the bit 5 setting.

Bit 5 PE	Description	
0	Parity bit addition and checking disabled*2	(initial value)
1	Parity bit addition and checking enabled*1*2	

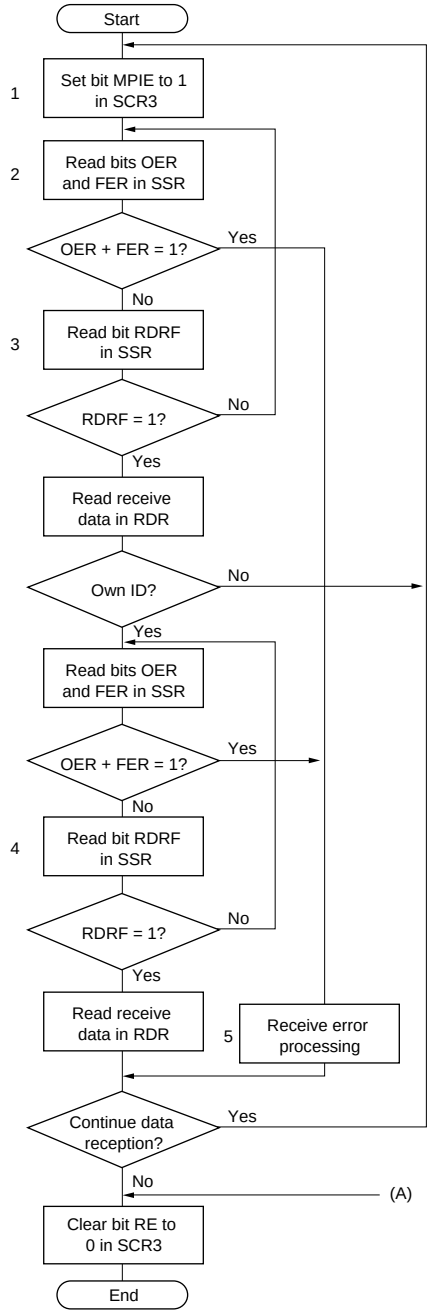
Notes: 1. When PE is set to 1, even or odd parity, as designated by bit PM, is added to transmit data before it is sent, and the received parity bit is checked against the parity designated by bit PM.
2. For the case where 5-bit data is selected, see table 10.11.

Bit 4: Parity mode (PM)

Bit 4 selects whether even or odd parity is to be used for parity addition and checking. The PM bit setting is only valid in asynchronous mode when bit PE is set to 1, enabling parity bit addition and checking. The PM bit setting is invalid in synchronous mode, and in asynchronous mode if parity bit addition and checking is disabled.

Bit 4 PM	Description	
0	Even parity*1	(initial value)
1	Odd parity*2	

Notes: 1. When even parity is selected, a parity bit is added in transmission so that the total number of 1 bits in the transmit data plus the parity bit is an even number; in reception, a check is carried out to confirm that the number of 1 bits in the receive data plus the parity bit is an even number.
2. When odd parity is selected, a parity bit is added in transmission so that the total number of 1 bits in the transmit data plus the parity bit is an odd number; in reception, a check is carried out to confirm that the number of 1 bits in the receive data plus the parity bit is an odd number.



1. Set bit MPIE to 1 in SCR3.
2. Read bits OER and FER in the serial status register (SSR) to determine if there is an error. If a receive error has occurred, execute receive error processing.
3. Read SSR and check that bit RDRF is set to 1. If it is, read the receive data in RDR and compare it with this receiver's own ID. If the ID is not this receiver's, set bit MPIE to 1 again. When the RDR data is read, bit RDRF is cleared to 0 automatically.
4. Read SSR and check that bit RDRF is set to 1, then read the data in RDR.
5. If a receive error has occurred, read bits OER and FER in SSR to identify the error, and after carrying out the necessary error processing, ensure that bits OER and FER are both cleared to 0. Reception cannot be resumed if either of these bits is set to 1. In the case of a framing error, a break can be detected by reading the value of the RXD_{3x} pin.

Figure 10.19 Example of Multiprocessor Data Reception Flowchart

Bit 7: Clock select (CKS)

Bit 7 sets the A/D conversion speed.

Bit 7		Conversion Time (Active (High-Speed) Mode)*	
CKS	**Conversion Period**	**ϕ = 1 MHz**	**ϕ = 5 MHz**
0	62/ϕ (initial value)	62 µs	12.4 µs
1	31/ϕ	31 µs	—

Note: * For information on conversion time settings for which operation is guaranteed, see section 15, Electrical Characteristics.

Bit 6: External trigger select (TRGE)

Bit 6 enables or disables the start of A/D conversion by external trigger input.

Bit 6 TRGE	Description	
0	Disables start of A/D conversion by external trigger	(initial value)
1	Enables start of A/D conversion by rising or falling edge of external trigger at pin $\overline{\text{ADTRG}}$*	

Note: * The external trigger ($\overline{\text{ADTRG}}$) edge is selected by bit IEG4 of IEGR. See 1. IRQ edge select register (IEGR) in section 3.3.2 for details.

Bits 5 and 4: Reserved bits

Bits 5 and 4 are reserved; they are always read as 1, and cannot be modified.

Bits 3 to 0: Channel select (CH3 to CH0)

Bits 3 to 0 select the analog input channel.

The channel selection should be made while bit ADSF is cleared to 0.

Bit 4: Expansion signal select (SGX)

Bit 4 selects whether the SEG_{32}/CL_1, SEG_{31}/CL_2, SEG_{30}/DO, and SEG_{29}/M pins are used as segment pins (SEG_{32} to SEG_{29}) or as segment external expansion pins (CL_1, CL_2, DO, and M).

In the H8/38327 Group and H8/38427 Group this bit should be left at its initial value and not written to. Changing the value of this bit may prevent the SEG/COM signal from operating normally.

Bit 4 SGX	Description	
0	Pins SEG_{32} to SEG_{29}*	(initial value)
1	Pins CL_1, CL_2, DO, M	

Note: * These pins function as ports when the setting of SGS3 to SGS0 is 0000 or 0001.

Bits 3 to 0: Segment driver select 3 to 0 (SGS3 to SGS0)

Bits 3 to 0 select the segment drivers to be used. The SGX = 0 setting is selected on the H8/38327 and H8/38427.

					Function of Pins SEG_{32} to SEG_1				
Bit 4 SGX	Bit 3 SGS3	Bit 2 SGS2	Bit 1 SGS1	Bit 0 SGS0	SEG_{32} to SEG_{25}	SEG_{24} to SEG_{17}	SEG_{16} to SEG_9	SEG_8 to SEG_1	Notes
0	0	0	0	0	Port	Port	Port	Port	(initial value)
	0	0	0	1	Port	Port	Port	Port	
	0	0	1	*	SEG	Port	Port	Port	
	0	1	0	*	SEG	SEG	Port	Port	
	0	1	1	*	SEG	SEG	SEG	Port	
	1	*	*	*	SEG	SEG	SEG	SEG	
1	0	0	0	0	Port*1	Port	Port	Port	
	*	*	*	*	Setting prohibited				

*: Don't care

Note: 1. SEG_{32} to SEG_{29} are external expansion pins.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Reference Figure
Oscillation stabilization time	t_{rc}	X_1, X_2	—	—	2.0	s		
External clock high width	t_{CPH}	OSC_1	25	—	—	ns	V_{CC} = 4.5 V to 5.5 V	Figure 15.1 *2
			40	—	—		V_{CC} = 2.7 V to 5.5 V	Figure 15.1
			100	—	—		V_{CC} = 1.8 V to 5.5 V	
		X_1	—	15.26 or 13.02	—	µs		
External clock low width	t_{CPL}	OSC_1	25	—	—	ns	V_{CC} = 4.5 V to 5.5 V	Figure 15.1 *2
			40	—	—		V_{CC} = 2.7 V to 5.5 V	Figure 15.1
			100	—	—		V_{CC} = 1.8 V to 5.5 V	
		X_1	—	15.26 or 13.02	—	µs		
External clock rise time	t_{CPr}	OSC_1	—	—	6	ns	V_{CC} = 4.5 V to 5.5 V	Figure 15.1 *2
			—	—	10		V_{CC} = 2.7 V to 5.5 V	Figure 15.1
			—	—	25		V_{CC} = 1.8 V to 5.5 V	
		X_1	—	—	55.0	ns		
External clock fall time	t_{CPf}	OSC_1	—	—	6	ns	V_{CC} = 4.5 V to 5.5 V	Figure 15.1 *2
			—	—	10		V_{CC} = 2.7 V to 5.5 V	Figure 15.1
			—	—	25		V_{CC} = 1.8 V to 5.5 V	
		X_1	—	—	55.0	ns		
Pin $\overline{RES}$ low width	t_{REL}	$\overline{RES}$	10	—	—	t_{cyc}		Figure 15.2

15.5 H8/3827S Group Absolute Maximum Ratings

Table 15.15 lists the absolute maximum ratings.

Table 15.15 Absolute Maximum Ratings

Item		Symbol	Value	Unit	Notes
Power supply voltage		V_{CC}	–0.3 to +4.3	V	*1
Analog power supply voltage		AV_{CC}	–0.3 to +4.3	V	
Input voltage	Ports other than Port B	V_{in}	–0.3 to V_{CC} +0.3	V	
	Port B	AV_{in}	–0.3 to AV_{CC} +0.3	V	
Operating temperature		T_{opr}	–20 to +75 (Regular specifications)	°C	
			–40 to +85 (wide-range specifications)		
			+75 (products shipped as chips)*2		
Storage temperature		T_{stg}	–55 to +125	°C	

Notes: 1. Permanent damage may occur to the chip if maximum ratings are exceeded. Normal operation should be under the conditions specified in Electrical Characteristics. Exceeding these values can result in incorrect operation and reduced reliability.
2. Power may be applied when the temperature is between –20 and –75°C.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Sleep mode current consumption	I_{SLEEP}	V_{CC}	—	0.5	—	mA	V_{CC} = 2.7 V, f_{OSC} = 2 MHz	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.8	—			*2 *3 *4 Approx. max. value = 1.1 × Typ.
			—	0.7	—		V_{CC} = 5 V, f_{OSC} = 2 MHz	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	1.2	—			*2 *3 *4 Approx. max. value = 1.1 × Typ.
			—	1.1	—		V_{CC} = 5 V, f_{OSC} = 4 MHz	*1 *3 *4 Approx. max. value = 1.1 × Typ.
			—	1.6	—			*2 *3 *4
			—	1.9	5.0		V_{CC} = 5 V, f_{OSC} = 10 MHz	*1 *3 *4
			—	2.6	5.0			*2 *3 *4
Subactive mode current consumption	I_{SUB}	V_{CC}	—	12	—	µA	V_{CC} = 2.7 V, LCD on, 32-kHz crystal resonator used (ϕ_{SUB} = ϕ_W/8)	*1 *3 *4 Reference value
			—	15	—			*2 *3 *4 Reference value
			—	18	50		V_{CC} = 2.7 V, LCD on, 32-kHz crystal resonator used (ϕ_{SUB} = ϕ_W/2)	*1 *3 *4
			—	30	50			*2 *3 *4

15.8.3 AC Characteristics

Table 15.24 lists the control signal timing and table 15.25 lists the serial interface timing.

Table 15.24 Control Signal Timing

V_{CC} = 2.7 V to 5.5 V, AV_{CC} = 2.7 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, unless otherwise specified

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Reference Figure
System clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	2.0	—	16.0	MHz		*3
			2.0	—	16.0		V_{CC} = 4.5 to 5.5 V	*4
			2.0	—	10.0		V_{CC} = 2.7 to 5.5 V	
OSC clock (ϕ_{OSC}) cycle time	t_{OSC}	OSC_1, OSC_2	62.5	—	500 (1000)	ns		Figure 15.1 *2 *3
			62.5	—	500 (1000)		V_{CC} = 4.5 to 5.5 V	Figure 15.1 *2 *4
			100	—	500 (1000)		V_{CC} = 2.7 to 5.5 V	
System clock (ϕ) cycle time	t_{cyc}		2	—	128	t_{OSC}		
			—	—	128	µs		
Subclock oscillation frequency	f_W	X_1, X_2, EXCL	—	32.768 or 38.4	—	kHz		
Watch clock (ϕ_W) cycle time	t_W	X_1, X_2, EXCL	—	30.5 or 26.0	—	µs		Figure 15.1
Subclock (ϕ_{SUB}) cycle time	t_{subcyc}		2	—	4	t_W		*1
Instruction cycle time			2	—	—	t_{cyc} t_{subcyc}		
Oscillation stabilization time	t_{rc}	OSC_1, OSC_2	—	20	45	µs	Ceramic resonator (V_{CC} = 3.0 to 5.5 V)	Figure 15.10
			—	80	—		Ceramic resonator other than above	
			—	0.8	2	ms	Crystal resonator	
			—	—	50		Other than above	
	t_{rc}	X_1, X_2	—	—	2.0	s		

Mnemonic	Operand Size	Operation	Addressing Mode/ Instruction Length (bytes)									Condition Code						No. of States
			#xx: 8/16	Rn	@Rn	@(d:16, Rn)	@–Rn/@Rn+	@aa: 8/16	@(d:8, PC)	@@aa	Implied	I	H	N	Z	V	C	
BTST #xx:3, Rd	B	(#xx:3 of Rd8) → Z		2								—	—	—	↕	—	—	2
BTST #xx:3, @Rd	B	(#xx:3 of @Rd16) → Z			4							—	—	—	↕	—	—	6
BTST #xx:3, @aa:8	B	(#xx:3 of @aa:8) → Z						4				—	—	—	↕	—	—	6
BTST Rn, Rd	B	(Rn8 of Rd8) → Z		2								—	—	—	↕	—	—	2
BTST Rn, @Rd	B	(Rn8 of @Rd16) → Z			4							—	—	—	↕	—	—	6
BTST Rn, @aa:8	B	(Rn8 of @aa:8) → Z						4				—	—	—	↕	—	—	6
BLD #xx:3, Rd	B	(#xx:3 of Rd8) → C		2								—	—	—	—	—	↕	2
BLD #xx:3, @Rd	B	(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↕	6
BLD #xx:3, @aa:8	B	(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↕	6
BILD #xx:3, Rd	B	(#xx:3 of Rd8) → C		2								—	—	—	—	—	↕	2
BILD #xx:3, @Rd	B	(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↕	6
BILD #xx:3, @aa:8	B	(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↕	6
BST #xx:3, Rd	B	C → (#xx:3 of Rd8)		2								—	—	—	—	—	—	2
BST #xx:3, @Rd	B	C → (#xx:3 of @Rd16)			4							—	—	—	—	—	—	8
BST #xx:3, @aa:8	B	C → (#xx:3 of @aa:8)						4				—	—	—	—	—	—	8
BIST #xx:3, Rd	B	$\overline{C}$ → (#xx:3 of Rd8)		2								—	—	—	—	—	—	2
BIST #xx:3, @Rd	B	$\overline{C}$ → (#xx:3 of @Rd16)			4							—	—	—	—	—	—	8
BIST #xx:3, @aa:8	B	$\overline{C}$ → (#xx:3 of @aa:8)						4				—	—	—	—	—	—	8
BAND #xx:3, Rd	B	C∧(#xx:3 of Rd8) → C		2								—	—	—	—	—	↕	2
BAND #xx:3, @Rd	B	C∧(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↕	6
BAND #xx:3, @aa:8	B	C∧(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↕	6
BIAND #xx:3, Rd	B	C∧($\overline{\text{#xx:3 of Rd8}}$) → C		2								—	—	—	—	—	↕	2
BIAND #xx:3, @Rd	B	C∧($\overline{\text{#xx:3 of @Rd16}}$) → C			4							—	—	—	—	—	↕	6
BIAND #xx:3, @aa:8	B	C∧($\overline{\text{#xx:3 of @aa:8}}$) → C						4				—	—	—	—	—	↕	6
BOR #xx:3, Rd	B	C∨(#xx:3 of Rd8) → C		2								—	—	—	—	—	↕	2
BOR #xx:3, @Rd	B	C∨(#xx:3 of @Rd16) → C			4							—	—	—	—	—	↕	6
BOR #xx:3, @aa:8	B	C∨(#xx:3 of @aa:8) → C						4				—	—	—	—	—	↕	6
BIOR #xx:3, Rd	B	C∨($\overline{\text{#xx:3 of Rd8}}$) → C		2								—	—	—	—	—	↕	2
BIOR #xx:3, @Rd	B	C∨($\overline{\text{#xx:3 of @Rd16}}$) → C			4							—	—	—	—	—	↕	6

PUCR6—Port Pull-Up Control Register 6 **H'E3** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	$PUCR6_7$	$PUCR6_6$	$PUCR6_5$	$PUCR6_4$	$PUCR6_3$	$PUCR6_2$	$PUCR6_1$	$PUCR6_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Port 6 input pull-up MOS control

0	Input pull-up MOS is off
1	Input pull-up MOS is on

Note: When the PCR6 specification is 0. (Input port specification)

PCR1—Port Control Register 1 **H'E4** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	$PCR1_7$	$PCR1_6$	$PCR1_5$	$PCR1_4$	$PCR1_3$	$PCR1_2$	$PCR1_1$	$PCR1_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 1 input/output select

0	Input pin
1	Output pin

PCR3—Port Control Register 3 **H'E6** **I/O ports**

Bit	7	6	5	4	3	2	1	0
	$PCR3_7$	$PCR3_6$	$PCR3_5$	$PCR3_4$	$PCR3_3$	$PCR3_2$	$PCR3_1$	$PCR3_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

Port 3 input/output select

0	Input pin
1	Output pin

IWPR—Wakeup Interrupt Request Register **H'F9** **System control**

Bit	7	6	5	4	3	2	1	0
	IWPF7	IWPF6	IWPF5	IWPF4	IWPF3	IWPF2	IWPF1	IWPF0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Wakeup interrupt request register

0	[Clearing condition] When IWPFn = 1, it is cleared by writing 0
1	[Setting condition] When pin $\overline{\text{WKP}}$n is designated for wakeup input and a falling edge is input at that pin

(n = 7 to 0)

Note: * All bits can only be written with 0, for flag clearing.

CKSTPR1—Clock Stop Register 1 **H'FA** **System control**

Bit	7	6	5	4	3	2	1	0
	—	S31CKSTP	S32CKSTP	ADCKSTP	TGCKSTP	TFCKSTP	TCCKSTP	TACKSTP
Initial value	1	1	1	1	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Timer A module standby mode control

0	Timer A is set to module standby mode
1	Timer A module standby mode is cleared

Timer C module standby mode control

0	Timer C is set to module standby mode
1	Timer C module standby mode is cleared

Timer F module standby mode control

0	Timer F is set to module standby mode
1	Timer F module standby mode is cleared

Timer G interrupt enable

0	Timer G is set to module standby mode
1	Timer G module standby mode is cleared

A/D converter module standby mode control

0	A/D converter is set to module standby mode
1	A/D converter module standby mode is cleared

SCI3-2 module standby mode control

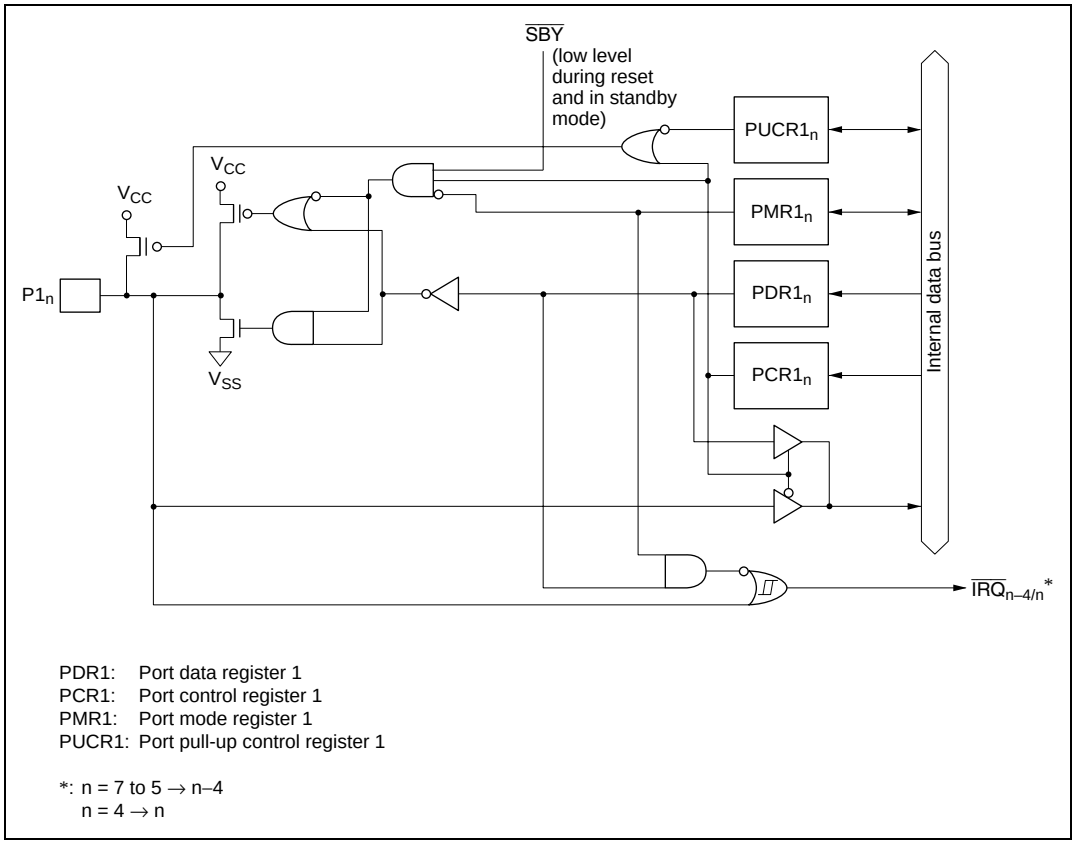
0	SCI3-2 is set to module standby mode
1	SCI3-2 module standby mode is cleared

SCI3-1 module standby mode control

0	SCI3-1 is set to module standby mode
1	SCI3-1 module standby mode is cleared

Appendix C I/O Port Block Diagrams

C.1 Block Diagrams of Port 1



PDR1: Port data register 1
PCR1: Port control register 1
PMR1: Port mode register 1
PUCR1: Port pull-up control register 1

*: n = 7 to 5 → n–4
n = 4 → n

Figure C.1 (a) Port 1 Block Diagram (Pins $P1_7$ to $P1_4$)

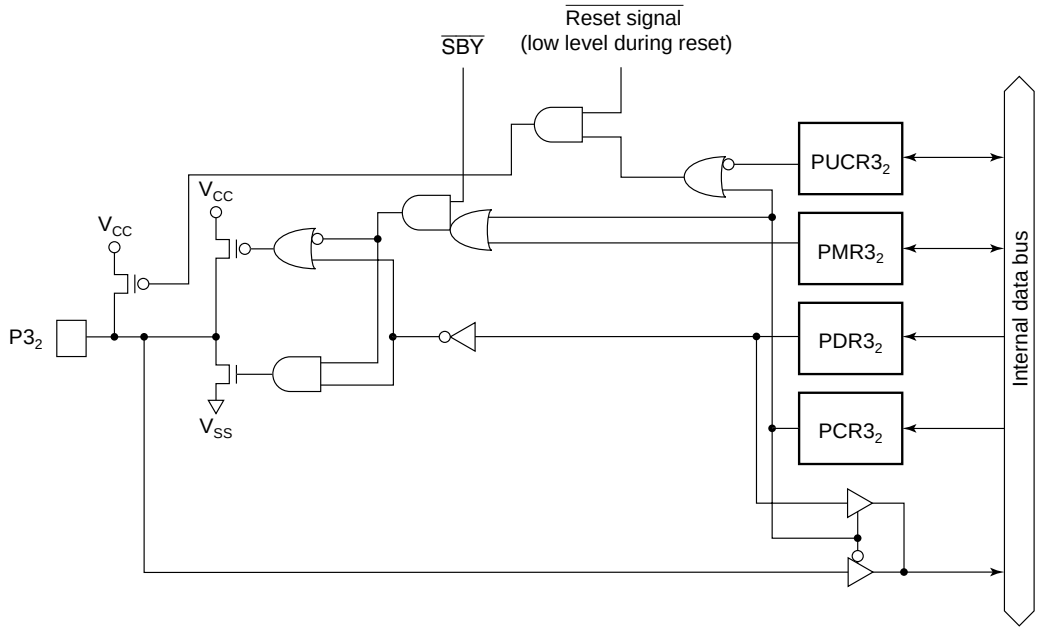
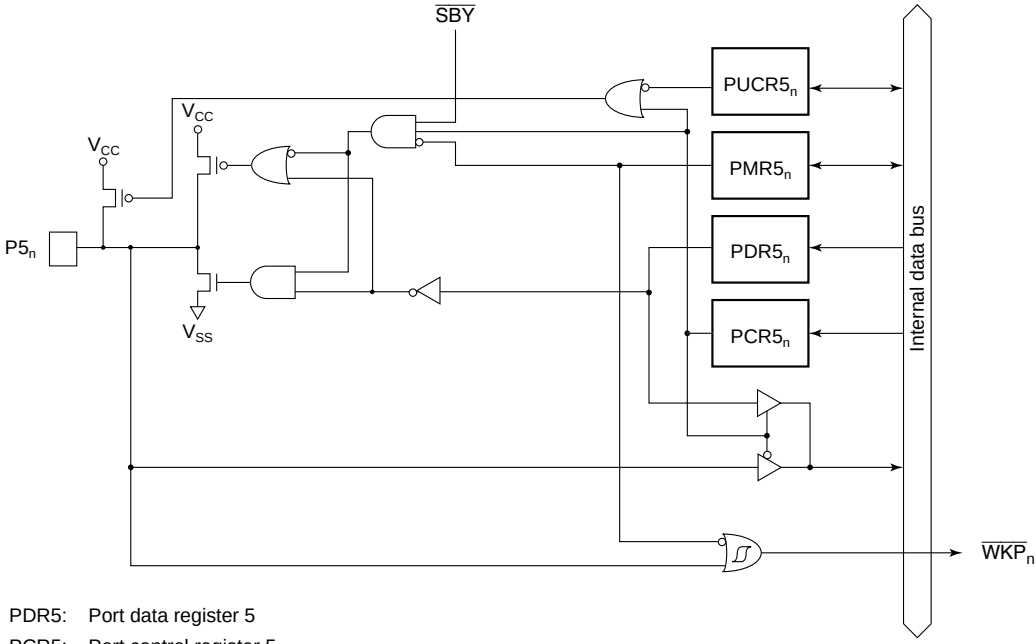


Figure C.2 (e-3) Port 3 Block Diagram (Pin P3$_2$ in the F-ZTAT Version of the H8/38327 Group and H8/38427 Group)

C.4 Block Diagram of Port 5



PDR5: Port data register 5
PCR5: Port control register 5
PMR5: Port mode register 5
PUCR5: Port pull-up control register 5
n = 7 to 0

Figure C.4 Port 5 Block Diagram