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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	55
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df38327wwv

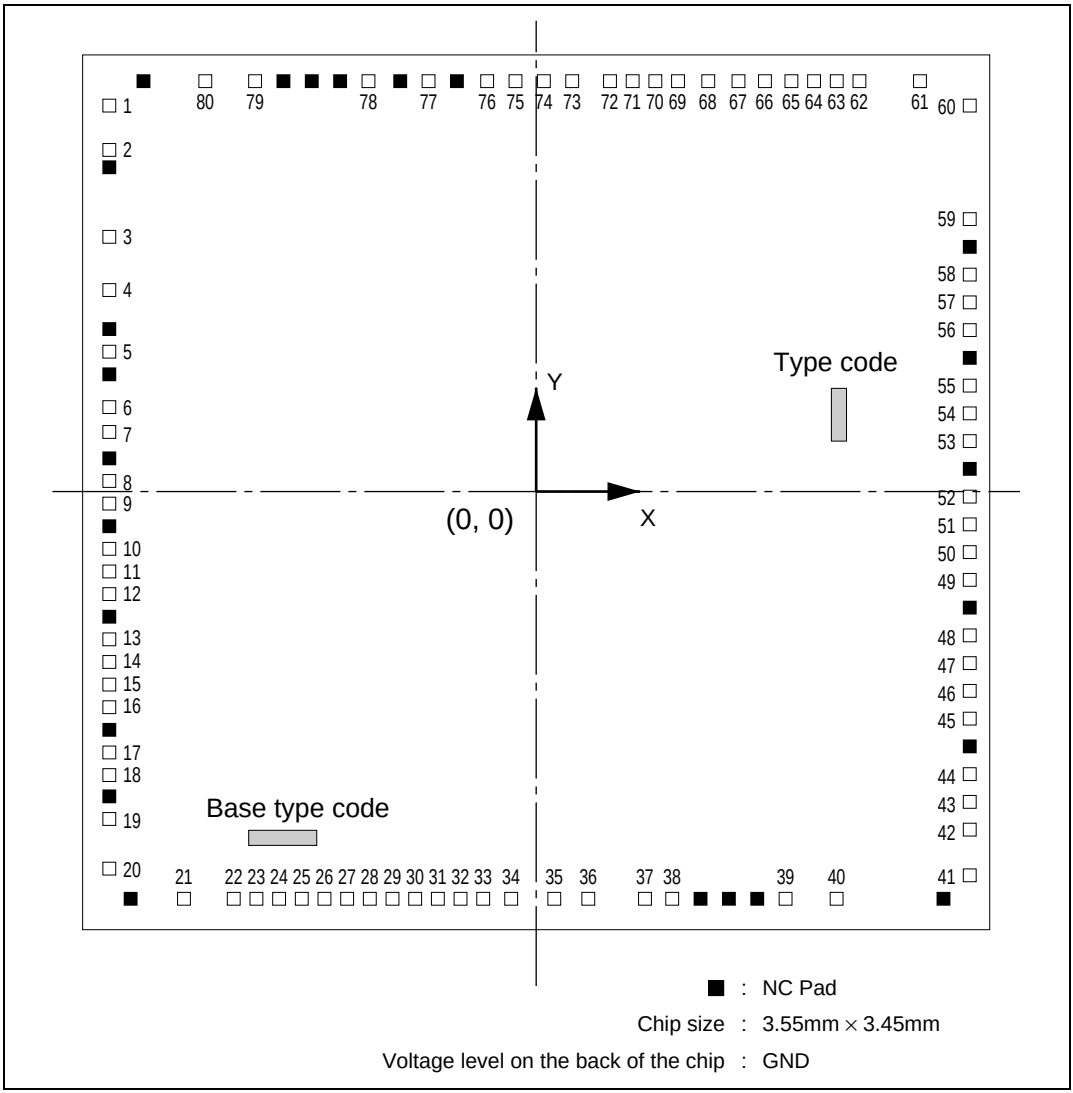


Figure 1.5 Bonding Pad Location Diagram of H8/3827S Group (Mask ROM Version) (Top View)

Type	Symbol	Pin No. FP-80A TFP-80C	Pin No. FP-80B	I/O	Name and Functions
A/D converter	AN7 to An0	1 80 to 74	3 to 1 80 to 76	Input	**Analog input channels 7 to 0:** These are analog data input channels to the A/D converter
	$\overline{\text{ADTRG}}$	14	16	Input	**A/D converter trigger input:** This is the external trigger input pin to the A/D converter
LCD controller/ driver	COM_4 to COM_1	33 to 36	35 to 38	Output	**LCD common output:** These are the LCD common output pins.
	SEG_{32} to SEG_1	68 to 37	70 to 39	Output	**LCD segment output:** These are the LCD segment output pins.
	CL_1	68	70	Output	**LCD latch clock:** This is the output pin for the segment external expansion display data latch clock. This function is not implemented in the H8/38327 Group and H8/38427 Group.
	CL_2	67	69	Output	**LCD shift clock:** This is the output pin for the segment external expansion display data shift clock. This function is not implemented in the H8/38327 Group and H8/38427 Group.
	DO	66	68	Output	**LCD serial data output:** This is the output pin for segment external expansion serial display data. This function is not implemented in the H8/38327 Group and H8/38427 Group.
	M	65	67	Output	**LCD alternation signal:** This is the output pin for the segment external expansion LCD alternation signal. This function is not implemented in the H8/38327 Group and H8/38427 Group.

Section 2 CPU

2.1 Overview

The H8/300L CPU has sixteen 8-bit general registers, which can also be paired as eight 16-bit registers. Its concise instruction set is designed for high-speed operation.

2.1.1 Features

Features of the H8/300L CPU are listed below.

- General-register architecture
  Sixteen 8-bit general registers, also usable as eight 16-bit general registers
- Instruction set with 55 basic instructions, including:
  — Multiply and divide instructions
  — Powerful bit-manipulation instructions
- Eight addressing modes
  — Register direct
  — Register indirect
  — Register indirect with displacement
  — Register indirect with post-increment or pre-decrement
  — Absolute address
  — Immediate
  — Program-counter relative
  — Memory indirect
- 64-Kbyte address space
- High-speed operation
  — All frequently used instructions are executed in two to four states
  — High-speed arithmetic and logic operations
  — 8- or 16-bit register-register add or subtract: 0.25 µs*
  — 8 × 8-bit multiply: 1.75 µs*
  — 16 ÷ 8-bit divide: 1.75 µs*
  Note: * These values are at ϕ = 8 MHz.
- Low-power operation modes
  SLEEP instruction for transfer to low-power operation

6.3.2 Programming Precautions

- Use the specified programming voltage and timing.

  The programming voltage in PROM mode (V_{PP}) is 12.5 V. Use of a higher voltage can permanently damage the chip. Be especially careful with respect to PROM programmer overshoot.

  Setting the PROM programmer to Renesas specifications for the HN27C101 will result in correct V_{PP} of 12.5 V.
- Make sure the index marks on the PROM programmer socket, socket adapter, and chip are properly aligned. If they are not, the chip may be destroyed by excessive current flow. Before programming, be sure that the chip is properly mounted in the PROM programmer.
- Avoid touching the socket adapter or chip while programming, since this may cause contact faults and write errors.
- Take care when setting the programming mode, as page programming is not supported.
- When programming with a PROM programmer, be sure to specify addresses from H'0000 to H'EDFF. If programming is inadvertently performed from H'EE00 onward, it may not be possible to continue PROM programming and verification. When programming, H'FF should be set as the data in address area H'EE00 to H'1FFFF.

6.6 Descriptions of Registers of the Flash Memory

6.6.1 Flash Memory Control Register 1 (FLMCR1)

Bit	7	6	5	4	3	2	1	0
	—	SWE	ESU	PSU	EV	PV	E	P
Initial value	0	0	0	0	0	0	0	0
Read/Write	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FLMCR1 is a register that makes the flash memory change to program mode, program-verify mode, erase mode, or erase-verify mode. For details on register setting, refer to section 6.8, Flash Memory Programming/Erasing. By setting this register, the flash memory enters program mode, erase mode, program-verify mode, or erase-verify mode. Read the data in the state that bits 6 to 0 of this register are cleared when using flash memory as normal built-in ROM.

Bit 7—Reserved

This bit is always read as 0 and cannot be modified.

Bit 6—Software Write Enable (SWE)

This bit is to set enabling/disabling of programming/enabling of flash memory (set when bits 5 to 0 and the EBR register are to be set).

Bit 6 SWE	Description
0	Programming/erasing is disabled. Other FLMCR1 register bits and all EBR bits cannot be set. (initial value)
1	Flash memory programming/erasing is enabled.

Bit 5—Erase Setup (ESU)

This bit is to prepare for changing to erase mode. Set this bit to 1 before setting the E bit to 1 in FLMCR1 (do not set SWE, PSU, EV, PV, E, and P bits at the same time).

Bit 5 ESU	Description
0	The erase setup state is cancelled (initial value)
1	The flash memory changes to the erase setup state. Set this bit to 1 before setting the E bit to 1 in FLMCR1.

Bit 6: $P1_6/\overline{IRQ_2}$ pin function switch (IRQ2)

This bit selects whether pin $P1_6/\overline{IRQ_2}$ is used as $P1_6$ or as $\overline{IRQ_2}$.

Bit 6 IRQ2	Description	
0	Functions as $P1_6$ I/O pin	(initial value)
1	Functions as $\overline{IRQ_2}$ input pin	

Note: Rising or falling edge sensing can be designated for $\overline{IRQ_2}$.

Bit 5: $P1_5/\overline{IRQ_1}$/TMIC pin function switch (IRQ1)

This bit selects whether pin $P1_5/\overline{IRQ_1}$/TMIC is used as $P1_5$ or as $\overline{IRQ_1}$/TMIC.

Bit 5 IRQ1	Description	
0	Functions as $P1_5$ I/O pin	(initial value)
1	Functions as $\overline{IRQ_1}$/TMIC input pin	

Note: Rising or falling edge sensing can be designated for $\overline{IRQ_1}$/TMIC.
For details of TMIC pin setting, see 1. Timer mode register C (TMC) in section 9.3.2.

Bit 4: $P1_4/\overline{IRQ_4}/\overline{ADTRG}$ pin function switch (IRQ4)

This bit selects whether pin $P1_4/\overline{IRQ_4}/\overline{ADTRG}$ is used as $P1_4$ or as $\overline{IRQ_4}/\overline{ADTRG}$.

Bit 4 IRQ4	Description	
0	Functions as $P1_4$ I/O pin	(initial value)
1	Functions as $\overline{IRQ_4}/\overline{ADTRG}$ input pin	

Note: For details of $\overline{ADTRG}$ pin setting, see section 12.3.2, Start of A/D Conversion by External Trigger Input.

8.5.2 Register Configuration and Description

Table 8.11 shows the port 5 register configuration.

Table 8.11 Port 5 Registers

Name	Abbr.	R/W	Initial Value	Address
Port data register 5	PDR5	R/W	H'00	H'FFD8
Port control register 5	PCR5	W	H'00	H'FFE8
Port pull-up control register 5	PUCR5	R/W	H'00	H'FFE2
Port mode register 5	PMR5	R/W	H'00	H'FFCC

1. Port Data Register 5 (PDR5)

Bit	7	6	5	4	3	2	1	0
	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR5 is an 8-bit register that stores data for port 5 pins $P5_7$ to $P5_0$. If port 5 is read while PCR5 bits are set to 1, the values stored in PDR5 are read, regardless of the actual pin states. If port 5 is read while PCR5 bits are cleared to 0, the pin states are read.

Upon reset, PDR5 is initialized to H'00.

2. Port Control Register 5 (PCR5)

Bit	7	6	5	4	3	2	1	0
	$PCR5_7$	$PCR5_6$	$PCR5_5$	$PCR5_4$	$PCR5_3$	$PCR5_2$	$PCR5_1$	$PCR5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCR5 is an 8-bit register for controlling whether each of the port 5 pins $P5_7$ to $P5_0$ functions as an input pin or output pin. Setting a PCR5 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. PCR5 and PDR5 settings are valid when the corresponding pins are designated for general-purpose input/output by PMR5 and bits SGS3 to SGS0 in LPCR.

Upon reset, PCR5 is initialized to H'00.

9.3.5 Usage Note

Note the following regarding the operation of timer C.

(1) Counting errors caused by external event input

Timer counter errors may occur under the following conditions.

Conditions

- An external event (TMIC) is used in subsleep mode.

Symptom

- The counter increments or decrements twice for a single external event input.

Approximate rate of occurrence

The approximate rate of occurrence in cases where the external event input is not synchronized with internal operation is defined by the following equation.

$$\text{Approximate rate of occurrence } P = 30 \text{ ns} / \text{tsubcyc}$$

For example, if tsubcyc = 61.06 µs (subclock ϕw/2), P = 0.0005 (0.05%). If 2,000 external event inputs occur, there is a likelihood that one of them will cause the counter to increment or decrement twice (+2 or –2).

The symptom described is caused by the internal circuit configuration of the device and therefore difficult to avoid. Therefore, it is not advisable to use the clock counter for applications requiring a high degree of accuracy.

4. Register Configuration

Table 9.20 shows the register configuration of the asynchronous event counter.

Table 9.20 Asynchronous Event Counter Registers

Name	Abbr.	R/W	Initial Value	Address
Event counter control/status register	ECCSR	R/W	H'00	H'FF95
Event counter H	ECH	R	H'00	H'FF96
Event counter L	ECL	R	H'00	H'FF97
Clock stop register 2	CKSTP2	R/W	H'FF	H'FFFB

9.7.2 Register Descriptions

1. Event Counter Control/Status Register (ECCSR)

Bit	7	6	5	4	3	2	1	0
	OVH	OVL	—	CH2	CUEH	CUEL	CRCH	CRCL
Initial Value	0	0	0	0	0	0	0	0
Read/Write	R/W*	R/W*	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Bits 7 and 6 can only be written with 0, for flag clearing.

ECCSR is an 8-bit read/write register that controls counter overflow detection, counter resetting, and halting of the count-up function.

ECCSR is initialized to H'00 upon reset.

Bit 5: Parity enable (PE)

Bit 5 selects whether a parity bit is to be added during transmission and checked during reception in asynchronous mode. In synchronous mode parity bit addition and checking is not performed, irrespective of the bit 5 setting.

Bit 5 PE	Description	
0	Parity bit addition and checking disabled*2	(initial value)
1	Parity bit addition and checking enabled*1*2	

Notes: 1. When PE is set to 1, even or odd parity, as designated by bit PM, is added to transmit data before it is sent, and the received parity bit is checked against the parity designated by bit PM.
2. For the case where 5-bit data is selected, see table 10.11.

Bit 4: Parity mode (PM)

Bit 4 selects whether even or odd parity is to be used for parity addition and checking. The PM bit setting is only valid in asynchronous mode when bit PE is set to 1, enabling parity bit addition and checking. The PM bit setting is invalid in synchronous mode, and in asynchronous mode if parity bit addition and checking is disabled.

Bit 4 PM	Description	
0	Even parity*1	(initial value)
1	Odd parity*2	

Notes: 1. When even parity is selected, a parity bit is added in transmission so that the total number of 1 bits in the transmit data plus the parity bit is an even number; in reception, a check is carried out to confirm that the number of 1 bits in the receive data plus the parity bit is an even number.
2. When odd parity is selected, a parity bit is added in transmission so that the total number of 1 bits in the transmit data plus the parity bit is an odd number; in reception, a check is carried out to confirm that the number of 1 bits in the receive data plus the parity bit is an odd number.

3. Data Transfer Operations

SCI3 initialization: Data transfer on SCI3 first of all requires that SCI3 be initialized as described in 10.3.2.3. SCI3 initialization, and shown in figure 10.5.

Transmitting: Figure 10.11 shows an example of a flowchart for data transmission. This procedure should be followed for data transmission after initializing SCI3.

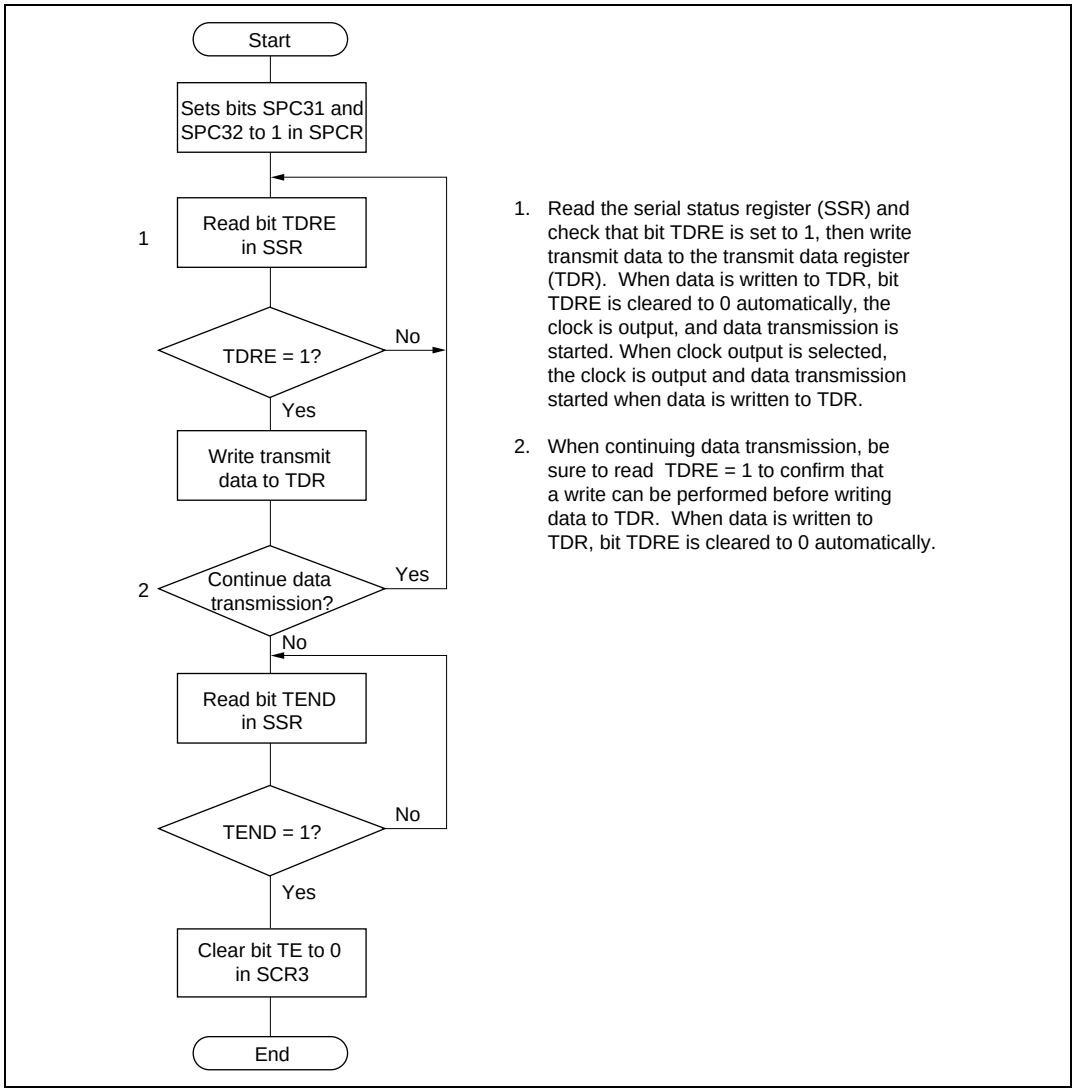


Figure 10.11 Example of Data Transmission Flowchart (Synchronous Mode)

7. Relation between RDR Reads and Bit RDRF

In a receive operation, SCI3 continually checks the RDRF flag. If bit RDRF is cleared to 0 when reception of one frame ends, normal data reception is completed. If bit RDRF is set to 1, this indicates that an overrun error has occurred.

When the contents of RDR are read, bit RDRF is cleared to 0 automatically. Therefore, if bit RDR is read more than once, the second and subsequent read operations will be performed while bit RDRF is cleared to 0. Note that, when an RDR read is performed while bit RDRF is cleared to 0, if the read operation coincides with completion of reception of a frame, the next frame of data may be read. This is illustrated in figure 10.22.

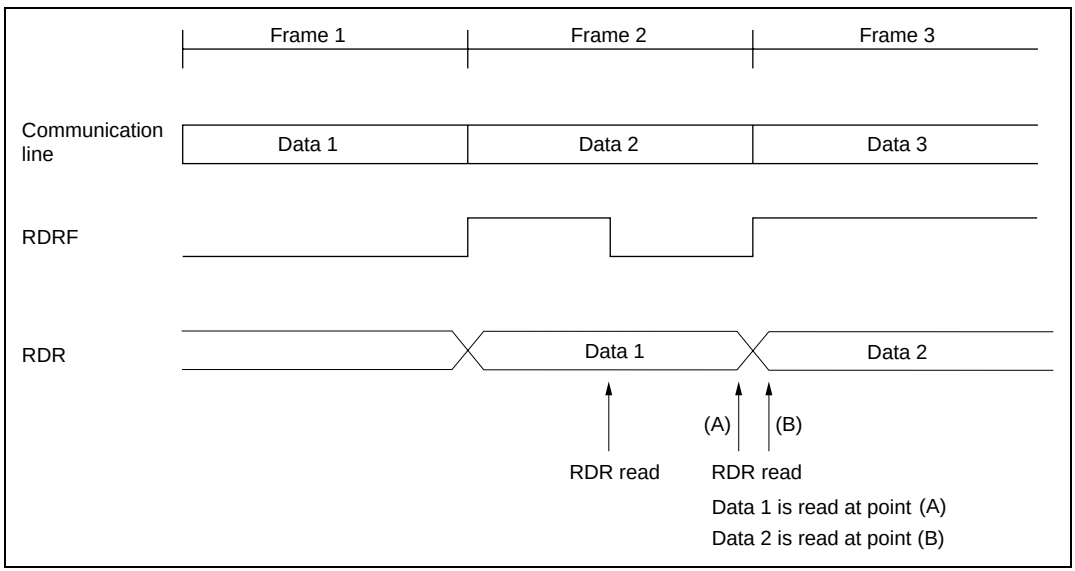


Figure 10.22 Relation between RDR Read Timing and Data

In this case, only a single RDR read operation (not two or more) should be performed after first checking that bit RDRF is set to 1. If two or more reads are performed, the data read the first time should be transferred to RAM, etc., and the RAM contents used. Also, ensure that there is sufficient margin in an RDR read operation before reception of the next frame is completed. To be precise in terms of timing, the RDR read should be completed before bit 7 is transferred in synchronous mode, or before the STOP bit is transferred in asynchronous mode.

12.3.3 A/D Converter Operation Modes

A/D converter operation modes are shown in table 12.3.

Table 12.3 A/D Converter Operation Modes

Operation Mode	Reset	Active	Sleep	Watch	Subactive	Subsleep	Standby	Module Standby
AMR	Reset	Functions	Functions	Held	Held	Held	Held	Held
ADSR	Reset	Functions	Functions	Held	Held	Held	Held	Held
ADRRH	Held*	Functions	Functions	Held	Held	Held	Held	Held
ADRRL	Held*	Functions	Functions	Held	Held	Held	Held	Held

Note: * Undefined in a power-on reset.

12.4 Interrupts

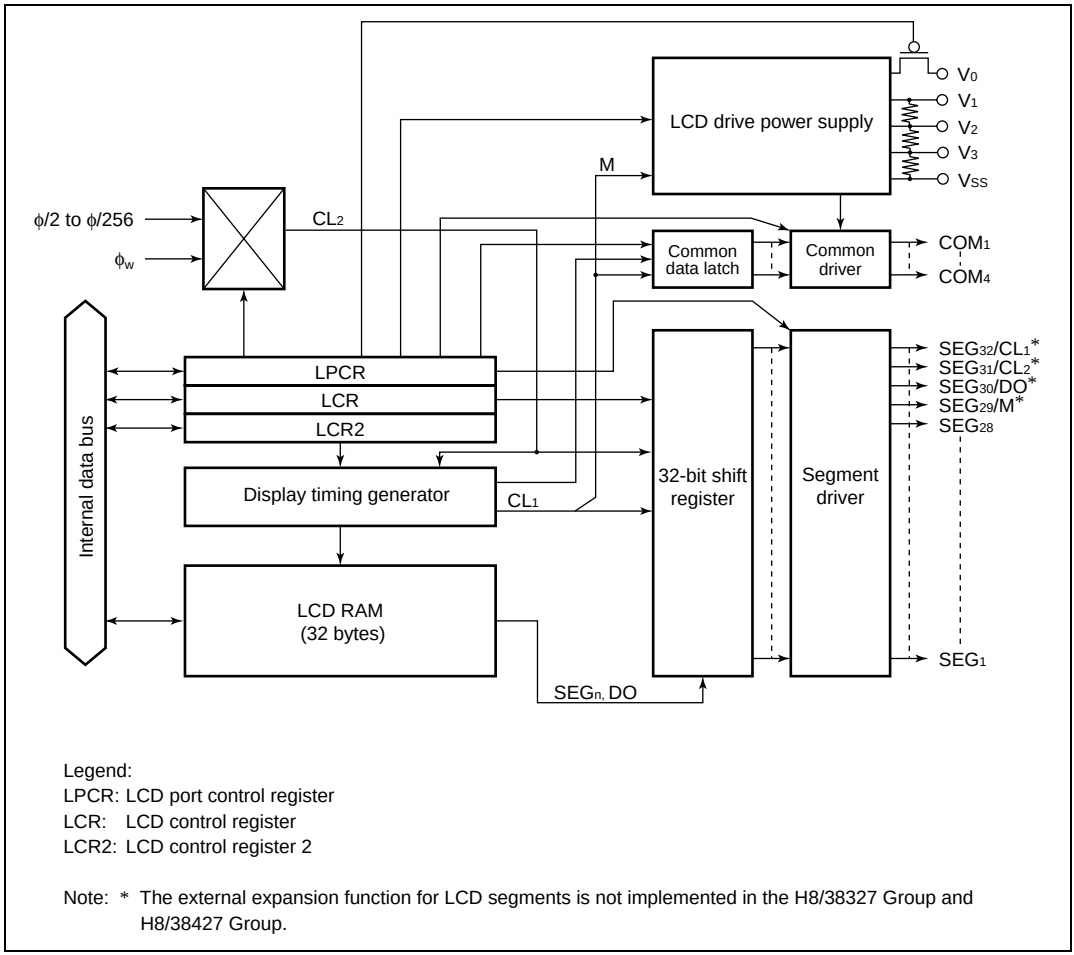
When A/D conversion ends (ADSF changes from 1 to 0), bit IRRAD in interrupt request register 2 (IRR2) is set to 1.

A/D conversion end interrupts can be enabled or disabled by means of bit IENAD in interrupt enable register 2 (IENR2).

For further details see section 3.3, Interrupts.

13.1.2 Block Diagram

Figure 13.1 shows a block diagram of the LCD controller/driver.



Legend:
LPCR: LCD port control register
LCR: LCD control register
LCR2: LCD control register 2

Note: * The external expansion function for LCD segments is not implemented in the H8/38327 Group and H8/38427 Group.

Figure 13.1 Block Diagram of LCD Controller/Driver

13.3.3 Luminance Adjustment Function (V_0 Pin)

Figure 13.13 shows a detailed block diagram of the LCD drive power supply unit.

The voltage output to the V_0 pin is V_{CC}. When either of these voltages is used directly as the LCD drive power supply, the V_0 and V_1 pins should be shorted. Also, connecting a variable resistance, R, between the V_0 and V_1 pins makes it possible to adjust the voltage applied to the V_1 pin, and so to provide luminance adjustment for the LCD panel.

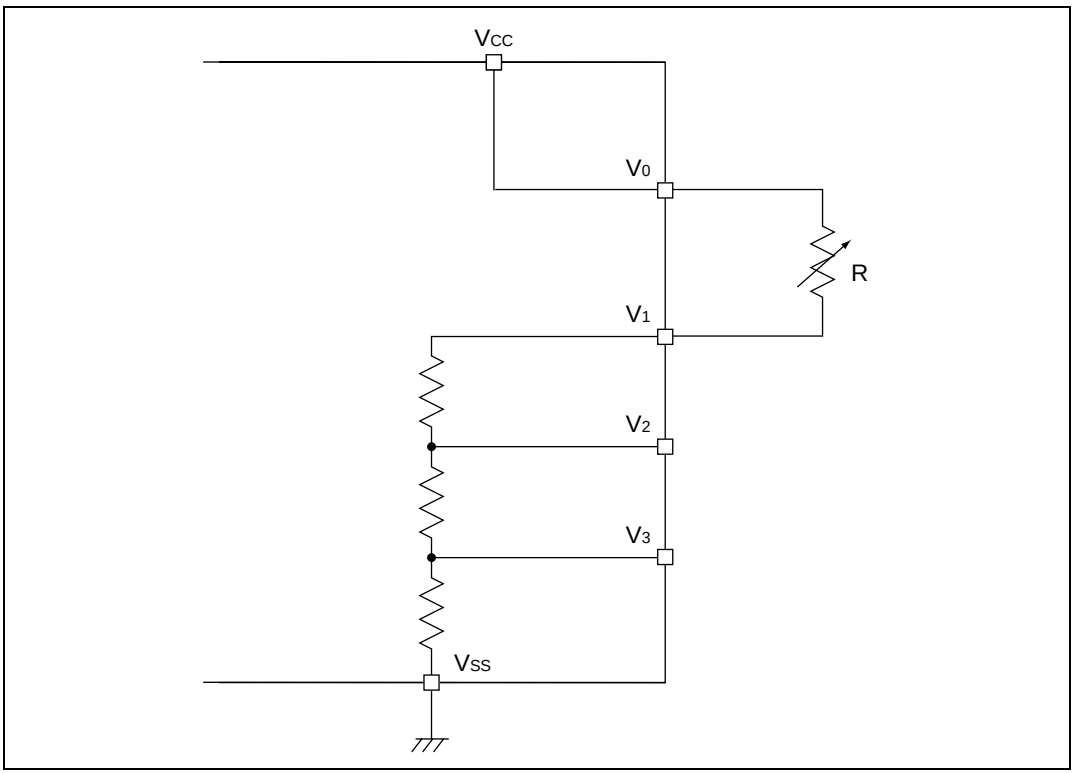


Figure 13.13 LCD Drive Power Supply Unit

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Output low voltage	V_{OL}	$P1_0$ to $P1_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	—	—	0.6	V	V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
		$P3_0$ to $P3_7$	—	—	1.0		V_{CC} = 4.0 V to 5.5 V I_{OL} = 10 mA	
			—	—	0.6		V_{CC} = 4.0 V to 5.5 V I_{OL} = 1.6 mA	
			—	—	0.5		I_{OL} = 0.4 mA	
Input/ output leakage current	$\lvert I_{IL} \rvert$	$\overline{RES}$, $P4_3$, $P1_0$ to $P1_7$, OSC_1, X_1, $P3_0$ to $P3_7$, $P4_0$ to $P4_2$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	—	—	1.0	µA	V_{IN} = 0.5 V to V_{CC} – 0.5 V	
		PB_0 to PB_7	—	—	1.0		V_{IN} = 0.5 V to AV_{CC} – 0.5 V	
Pull-up MOS current	$-I_p$	$P1_0$ to $P1_7$, $P3_0$ to $P3_7$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$	20	—	200	µA	V_{CC} = 5.0 V, V_{IN} = 0.0 V	
			—	40	—		V_{CC} = 2.7 V, V_{IN} = 0.0 V	Reference value
Input capacitance	C_{in}	All input pins except power supply pin	—	—	15.0	pF	f = 1 MHz, V_{IN} = 0.0 V, T_a = 25°C	

Mnemonic	Operand Size	Operation	Branching Condition	Addressing Mode/ Instruction Length (bytes) #xx: 8/16	Rn	@Rn	@(d:16, Rn)	@–Rn/@Rn+	@aa: 8/16	@(d:8, PC)	@@aa	Implied	Condition Code I	H	N	Z	V	C	No. of States
BIOR #xx:3, @aa:8	B	C∨(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
BXOR #xx:3, Rd	B	C⊕(#xx:3 of Rd8) → C			2								—	—	—	—	—	↕	2
BXOR #xx:3, @Rd	B	C⊕(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
BXOR #xx:3, @aa:8	B	C⊕(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
BIXOR #xx:3, Rd	B	C⊕(#xx:3 of Rd8) → C			2								—	—	—	—	—	↕	2
BIXOR #xx:3, @Rd	B	C⊕(#xx:3 of @Rd16) → C				4							—	—	—	—	—	↕	6
BIXOR #xx:3, @aa:8	B	C⊕(#xx:3 of @aa:8) → C							4				—	—	—	—	—	↕	6
BRA d:8 (BT d:8)	—	PC ← PC+d:8								2			—	—	—	—	—	—	4
BRN d:8 (BF d:8)	—	PC ← PC+2								2			—	—	—	—	—	—	4
BHI d:8	—	If condition is true then PC ← PC+d:8 else next;	C ∨ Z = 0							2			—	—	—	—	—	—	4
BLS d:8	—		C ∨ Z = 1							2			—	—	—	—	—	—	4
BCC d:8 (BHS d:8)	—		C = 0							2			—	—	—	—	—	—	4
BCS d:8 (BLO d:8)	—		C = 1							2			—	—	—	—	—	—	4
BNE d:8	—		Z = 0							2			—	—	—	—	—	—	4
BEQ d:8	—		Z = 1							2			—	—	—	—	—	—	4
BVC d:8	—		V = 0							2			—	—	—	—	—	—	4
BVS d:8	—		V = 1							2			—	—	—	—	—	—	4
BPL d:8	—		N = 0							2			—	—	—	—	—	—	4
BMI d:8	—		N = 1							2			—	—	—	—	—	—	4
BGE d:8	—		N⊕V = 0							2			—	—	—	—	—	—	4
BLT d:8	—		N⊕V = 1							2			—	—	—	—	—	—	4
BGT d:8	—		Z ∨ (N⊕V) = 0							2			—	—	—	—	—	—	4
BLE d:8	—		Z ∨ (N⊕V) = 1							2			—	—	—	—	—	—	4
JMP @Rn	—	PC ← Rn16				2							—	—	—	—	—	—	4
JMP @aa:16	—	PC ← aa:16							4				—	—	—	—	—	—	6
JMP @@aa:8	—	PC ← @aa:8									2		—	—	—	—	—	—	8
BSR d:8	—	SP–2 → SP PC → @SP PC ← PC+d:8								2			—	—	—	—	—	—	6

TCFH—8-Bit Timer Counter FH **H'B8** **Timer F**

Bit	7	6	5	4	3	2	1	0
	TCFH7	TCFH6	TCFH5	TCFH4	TCFH3	TCFH2	TCFH1	TCFH0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Count value

Note: TCFH and TCFL can also be used as the upper and lower halves, respectively, of a 16-bit event counter (TCF).

TCFL—8-Bit Timer Counter FL **H'B9** **Timer F**

Bit	7	6	5	4	3	2	1	0
	TCFL7	TCFL6	TCFL5	TCFL4	TCFL3	TCFL2	TCFL1	TCFL0
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Count value

Note: TCFH and TCFL can also be used as the upper and lower halves, respectively, of a 16-bit event counter (TCF).

Renesas 8-Bit Single-Chip Microcomputer
Hardware Manual
H8/3827R Group, H8/3827S Group, H8/38327 Group, H8/38427 Group

Publication Date: 1st Edition, September, 1999
Rev.6.00, August 04, 2006
Published by: Sales Strategic Planning Div.
Renesas Technology Corp.
Edited by: Customer Support Department
Global Strategic Communication Div.
Renesas Solutions Corp.