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Details	
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Core Processor	H8/300L
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LCD, PWM, WDT
Number of I/O	55
Program Memory Size	60KB (60K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
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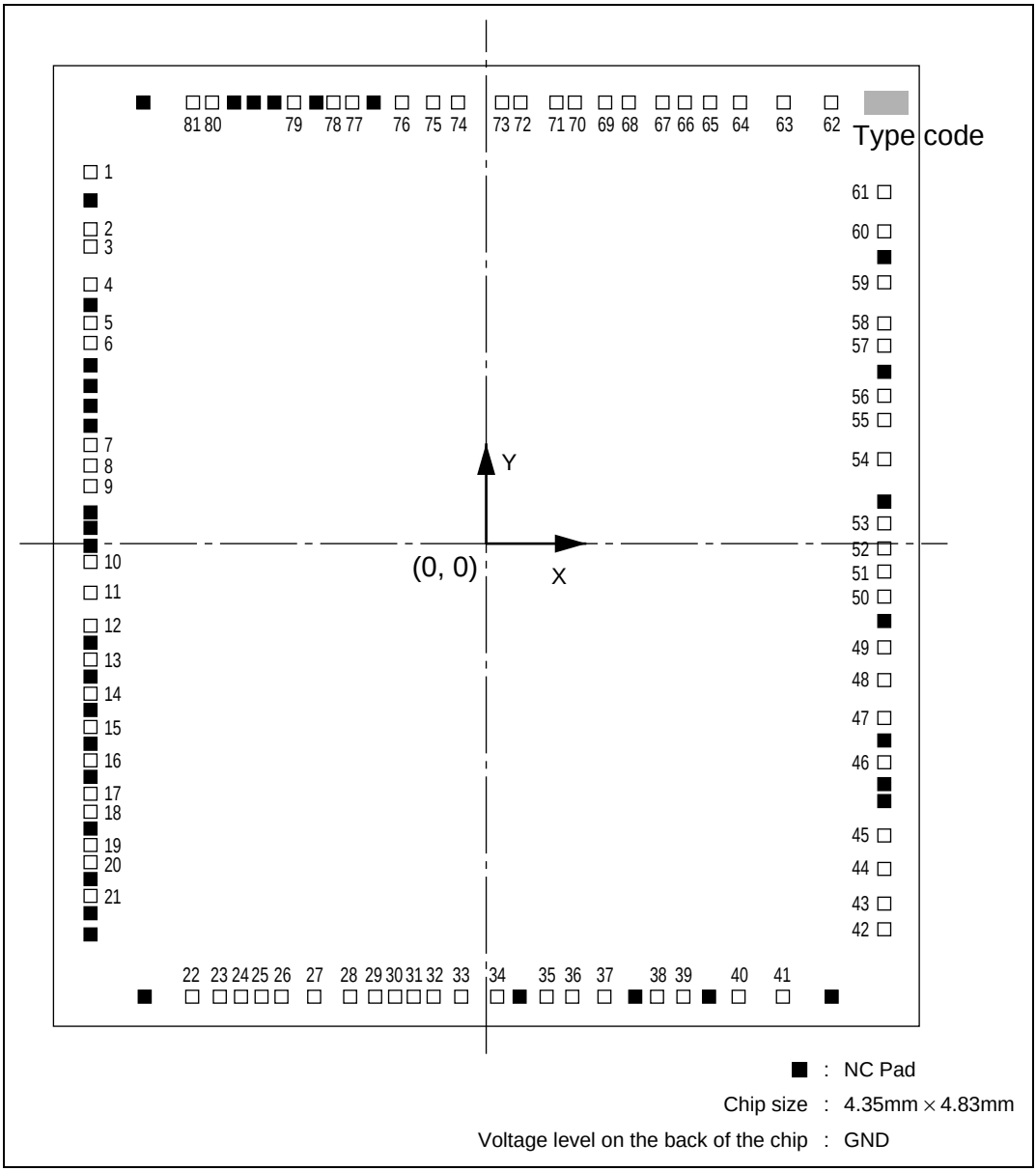


Figure 1.6 Bonding Pad Location Diagram of HCD64F38327 and HCD64F38427 (Top View)

		Coordinates*	
Pad No.	**Pad Name**	**X (µm)**	**Y (µm)**
31	V0	-67	-1577
32	Vcc	109	-1577
33	PA_3/COM4	237	-1577
34	PA_2/COM3	361	-1577
35	PA_1/COM2	486	-1577
36	PA_0/COM1	611	-1577
37	$P5_0/\overline{WKP}_0/SEG_1$	767	-1577
38	$P5_1/\overline{WKP}_1/SEG_2$	892	-1577
39	$P5_2/\overline{WKP}_2/SEG_3$	1017	-1577
40	$P5_3/\overline{WKP}_3/SEG_4$	1141	-1577
41	$P5_4/\overline{WKP}_4/SEG_5$	1605	-1224
42	$P5_5/\overline{WKP}_5/SEG_6$	1605	-1100
43	$P5_6/\overline{WKP}_6/SEG_7$	1605	-975
44	$P5_7/\overline{WKP}_7/SEG_8$	1605	-850
45	$P6_0/SEG_9$	1605	-723
46	$P6_1/SEG_{10}$	1605	-598
47	$P6_2/SEG_{11}$	1605	-473
48	$P6_3/SEG_{12}$	1605	-349
49	$P6_4/SEG_{13}$	1605	-195
50	$P6_5/SEG_{14}$	1605	-70
51	$P6_6/SEG_{15}$	1605	55
52	$P6_7/SEG_{16}$	1605	179
53	$P7_0/SEG_{17}$	1605	336
54	$P7_1/SEG_{18}$	1605	460
55	$P7_2/SEG_{19}$	1605	585
56	$P7_3/SEG_{20}$	1605	710
57	$P7_4/SEG_{21}$	1605	835
58	$P7_5/SEG_{22}$	1605	959
59	$P7_6/SEG_{23}$	1605	1084
60	$P7_7/SEG_{24}$	1605	1209
61	$P8_0/SEG_{25}$	1130	1577

1.3.2 Pin Functions

Table 1.6 outlines the pin functions of this LSI.

Table 1.6 Pin Functions

		Pin No.			
Type	**Symbol**	**FP-80A TFP-80C**	**FP-80B**	**I/O**	**Name and Functions**
Power source pins	V_{CC} CV_{CC}	32 26	34 28	Input	**Power supply:** All V_{CC} pins should be connected to the system power supply. See section 14, Power Supply Circuit, for a CV_{CC} pin (V_{CC} pin in the H8/3827S Group).
	V_{SS}	5 27	7 29	Input	**Ground:** All V_{SS} pins should be connected to the system power supply (0 V).
	AV_{CC}	73	75	Input	**Analog power supply:** This is the power supply pin for the A/D converter. When the A/D converter is not used, connect this pin to the system power supply.
	AV_{SS}	2	4	Input	**Analog ground:** This is the A/D converter ground pin. It should be connected to the system power supply (0V).
	V_0	31	33	Output	**LCD power supply:** These are the power supply pins for the LCD controller/driver. They incorporate a power supply split-resistance, and are normally used with V_0 and V_1 shorted.
	V_1 V_2 V_3	30 29 28	32 31 30	Input	

2.3.1 Data Formats in General Registers

Data of all the sizes above can be stored in general registers as shown in figure 2.3.

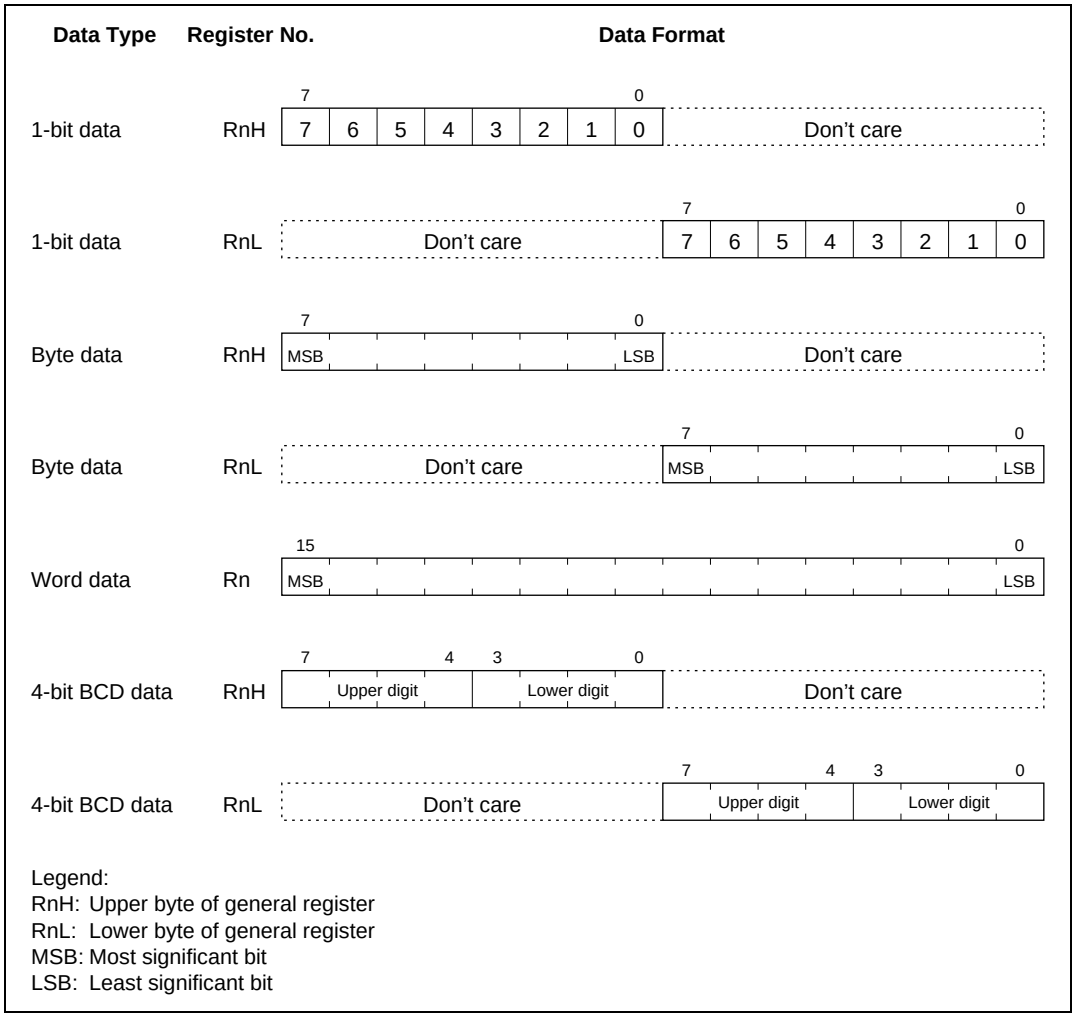


Figure 2.3 Register Data Formats

Section 3 Exception Handling

3.1 Overview

Exception handling is performed in this LSI when a reset or interrupt occurs. Table 3.1 shows the priorities of these two types of exception handling.

Table 3.1 Exception Handling Types and Priorities

Priority	Exception Source	Time of Start of Exception Handling
High	Reset	Exception handling starts as soon as the reset state is cleared
↑	Interrupt	When an interrupt is requested, exception handling starts after execution of the present instruction or the exception handling in progress is completed
Low		

3.2 Reset

3.2.1 Overview

A reset is the highest-priority exception. The internal state of the CPU and the registers of the on-chip peripheral modules are initialized.

3.2.2 Reset Sequence

As soon as the $\overline{\text{RES}}$ pin goes low, all processing is stopped and the chip enters the reset state.

To make sure the chip is reset properly, observe the following precautions.

- At power on: Hold the $\overline{\text{RES}}$ pin low until the clock pulse generator output stabilizes.
- Resetting during operation: Hold the $\overline{\text{RES}}$ pin low for at least 10 system clock cycles.

Reset exception handling takes place as follows.

- The CPU internal state and the registers of on-chip peripheral modules are initialized, with the I bit of the condition code register (CCR) set to 1.
- The PC is loaded from the reset exception handling vector address (H'0000 to H'0001), after which the program starts executing from the address indicated in PC.

3. Port Pull-Up Control Register 1 (PUCR1)

Bit	7	6	5	4	3	2	1	0
	$PUCR1_7$	$PUCR1_6$	$PUCR1_5$	$PUCR1_4$	$PUCR1_3$	$PUCR1_2$	$PUCR1_1$	$PUCR1_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PUCR1 controls whether the MOS pull-up of each of the port 1 pins $P1_7$ to $P1_0$ is on or off. When a PCR1 bit is cleared to 0, setting the corresponding PUCR1 bit to 1 turns on the MOS pull-up for the corresponding pin, while clearing the bit to 0 turns off the MOS pull-up.

Upon reset, PUCR1 is initialized to H'00.

4. Port Mode Register 1 (PMR1)

Bit	7	6	5	4	3	2	1	0
	IRQ3	IRQ2	IRQ1	IRQ4	TMIG	TMOFH	TMOFL	TMOW
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PMR1 is an 8-bit read/write register, controlling the selection of pin functions for port 1 pins.

Upon reset, PMR1 is initialized to H'00.

Bit 7: $P1_7/\overline{IRQ_3}$/TMIF pin function switch (IRQ3)

This bit selects whether pin $P1_7/\overline{IRQ_3}$/TMIF is used as $P1_7$ or as $\overline{IRQ_3}$/TMIF.

Bit 7 IRQ3	Description	
0	Functions as $P1_7$ I/O pin	(initial value)
1	Functions as $\overline{IRQ_3}$/TMIF input pin	

Note: Rising or falling edge sensing can be designated for IRQ_3, TMIF. For details on TMIF settings, see 3. Timer Control Register F (TCRF) in section 9.4.2.

8.5.2 Register Configuration and Description

Table 8.11 shows the port 5 register configuration.

Table 8.11 Port 5 Registers

Name	Abbr.	R/W	Initial Value	Address
Port data register 5	PDR5	R/W	H'00	H'FFD8
Port control register 5	PCR5	W	H'00	H'FFE8
Port pull-up control register 5	PUCR5	R/W	H'00	H'FFE2
Port mode register 5	PMR5	R/W	H'00	H'FFCC

1. Port Data Register 5 (PDR5)

Bit	7	6	5	4	3	2	1	0
	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDR5 is an 8-bit register that stores data for port 5 pins $P5_7$ to $P5_0$. If port 5 is read while PCR5 bits are set to 1, the values stored in PDR5 are read, regardless of the actual pin states. If port 5 is read while PCR5 bits are cleared to 0, the pin states are read.

Upon reset, PDR5 is initialized to H'00.

2. Port Control Register 5 (PCR5)

Bit	7	6	5	4	3	2	1	0
	$PCR5_7$	$PCR5_6$	$PCR5_5$	$PCR5_4$	$PCR5_3$	$PCR5_2$	$PCR5_1$	$PCR5_0$
Initial value	0	0	0	0	0	0	0	0
Read/Write	W	W	W	W	W	W	W	W

PCR5 is an 8-bit register for controlling whether each of the port 5 pins $P5_7$ to $P5_0$ functions as an input pin or output pin. Setting a PCR5 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. PCR5 and PDR5 settings are valid when the corresponding pins are designated for general-purpose input/output by PMR5 and bits SGS3 to SGS0 in LPCR.

Upon reset, PCR5 is initialized to H'00.

Bits 6 and 5: Counter up/down control (TMC6, TMC5)

Selects whether TCC up/down control is performed by hardware using UD pin input, or whether TCC functions as an up-counter or a down-counter.

Bit 6 TMC6	Bit 5 TMC5	Description	
0	0	TCC is an up-counter	(initial value)
0	1	TCC is a down-counter	
1	*	Hardware control by UD pin input UD pin input high: Down-counter UD pin input low: Up-counter	

*: Don't care

Bits 4 and 3: Reserved bits

Bits 4 and 3 are reserved; they are always read as 1 and cannot be modified.

Bits 2 to 0: Clock select (TMC2 to TMC0)

Bits 2 to 0 select the clock input to TCC. For external event counting, either the rising or falling edge can be selected.

Bit 2 TMC2	Bit 1 TMC1	Bit 0 TMC0	Description	
0	0	0	Internal clock: ϕ/8192	(initial value)
0	0	1	Internal clock: ϕ/2048	
0	1	0	Internal clock: ϕ/512	
0	1	1	Internal clock: ϕ/64	
1	0	0	Internal clock: ϕ/16	
1	0	1	Internal clock: ϕ/4	
1	1	0	Internal clock: ϕw/4	
1	1	1	External event (TMIC): rising or falling edge*	

Note: * The edge of the external event signal is selected by bit IEG1 in the IRQ edge select register (IEGR). See 1. IRQ edge select register (IEGR) in 3.3.2 for details. IRQ1 must be set to 1 in port mode register 1 (PMR1) before setting 111 in bits TMC2 to TMC0.

9.5.3 Noise Canceler

The noise canceler consists of a digital low-pass filter that eliminates high-frequency component noise from the pulses input from the input capture input pin. The noise canceler is set by NCS* in PMR3.

Figure 9.9 shows a block diagram of the noise canceler.

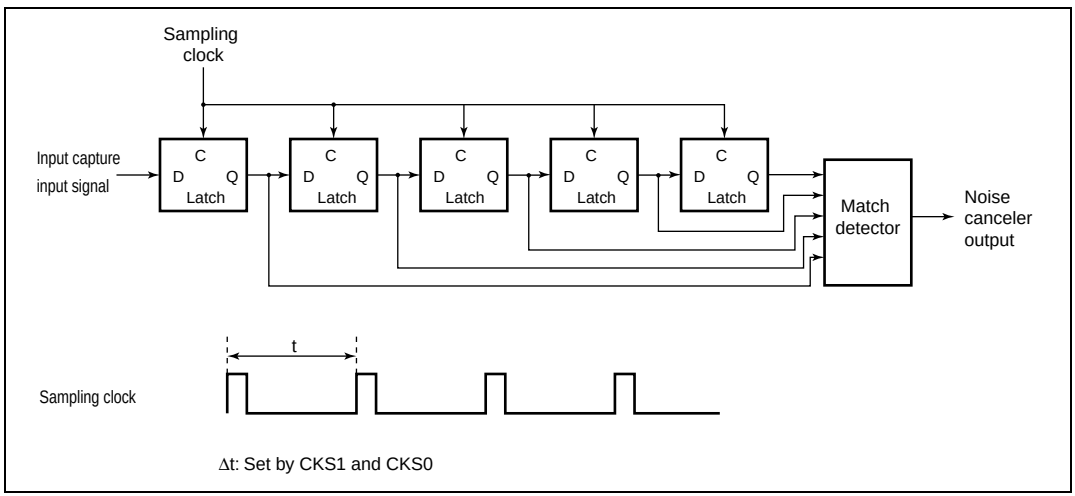


Figure 9.9 Noise Canceler Block Diagram

The noise canceler consists of five latch circuits connected in series and a match detector circuit. When the noise cancellation function is not used (NCS = 0), the system clock is selected as the sampling clock. When the noise cancellation function is used (NCS = 1), the sampling clock is the internal clock selected by CKS1 and CKS0 in TMG, the input capture input is sampled on the rising edge of this clock, and the data is judged to be correct when all the latch outputs match. If all the outputs do not match, the previous value is retained. After a reset, the noise canceler output is initialized when the falling edge of the input capture input signal has been sampled five times. Therefore, after making a setting for use of the noise cancellation function, a pulse with at least five times the width of the sampling clock is a dependable input capture signal. Even if noise cancellation is not used, an input capture input signal pulse width of at least 2ϕ or $2\phi_{SUB}$ is necessary to ensure that input capture operations are performed properly

Note: * An input capture signal may be generated when the NCS bit is modified.

Bit 7 TIE	Description	
0	Transmit data empty interrupt request (TXI) disabled	(initial value)
1	Transmit data empty interrupt request (TXI) enabled	

Bit 6: Receive interrupt enable (RIE)

Bit 6 selects enabling or disabling of the receive data full interrupt request (RXI) and the receive error interrupt request (ERI) when receive data is transferred from the receive shift register (RSR) to the receive data register (RDR), and bit RDRF in the serial status register (SSR) is set to 1. There are three kinds of receive error: overrun, framing, and parity.

RXI can be released by clearing bit RDRF or the FER, PER, or OER error flag to 0, or by clearing bit RIE to 0.

Bit 6 RIE	Description	
0	Receive data full interrupt request (RXI) and receive error interrupt request (ERI) disabled	(initial value)
1	Receive data full interrupt request (RXI) and receive error interrupt request (ERI) enabled	

Bit 5: Transmit enable (TE)

Bit 5 selects enabling or disabling of the start of transmit operation.

Bit 5 TE	Description	
0	Transmit operation disabled[*1] (TXD pin is I/O port)	(initial value)
1	Transmit operation enabled[*2] (TXD pin is transmit data pin)	

Notes: 1. Bit TDRE in SSR is fixed at 1.

2. When transmit data is written to TDR in this state, bit TDR in SSR is cleared to 0 and serial data transmission is started. Be sure to carry out serial mode register (SMR) settings, and setting of bit SPC31 or SPC32 in SPCR, to decide the transmission format before setting bit TE to 1.

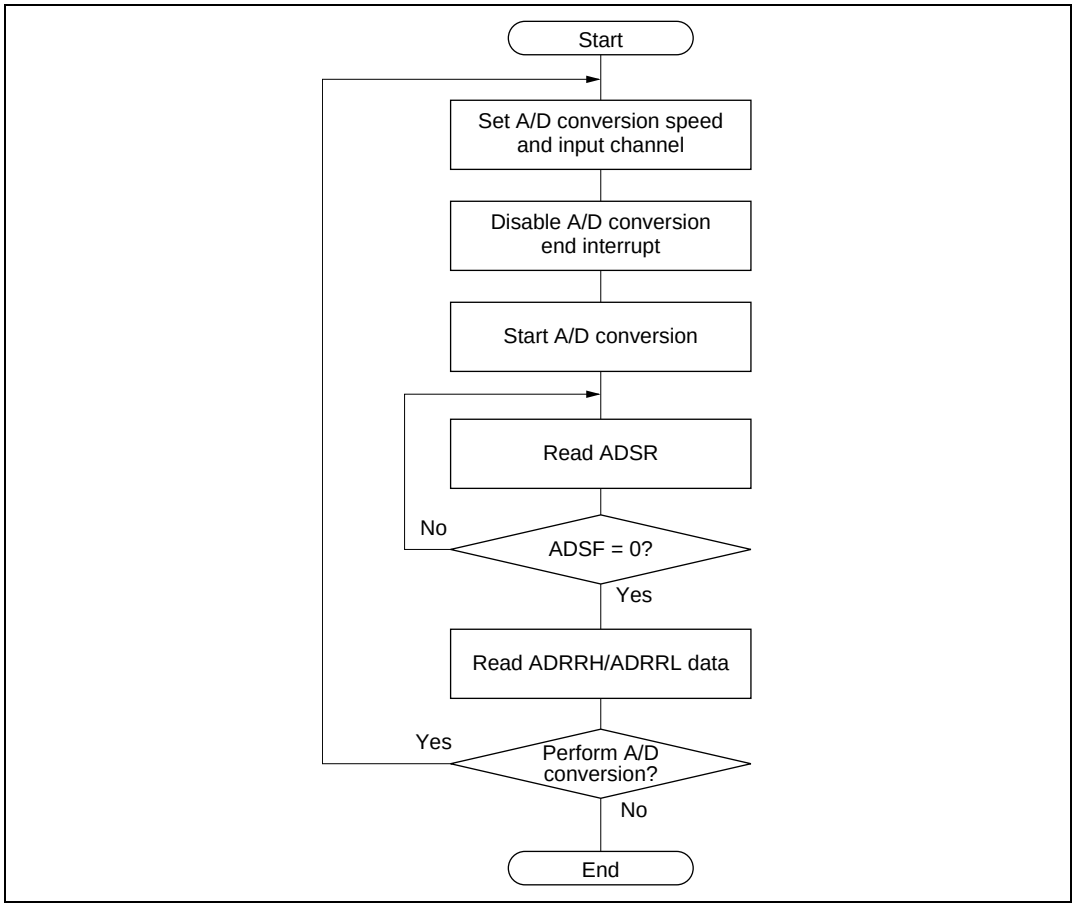


Figure 12.4 Flow Chart of Procedure for Using A/D Converter (Polling by Software)

12.6 Application Notes

12.6.1 Application Notes

- Data in ADRRH and ADRRL should be read only when the A/D start flag (ADSF) in the A/D start register (ADSR) is cleared to 0.
- Changing the digital input signal at an adjacent pin during A/D conversion may adversely affect conversion accuracy.
- When A/D conversion is started after clearing module standby mode, wait for 10 ϕ clock cycles before starting.
- In active mode or sleep mode, analog power supply current (AI_{STOP1}) flows into the ladder resistance even when the A/D converter is not operating. Therefore, if the A/D converter is not used, it is recommended that AV_{CC} be connected to the system power supply and the ADCKSTP(A/D converter module standby mode control) bit be cleared to 0 in clock stop register 1 (CKSTPR1).

12.6.2 Permissible Signal Source Impedance

This LSI's analog input is designed such that conversion precision is guaranteed for an input signal for which the signal source impedance is 10 kΩ or less. This specification is provided to enable the A/D converter's sample-and-hold circuit input capacitance to be charged within the sampling time; if the sensor output impedance exceeds 10 kΩ, charging may be insufficient and it may not be possible to guarantee A/D conversion precision. However, a large capacitance provided externally, the input load will essentially comprise only the internal input resistance of 10 kΩ, and the signal source impedance is ignored. However, as a low-pass filter effect is obtained in this case, it may not be possible to follow an analog signal with a large differential coefficient (e.g., 5 mV/μs or greater) (see figure 12.6). When converting a high-speed analog signal, a low-impedance buffer should be inserted.

Bit 4: Expansion signal select (SGX)

Bit 4 selects whether the SEG_{32}/CL_1, SEG_{31}/CL_2, SEG_{30}/DO, and SEG_{29}/M pins are used as segment pins (SEG_{32} to SEG_{29}) or as segment external expansion pins (CL_1, CL_2, DO, and M).

In the H8/38327 Group and H8/38427 Group this bit should be left at its initial value and not written to. Changing the value of this bit may prevent the SEG/COM signal from operating normally.

Bit 4 SGX	Description	
0	Pins SEG_{32} to SEG_{29}*	(initial value)
1	Pins CL_1, CL_2, DO, M	

Note: * These pins function as ports when the setting of SGS3 to SGS0 is 0000 or 0001.

Bits 3 to 0: Segment driver select 3 to 0 (SGS3 to SGS0)

Bits 3 to 0 select the segment drivers to be used. The SGX = 0 setting is selected on the H8/38327 and H8/38427.

					Function of Pins SEG_{32} to SEG_1				
Bit 4 SGX	Bit 3 SGS3	Bit 2 SGS2	Bit 1 SGS1	Bit 0 SGS0	SEG_{32} to SEG_{25}	SEG_{24} to SEG_{17}	SEG_{16} to SEG_9	SEG_8 to SEG_1	Notes
0	0	0	0	0	Port	Port	Port	Port	(initial value)
	0	0	0	1	Port	Port	Port	Port	
	0	0	1	*	SEG	Port	Port	Port	
	0	1	0	*	SEG	SEG	Port	Port	
	0	1	1	*	SEG	SEG	SEG	Port	
	1	*	*	*	SEG	SEG	SEG	SEG	
1	0	0	0	0	Port*1	Port	Port	Port	
	*	*	*	*	Setting prohibited				

*: Don't care

Note: 1. SEG_{32} to SEG_{29} are external expansion pins.

15.2.2 DC Characteristics

Table 15.2 lists the DC characteristics.

Table 15.2 DC Characteristics

V_{CC} = 1.8 V to 5.5 V, AV_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –20°C to +75°C[*4] (including subactive mode) unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$\overline{RES}$, $\overline{WKP}_0$ to $\overline{WKP}_7$, $\overline{IRQ}_0$ to $\overline{IRQ}_4$, AEVL, AEVH, TMIC, TMIF, TMIG SCK_{31}, SCK_{32}, $\overline{ADTRG}$	0.8 V_{CC}	—	Vcc + 0.3	V	V_{CC} = 4.0 V to 5.5 V	
			0.9 V_{CC}	—	V_{CC} + 0.3		Except the above	
		RXD_{31}, RXD_{32}, UD	0.7 V_{CC}	—	V_{CC} + 0.3	V	V_{CC} = 4.0 V to 5.5 V	
			0.8 V_{CC}	—	V_{CC} + 0.3		Except the above	
		OSC_1	0.8 V_{CC}	—	V_{CC} + 0.3	V	V_{CC} = 4.0 V to 5.5 V	
			0.9 V_{CC}	—	V_{CC} + 0.3		Except the above	
		X_1	0.9 V_{CC}	—	V_{CC} + 0.3	V	V_{CC} = 1.8 V to 5.5 V	
		$P1_0$ to $P1_7$, $P3_0$ to $P3_7$, $P4_0$ to $P4_3$, $P5_0$ to $P5_7$, $P6_0$ to $P6_7$, $P7_0$ to $P7_7$, $P8_0$ to $P8_7$, PA_0 to PA_3	0.7 V_{CC}	—	V_{CC} + 0.3	V	V_{CC} = 4.0 V to 5.5 V	
			0.8 V_{CC}	—	V_{CC} + 0.3		Except the above	
		PB_0 to PB_7	0.7 V_{CC}	—	AV_{CC} + 0.3		V_{CC} = 4.0 V to 5.5 V	
			0.8 V_{CC}	—	AV_{CC} + 0.3		Except the above	

Note: Connect the TEST pin to V_{SS}.

15.4.4 A/D Converter Characteristics

Table 15.12 shows the A/D converter characteristics of the H8/3827R.

Table 15.12 A/D Converter Characteristics

V_{CC} = 1.8 V to 5.5 V, V_{SS} = AV_{SS} = 0.0 V, T_a = –40°C to +85°C unless otherwise indicated.

Item	Symbol	Applicable Pins	Values Min	Typ	Max	Unit	Test Condition	Notes
Analog power supply voltage	AV_{CC}	AV_{CC}	1.8	—	5.5	V		*1
Analog input voltage	AV_{IN}	AN_0 to AN_7	– 0.3	—	AV_{CC} + 0.3	V		
Analog power supply current	AI_{OPE}	AV_{CC}	—	—	1.5	mA	AV_{CC} = 5 V	
	AI_{STOP1}	AV_{CC}	—	600	—	µA		*2 Reference value
	AI_{STOP2}	AV_{CC}	—	—	5	µA		*3
Analog input capacitance	C_{AIN}	AN_0 to AN_7	—	—	15.0	pF		
Allowable signal source impedance	R_{AIN}		—	—	10.0	kΩ		
Resolution (data length)			—	—	10	bit		
Nonlinearity error			—	—	±2.5	LSB	AV_{CC} = 2.7 V to 5.5 V V_{CC} = 2.7 V to 5.5 V	*4
			—	—	±5.5		AV_{CC} = 2.0 V to 5.5 V V_{CC} = 2.0 V to 5.5 V	
			—	—	±7.5		Except the above	*5
Quantization error			—	—	±0.5	LSB		

Table 15.14 AC Characteristics for External Segment Expansion

V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_a = –40°C to +85°C (including subactive mode) unless otherwise specified.

Item	Symbol	Applicable Pins	Test Conditions	Values			Unit	Reference Figure
				Min	Typ	Max		
Clock high width	t_{CWH}	CL_1, CL_2	*	800	—	—	ns	Figure 15.7
Clock low width	t_{CWL}	CL_2	*	800	—	—	ns	Figure 15.7
Clock setup time	t_{CSU}	CL_1, CL_2	*	500	—	—	ns	Figure 15.7
Data setup time	t_{SU}	DO	*	300	—	—	ns	Figure 15.7
Data hold time	t_{DH}	DO	*	300	—	—	ns	Figure 15.7
M delay time	t_{DM}	M	*	–1000	—	1000	ns	Figure 15.7
Clock rise and fall times	t_{CT}	CL_1, CL_2		—	—	170	ns	Figure 15.7

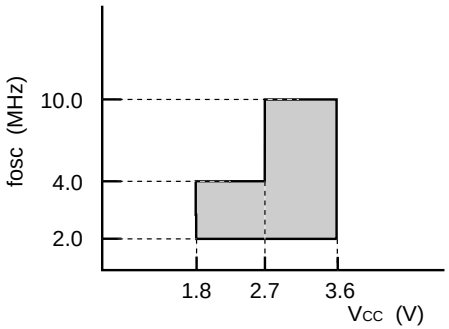
Note: * Value when the frame frequency is set to between 30.5 Hz and 488 Hz.

15.6 H8/3827S Group Electrical Characteristics

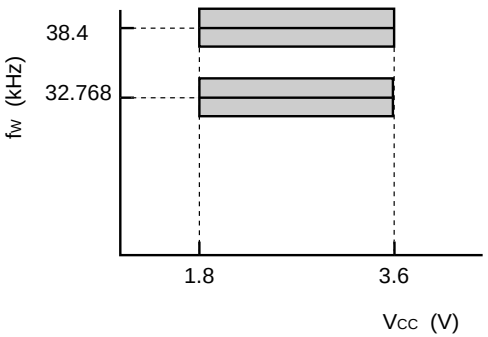
15.6.1 Power Supply Voltage and Operating Range

The power supply voltage and operating range are indicated by the shaded region in the figures.

1. Power Supply Voltage and Oscillator Frequency Range



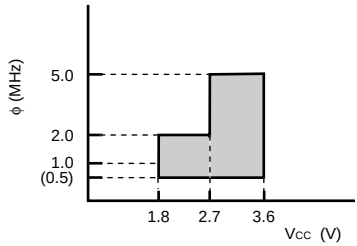
• Active (high-speed) mode
• Sleep (high-speed) mode



• All operating modes

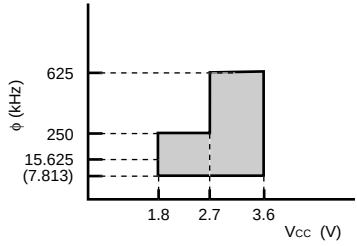
Note: fosc is the oscillator frequency. When external clocks are used, fosc=1MHz is the minimum.

2. Power Supply Voltage and Operating Frequency Range



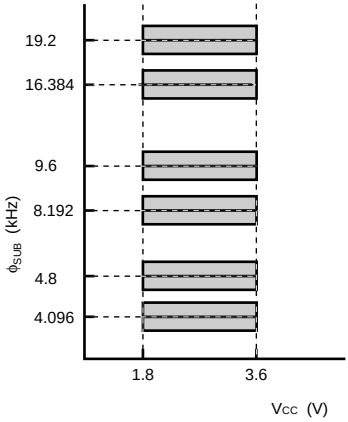
• Active (high-speed) mode
• Sleep (high-speed) mode (except CPU)

Note: Figures in parentheses are the minimum operating frequency of a case external clocks are used. When using an oscillator, the minimum operating frequency is ϕ=1MHz.



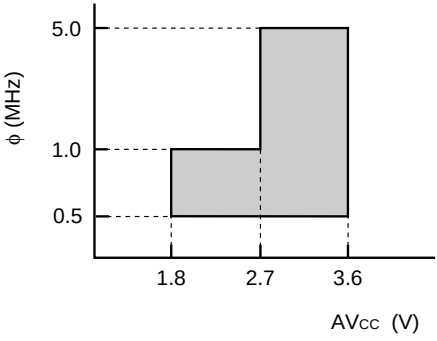
• Active (medium-speed) mode (except A/D converter)
• Sleep (medium-speed) mode (except A/D converter)

Note: Figures in parentheses are the minimum operating frequency of a case external clocks are used. When using an oscillator, the minimum operating frequency is ϕ=15.625kHz.

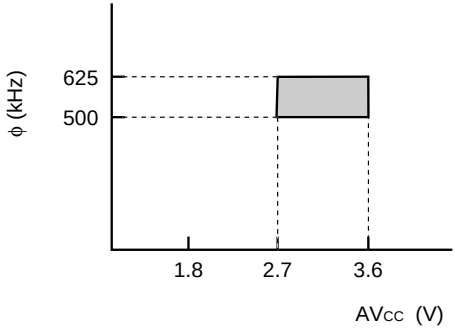


• Subactive mode
• Subsleep mode (except CPU)
• Watch mode (except CPU)

3. Analog Power Supply Voltage and A/D Converter Operating Range



• Active (high-speed) mode
• Sleep (high-speed) mode



• Active (medium-speed) mode
• Sleep (medium-speed) mode

PMR2—Port Mode Register 2 **H'C9** **I/O port**

Bit	7	6	5	4	3	2	1	0
	EXCL	—	—	—	—	—	—	—
Initial value	0	1	0	1	1	0	0	0
Read/Write	R/W	R	R/W	R	R	R/W	R/W	R/W

$P3_1$/UD/EXCL pin function switch

0	Functions as $P3_1$/UD I/O pin
1	Functions as EXCL input pin

Note: The information on this register applies to the H8/38327 Group and H8/38427 Group.