Welcome to E-XFL.COM

Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Not For New Designs
Module/Board Type	FPGA, USB Core
Core Processor	Spartan-3A DSP
Co-Processor	Cypress EZ-USB FX2LP
Speed	100MHz
Flash Size	4MB
RAM Size	128MB
Connector Type	B2B
Size / Dimension	2.7" x 1.9" (68mm x 48mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0320-00-ev02

Key Features

- Industrial-grade **Xilinx Spartan-3A DSP** FPGA module (1800 k gates or 3400 k gates)
- USB 2.0 (**Hi-Speed USB**) interface with a signalling bit rate of up to 480 Mbit/s
- 32-bit wide 1 Gbit **DDR SDRAM**
- FPGA configuration through:
  - B2B connector
  - JTAG port
  - SPI Flash memory
- Large **SPI Flash** memory (for configuration and operation) accessible through:
  - B2B connector (SPI direct)
  - FPGA
  - JTAG port (SPI indirect)
  - USB bus (Firmware Upgrade Tool)
- On-board 100 MHz oscillator for high performance
- On-board 24 MHz oscillator available to user
- 3 on-board high-power, high-efficiency, switch-mode DC-DC converters capable of 3 A each
- Power supply range: 4.0 - 7.0 V
- Power supply via USB or B2B (carrier board)
- 4 LEDs, 2 push buttons, 8 DIP switches.
- Plug-on module with 2 female 1.27 mm pitch header connectors
- 109 FPGA I/O pins (+ 10 dual-purpose pins) available on B2B connectors
- Evenly spread supply pins for good signal integrity
- Assembly options for cost or performance optimization available on request

Table of Contents

5 Power Supply

5.1 Power Supply Range

The power supply range of TE0320 is 4.0 V to 7.0 V.

5.2 Power Supply Sources

TE0320 can be power supplied in two ways:

- through USB connector J1,
- through B2B connector JM5 (pins 1 to 4).

The power supply source is determined by assembly option. See Figure 5.

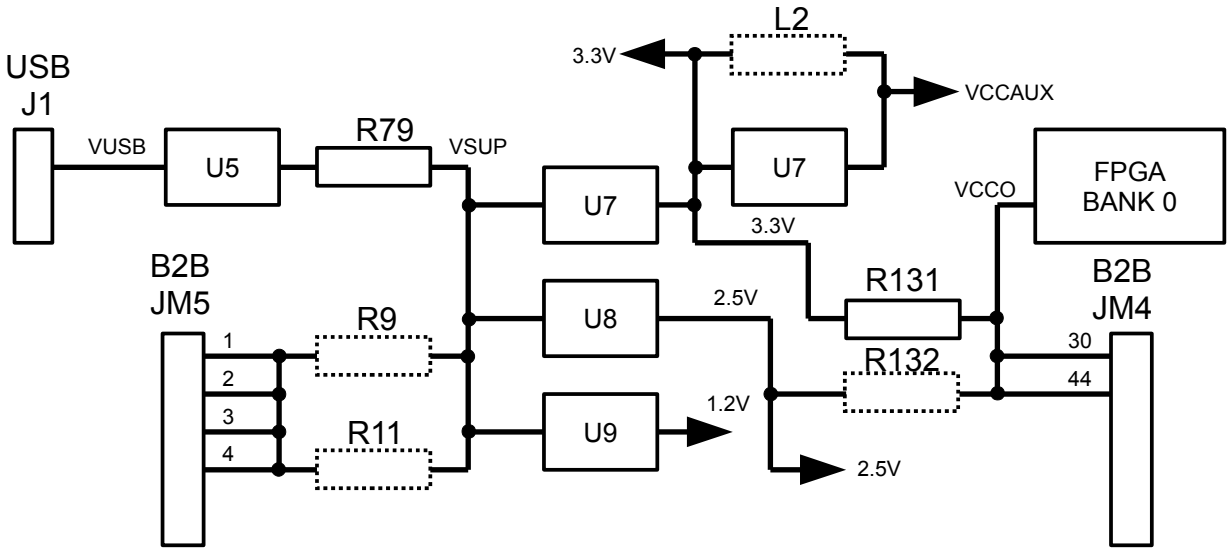


Figure 5: Power supply options diagram

If resistors R9 and R11 are populated and R12 is not populated, then TE0320 is power supplied through JM5 (B2B connector).

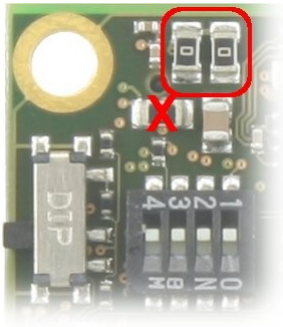


Figure 6: assembly combination for power supply through JM5.

If resistors R9 and R11 are not populated and R12 is populated, then TE0320 is power supplied through J1 (USB bus).

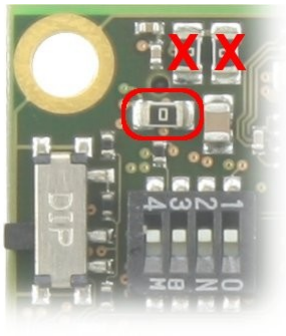


Figure 7: assembly combination for power supply through J1.

Any other assembly combination of R9, R11 and R12 is not allowed.

5.3 On-Board Power Rails

According to the Xilinx Spartan-3A DSP literature, there are the following power supply pin types:

- V_{CCAUX}: dedicated auxiliary power supply pins
- V_{CCINT}: dedicated internal core logic power supply pins
- V_{CCO}: supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards.

TE0320 has the following power rails on-board:

- Vsup

  It is the main internal power rail irrespective of the external power supply. It is supplied by either Vb2b or Vusb. It manages power distribution, conversion and supervision. It is routed also to connector JM5 as a user power supply output.
- Vb2b

  It is the main power rail when the module is supplied from B2B connector JM5.
- Vusb

  It is the main power rail when the module is supplied from USB mini-B connector J1. The maximum current than can be provided to J1 is determined by the USB power source.
- 3.3V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the module and connectors JM4 and JM5.
- 2.5V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the DDR SDRAM and connectors JM5.
- 1.2V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the V_{CCINT} power supply pins and connectors JM5.
- VCCAUX

Figure 10: assembly option for VCCAUX = off (bottom view).

Pins 30 and 44 of JM4 are power supply **inputs** in this case.

(b) if resistor R131 is not populated and R132 is populated, VCCCIO0 power rail is set to power rail 2.5V (nominal voltage = 2.5 V).

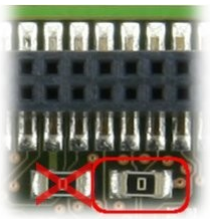


Figure 11: assembly option for VCCAUX = 2.5 V (bottom view).

Pins 30 and 44 of JM4 are power supply **outputs** in this case.

(c) if resistor R131 is populated and R132 is not populated, VCCCIO0 power rail is set to power rail 3.3V (nominal voltage = 3.3 V). This is the default.

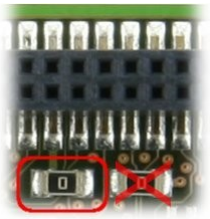


Figure 12: assembly option for VCCCIO0 = 3.3 V (bottom view).

Pins 30 and 44 of JM4 are power supply **outputs** in this case.

Assembly option where both R131 and R132 are populated is not allowed.

1.2 V, 2.5 V and 3.3 V voltage rails are provided by corresponding step-down regulator DC/DC converters, each one capable of providing up to 3 A of output current. These three regulators are synchronized to switch with 120° phase lag, to improve EMC, and to reduce input ripple. The synchronization circuit can be omitted in cost sensitive applications (please contact Trenz Electronic).

M0 value	M0 @ JM5
0	0
1	floating
1	1

Table 23: mode pin M0 settings.

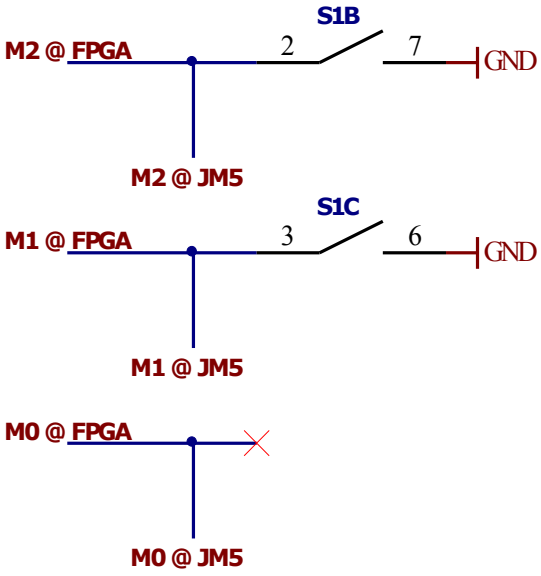


Figure 44: configuration modes schematic

10.2 Configuration via USB bus

To configure a TE0320 module via USB bus, there are different procedures to follow according to module status and purpose of use. For instance, a full quality control test already performed at Trenz Electronic laboratory premises requires all the following steps to be performed:

(a) generic USB device driver installation

(b) USB microcontroller large EEPROM programming

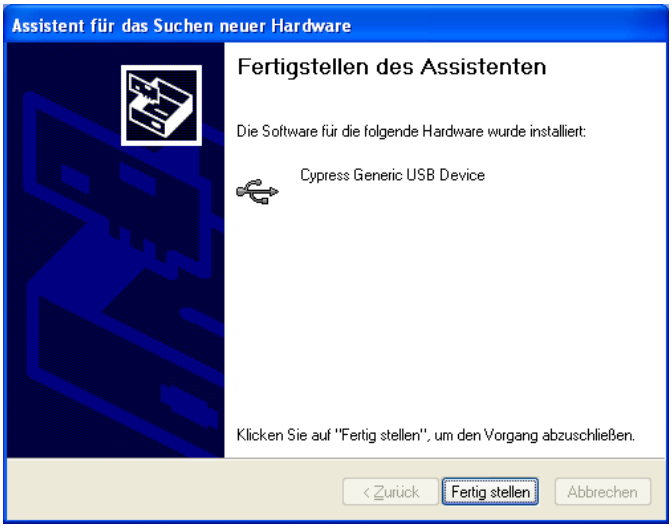
(c) specific USB device driver installation

(d) FWU file generation

(e) Firmware Upgrade Tool utilization.

step	first development cycle	following development cycles	EEPROM recovery	quality control (lab test)
(a)			•	•
(b)			•	•
(c)	•			•
(d)	•	•		•
(e)	•	•		•

Table 24: configuration steps via USB bus according to module status and purpose of use.



After successful installation of the generic device driver, TE0320 should be identified as “Cypress Generic USB Device” and the Device Manager panel should look like Figure 46.

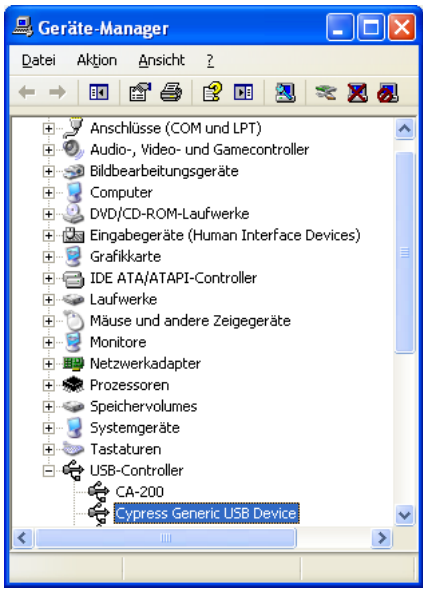


Figure 46: Device manager after successful installation of the generic device driver.

Now the EZ-USB microcontroller can be controlled from a computer by the Cypress USB Console.

10.2.2 USB microcontroller large EEPROM programming

TE0320 users are not normally required to perform this step.

Disconnect the TE0320 from the USB bus or leave it unconnected if it already is.

Ensure that DIP switch S1 is set as follows:

- S1A = OFF

  this disconnect the serial data line between the USB microcontroller and the large EEPROM; in so doing, the USB microcontroller enumerates as a

Cypress generic USB device

- S1B and S1C = do not care

  configuration mode is irrelevant for this step
- S1D = OFF

  master reset disabled

switch	S1 label	signal name	status
S1A	1	EEPROM serial data	OFF
S1B	2	M2	X
S1C	3	M1	X
S1D	4	/MR (master reset)	OFF

Table 26: S1 settings for forcing the EZ-USB FX2LP USB microcontroller to enumerate as a generic USB device driver.

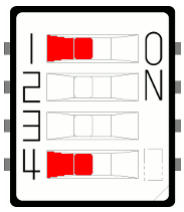


Figure 47: S1 settings for forcing the EZ-USB FX2LP USB microcontroller to enumerate as a generic USB device driver.

Connect the TE0320 to a USB port on your computer using a USB cable.

The USB microcontroller should now enumerate as a Cypress generic USB device.

Toggle S1A to ON; this will

- Connect the serial data line between the USB microcontroller and the large EEPROM;
- Allow the EZ-USB FX2LP USB microcontroller to program the large EEPROM;
- Prevent the EZ-USB FX2LP USB microcontroller to enumerate again for any content of the large EEPROM.

switch	S1 label	signal name	status
S1A	1	EEPROM serial data	ON
S1B	2	M2	X
S1C	3	M1	X
S1D	4	/MR (master reset)	OFF

Table 27: S1 settings for programming EZ-USB FX2LP USB microcontroller large EEPROM.

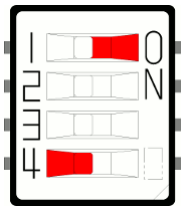
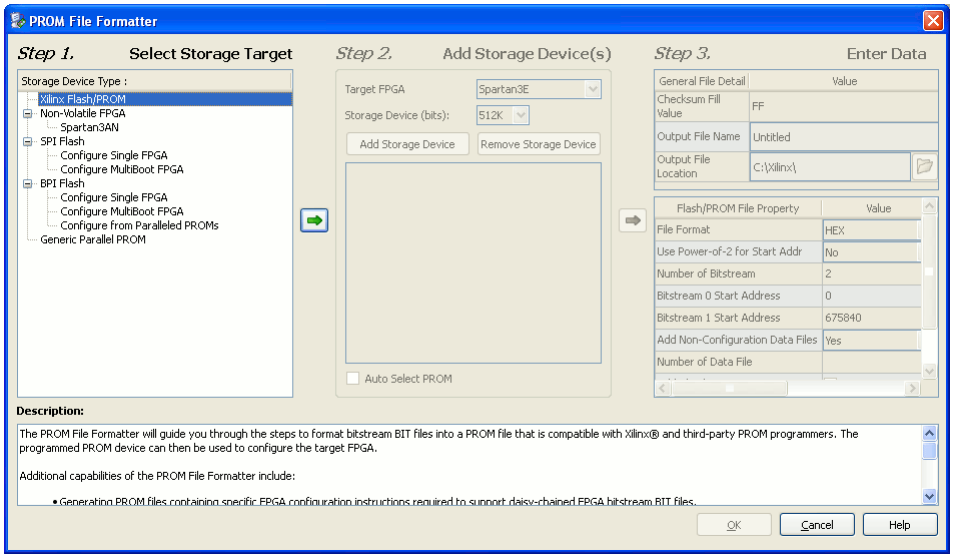
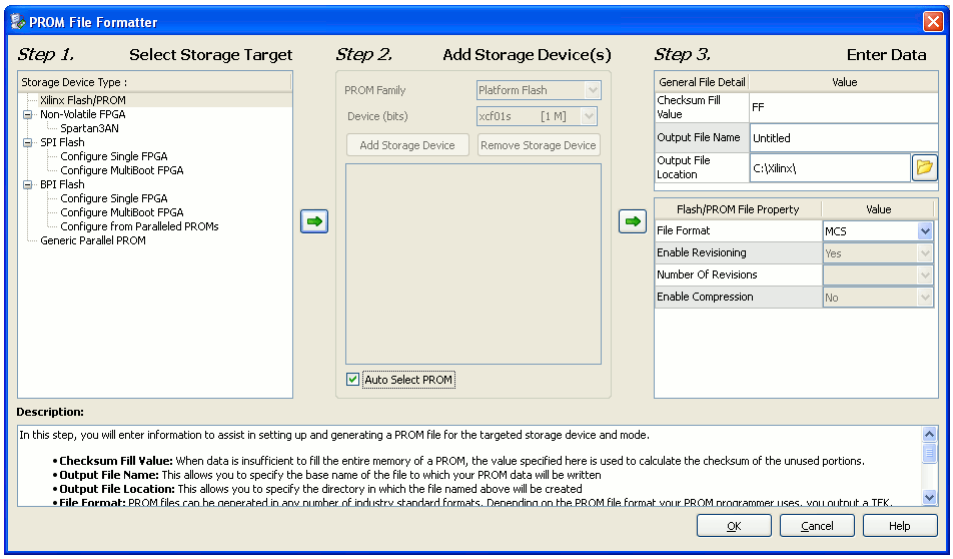


Figure 48: S1 settings for programming EZ-USB FX2LP USB microcontroller large EEPROM.

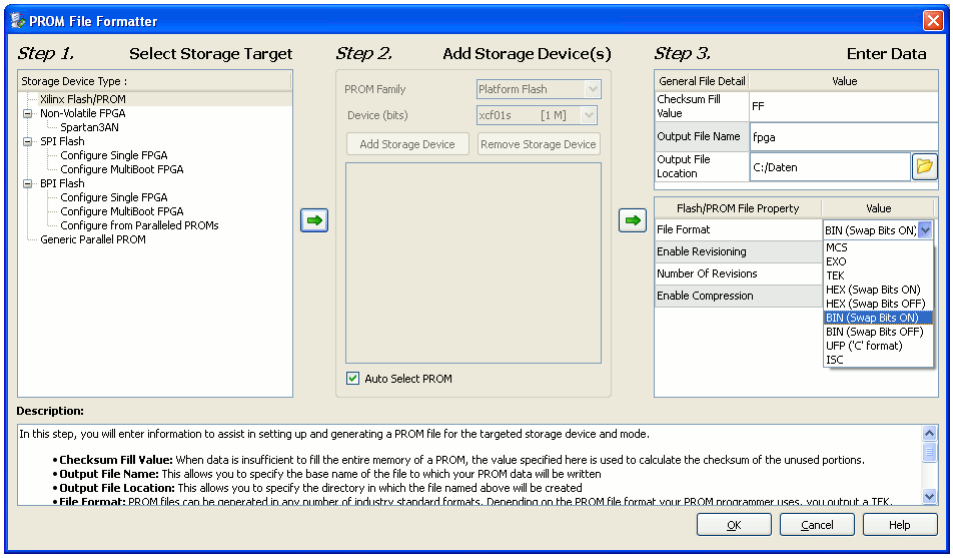


Select ***step 2. add storage device(s) / auto select PROM*** of the middle panel and press the right green arrow.



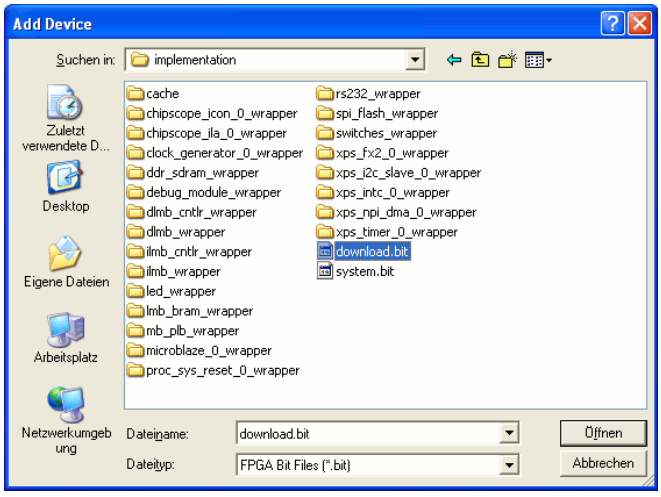
In ***step 3. enter data*** of the right panel

- type ***fpga*** in the `output file name` input field;
- choose a suitable path for the `output file location` input field;
- select ***BIN (swap bits ON)*** from the drop-down menu `file format` in the `flash/PROM file property` sub-panel;
- press the ***OK*** button in the bottom left corner of the current window.

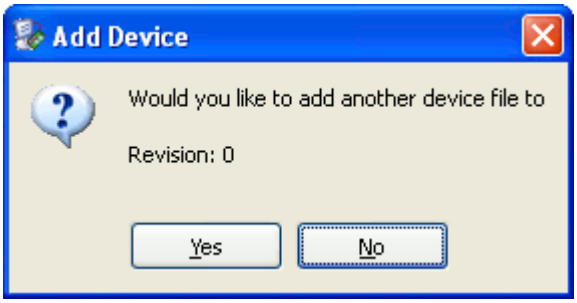


Any other name than ***fpga*** for the `output file name` input field is not allowed.

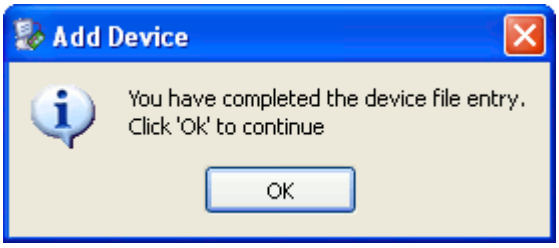
Just acknowledge the pup-up message.



Browse to the `./implementation/` folder of your "`.`" project folder and select the bit-stream file `download.bit`.
Press the ***open*** button in the bottom left corner of the current window.

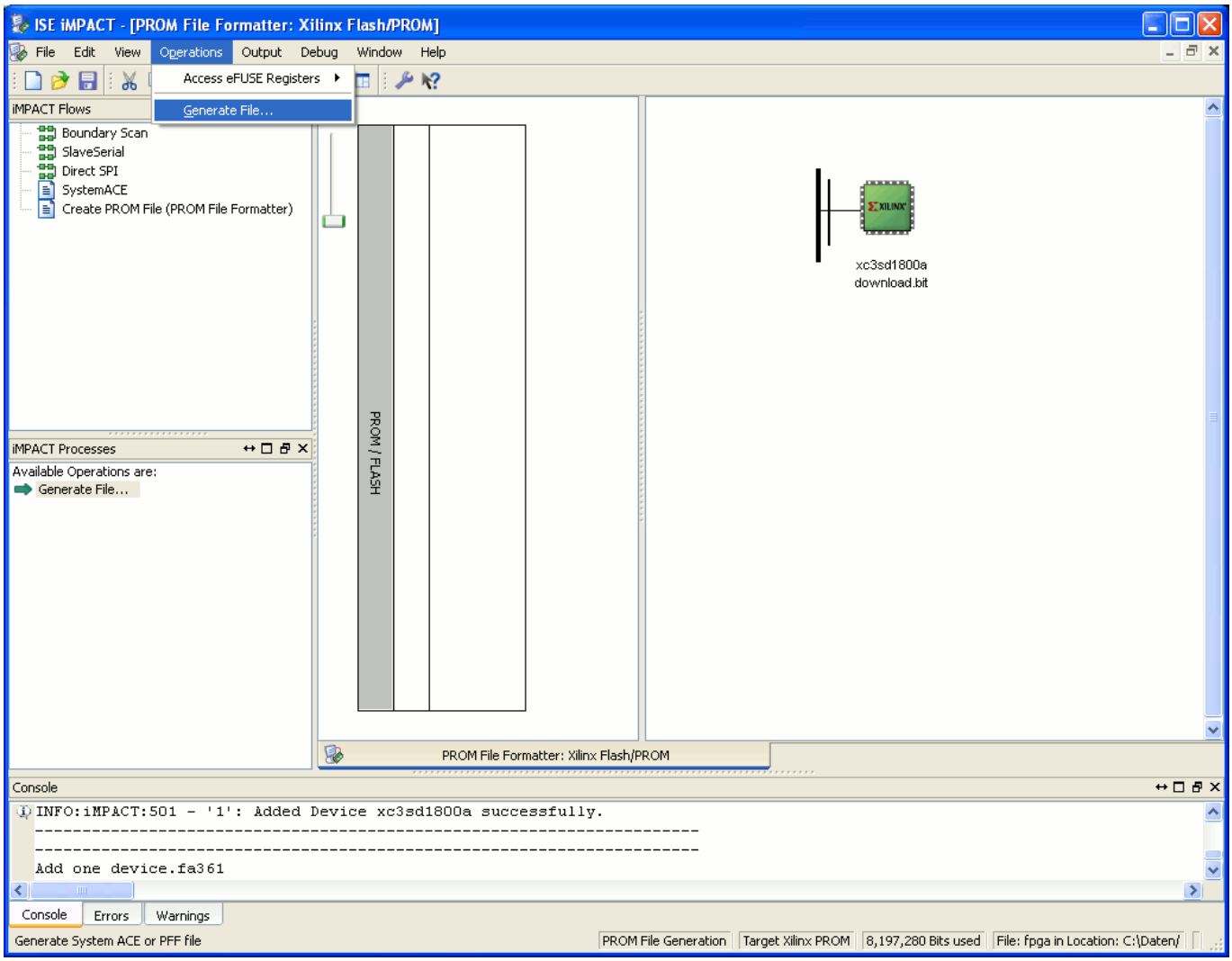


Your design likely consist of just one device file. So deny the request by pressing the ***NO*** button.

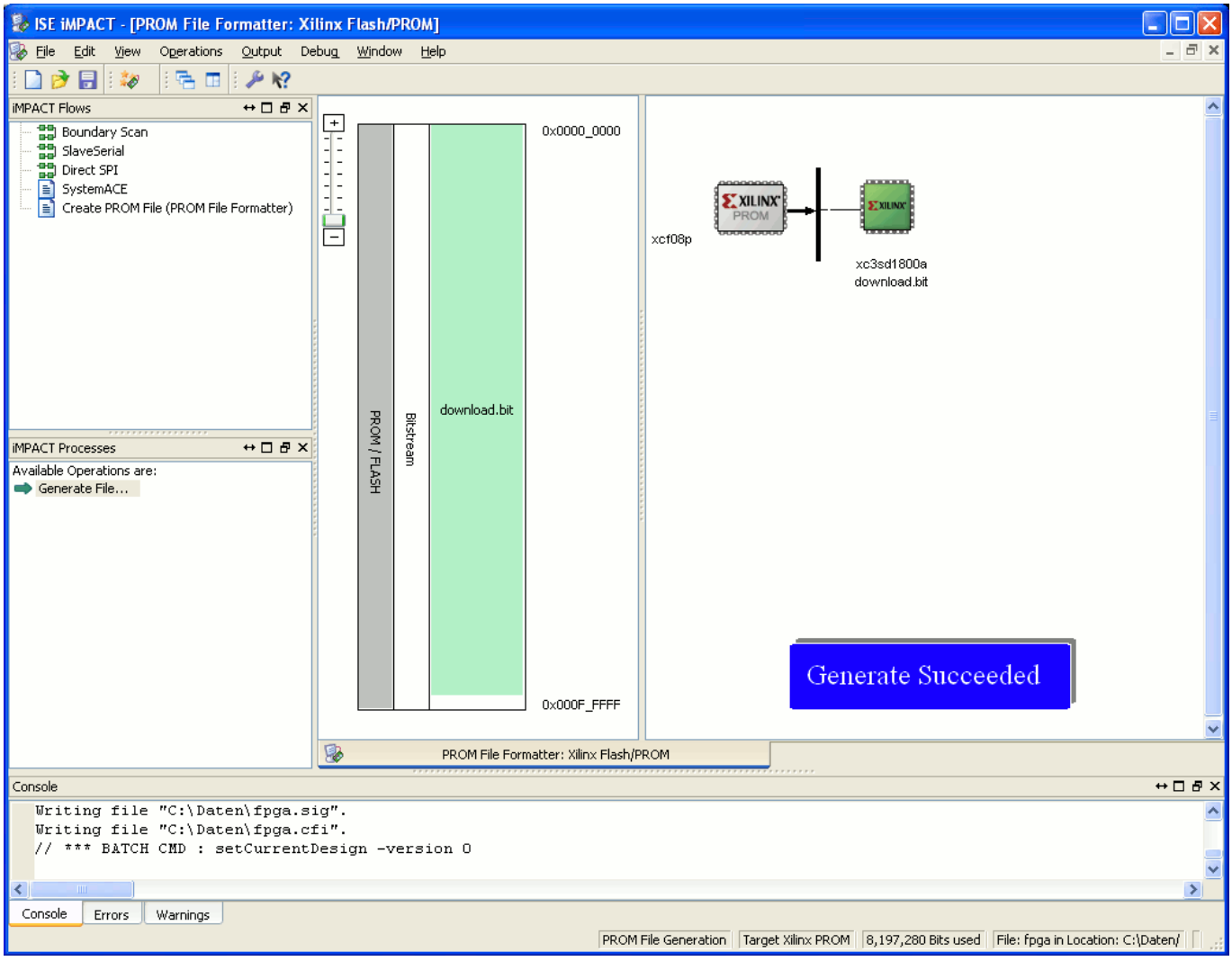


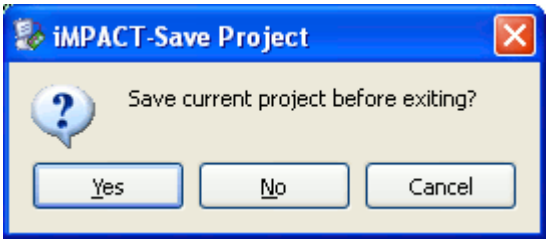
Just acknowledge the pup-up message.

Select ***operations / generate file...*** or double click ***generate file...*** from the `iMPACT processes` panel.



You should see the following message in the main panel: `generate succeeded.`





You might now want to save your Xilinx iMPACT project settings for future use.

In the folder corresponding to the path you chose as the `output file location`, you should find the `fpga.bin` PROM file.

10.2.4.3 FWU file from the PROM file

Once you have got your `fpga.bin` PROM file, you can proceed and generate your FWU (= FirmWare Upgrade) file. The FWU file is a ZIP archive containing 3 files:

- `Bootload.ini` – TE0320 booting settings (see paragraph 10.2.4.3.1 Bootload.ini file)
- `fpga.bin` – FPGA configuration PROM file

- master reset disabled (S1D set to OFF)

S1	S1 label	signal	status
S1A	1	EEPROM serial data	ON
S1B	2	M2	ON
S1C	3	M1	ON
S1D	4	/MR (master reset)	OFF

Table 29: S1 settings for configuration via USB bus.

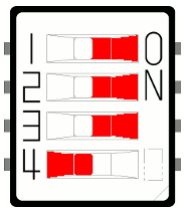


Figure 51: S1 settings for configuration via USB bus.

10.2.5.3 Slide Switch S2

Ensure that slide switch S2 is set to FX2 PON.

switch	signal	status
S2	PON / FX2 PON	FX2PON

Table 30: S2 settings for SPI Flash programming via USB bus.

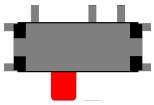


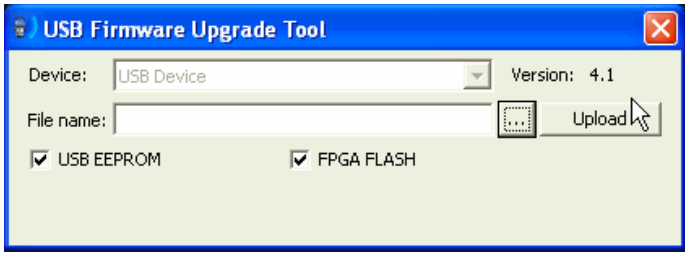
Figure 22: S2 settings for SPI Flash programming via USB bus (FX2 PON).

This will

- allow the EZ-USB FX2LP USB microcontroller to power off the FPGA,
- release the SPI lines driven by the FPGA and made them available to the EZ-USB FX2LP USB microcontroller
- allow the EZ-USB FX2LP USB microcontroller to program the SPI Flash memory.

10.2.5.4 FUT upgrade procedure

Open `USB Firmware Upgrade Tool` (double click `step5_user\USBFirmwareUpgradeTool.exe`).



Press the "`...`" button corresponding to the `File name`:

11.2 Unused IOB Pins

All signals entering and exiting a Xilinx Spartan-3 generation FPGA must pass through the I/O resources, known as I/O blocks or IOBs. Users can specify the configuration for any unused IOB pins. This is the serial data outputs for all JTAG instruction and data registers.

This options are set graphically in Xilinx ISE Software Project Navigator by selecting the following:

- Generate Programming File > Process Properties > Configuration Options > Unused IOB Pins

Select an option from the drop-down list.

(a) Pull Down
Default. All unused I/O pins and input-only pins have a pull-down resistor to GND.

(b) Pull Up
All unused I/O pins and input-only pins have a pull-up resistor to the VCCO_# supply for its associated I/O bank.

(c) Float (also: Pullnone)
All unused I/O pins and input-only pins are left floating (Hi-Z, high-impedance, three-state). Use external pull-up or pulldown resistors or logic to apply a valid signal level.

11.3 CCLK Frequency

In SPI Flash mode, the FPGA's internal oscillator generates the configuration clock frequency. The FPGA provides this clock on its CCLK output pin, driving the PROM's Slave Clock input pin. The FPGA begins configuring using its lowest frequency setting. If so specified in the configuration bitstream, the FPGA increases the CCLK frequency to the specified setting for the remainder of the configuration process. The maximum frequency is specified using the ConfigRate bitstream generator option. The maximum frequency supported by the FPGA configuration logic depends on the timing for the SPI Flash device. For TE0320 SPI Flash PROM, use ConfigRate = 12 or lower.

This options are set graphically in Xilinx ISE Software Project Navigator by selecting the following:

- Generate Programming File > Process Properties > Configuration Options > Configuration Rate > 12 (or lower)

```
Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)


Device speed data version:  "PRODUCTION 1.33 2010-02-13".



Design Summary Report:

 Number of External IOBs                          119 out of 519    22%

   Number of External Input IOBs                  30

      Number of External Input IBUFs              30
        Number of LOCed External Input IBUFs      30 out of 30    100%


   Number of External Output IOBs                 43

      Number of External Output DIFFMs             2
        Number of LOCed External Output DIFFMs     2 out of 2     100%

      Number of External Output DIFFSs             2
        Number of LOCed External Output DIFFSs     2 out of 2     100%

      Number of External Output IOBs              39
        Number of LOCed External Output IOBs      39 out of 39    100%


   Number of External Bidir IOBs                  46

      Number of External Bidir IOBs               46
        Number of LOCed External Bidir IOBs       46 out of 46    100%


   Number of BSCANs                             1 out of 1     100%
   Number of BUFGMUXs                           5 out of 24     20%
   Number of DCMs                               1 out of 8      12%
   Number of DSP48As                            3 out of 84      3%
   Number of RAMB16BWERs                       30 out of 84     35%
   Number of Slices                          7304 out of 16640  43%
      Number of SLICEMs                      1156 out of 8320   13%

   Number of LOCed Slices                      125 out of 7304    1%
      Number of LOCed SLICEMs                   83 out of 1156    7%



Overall effort level (-ol):   High
Router effort level (-rl):    High

--------------------------------------------------------------------------------
```

12.2 Reference Design Summary for Xilinx Spartan-3A DSP 3400

```
--------------------------------------------------------------------------

platgen -p xc3sd3400afg676-4 -lang vhdl -lp x:/xxx/projects_EDK/  system.mhs
Release 11.5 - platgen Xilinx EDK 11.5 Build EDK_LS5.70 (nt)
Copyright (c) 1995-2009 Xilinx, Inc.  All rights reserved.

--------------------------------------------------------------------------

Command Line: platgen -p xc3sd3400afg676-4 -lang vhdl -lp

Running post-placement packing...

Design Summary:
Number of errors:      0
Number of warnings: 1272
Logic Utilization:
  Number of Slice Flip Flops:         6,442 out of  47,744   13%
  Number of 4 input LUTs:             8,290 out of  47,744   17%
Logic Distribution:
  Number of occupied Slices:          7,889 out of  23,872   33%
    Number of Slices containing only related logic:   7,889 out of   7,889 100%
    Number of Slices containing unrelated logic:          0 out of   7,889   0%
      *See NOTES below for an explanation of the effects of unrelated logic.
  Total Number of 4 input LUTs:       8,662 out of  47,744   18%
    Number used as logic:             6,212
    Number used as a route-thru:        372
    Number used for Dual Port RAMs:   1,892
      (Two LUTs used per Dual Port RAM)
    Number used as Shift registers:     186

  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

  Number of bonded IOBs:                119 out of     469   25%
    IOB Flip Flops:                      39
    IOB Master Pads:                      2
    IOB Slave Pads:                       2
  Number of ODDR2s used:                 44
    Number of DDR_ALIGNMENT = NONE       44
    Number of DDR_ALIGNMENT = C0          0
    Number of DDR_ALIGNMENT = C1          0
  Number of BUFGMUXs:                     5 out of      24   20%
  Number of DCMs:                         1 out of       8   12%
  Number of BSCANs:                       1 out of       1  100%
  Number of DSP48As:                      3 out of     126    2%
  Number of RAMB16BWERs:                 30 out of     126   23%
  Number of BSCAN_SPARTAN3As:             1 out of       1  100%

  Number of RPM macros:           1
Average Fanout of Non-Clock Nets:               3.56

--------------------------------------------------------------------------
```

```
Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)


Device speed data version:  "PRODUCTION 1.33 2010-02-13".



Design Summary Report:

 Number of External IOBs                          119 out of 469    25%

   Number of External Input IOBs                  30

      Number of External Input IBUFs              30
        Number of LOCed External Input IBUFs      30 out of 30    100%


   Number of External Output IOBs                 43

      Number of External Output DIFFMs             2
        Number of LOCed External Output DIFFMs     2 out of 2     100%

      Number of External Output DIFFSs             2
        Number of LOCed External Output DIFFSs     2 out of 2     100%

      Number of External Output IOBs              39
        Number of LOCed External Output IOBs      39 out of 39    100%


   Number of External Bidir IOBs                  46

      Number of External Bidir IOBs               46
        Number of LOCed External Bidir IOBs       46 out of 46    100%


   Number of BSCANs                             1 out of 1     100%
   Number of BUFGMUXs                           5 out of 24     20%
   Number of DCMs                               1 out of 8      12%
   Number of DSP48As                            3 out of 126     2%
   Number of RAMB16BWERs                       30 out of 126    23%
   Number of Slices                          7889 out of 23872  33%
      Number of SLICEMs                      1156 out of 11936   9%

   Number of LOCed Slices                     125 out of 7889    1%
      Number of LOCed SLICEMs                  83 out of 1156    7%



Overall effort level (-ol):   High
Router effort level (-rl):    High

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14 High Resolution Pictures

(a) Figure 53: TE0320 high resolution top view.

(b) Figure 54: TE0320 high resolution bottom view.

(c) Figure 55: TE0320 angle view.

18.4.1 JM4 Signals Trace Length

len. mm	FPGA pin	FPGA ball	JM4 singal	JM4	pin	JM4 singal	FPGA ball	FPGA pin	len. mm
				1	2				
26	IO_L20P_0	F15	JM4-IO01	3	4				
29	IO_L21N_0	C16	JM4-IO02	5	6				
				7	8	JM4-IO34	K12	IO_L39N_0	29
26	IO_L21P_0	D17	JM4-IO03	9	10	JM4-IO35	J12	IO_L39P_0	26
24	IO_L22N_0	C15	JM4-IO04	11	12	JM4-IO36	D8	IO_L40N_0	26
26	IO_L22P_0	D16	JM4-IO05	13	14	JM4-IO37	C8	IO_L40P_0	24
21	IO_L23N_0	A15	JM4-IO06	15	16				
20	IO_L23P_0	B15	JM4-IO07	17	18	JM4-IO38	C6	IO_L41N_0	24
22	IO_L24N_0	F14	JM4-IO08	19	20	JM4-IO39	B6	IO_L41P_0	24
18	IO_L24P_0	E14	JM4-IO09	21	22	JM4-IO40	C7	IO_L42N_0	23
				23	24	JM4-IO41	B7	IO_L42P_0	19
20	IO_L25N_0 GCLK5	J14	JM4-IO10	25	26	JM4-IO42	K11	IO_L43N_0	24
21	IO_L25P_0 GCLK4	K14	JM4-IO11	27	28	JM4-IO43	J11	IO_L43P_0	23
11	IO_L26N_0 GCLK7	A14	JM4-IO12	29	30				
11	IO_L26P_0 GCLK6	B14	JM4-IO13	31	32	JM4-IO44	D6	IO_L44N_0	15
17	IO_L27N_0 GCLK9	G13	JM4-IO14	33	34	JM4-IO45	C5	IO_L44P_0	14
16	IO_L27P_0 GCLK8	F13	JM4-IO15	35	36	JM4-IO46	B4	IO_L45N_0	15
				37	38	JM4-IO47	A4	IO_L45P_0	14
13	IO_L28N_0 GCLK11	C13	JM4-IO16	39	40	JM4-IO48	H10	IO_L46N_0	14
12	IO_L28P_0 GCLK10	B13	JM4-IO17	41	42	JM4-IO49	G10	IO_L46P_0	14
14	IO_L29N_0	B12	JM4-IO18	43	44				
14	IO_L29P_0	A12	JM4-IO19	45	46	JM4-IO50	H9	IO_L47N_0	15
27	IO_L30N_0	C12	JM4-IO20	47	48	JM4-IO51	G9	IO_L47P_0	14
30	IO_L30P_0	D13	JM4-IO21	49	50	JM4-IO52	E7	IO_L48N_0	13
				51	52	JM4-IO53	F7	IO_L48P_0	15
20	IO_L33N_0	B10	JM4-IO22	53	54	JM4-IO54	B3	IO_L51N_0	9
17	IO_L33P_0	A10	JM4-IO23	55	56	JM4-IO55	A3	IO_L51P_0	9
20	IO_L34N_0	D10	JM4-IO24	57	58				
21	IO_L34P_0	C10	JM4-IO25	59	60	JM4-IO56	C23	IO_L06N_0	36
29	IO_L35N_0	H12	JM4-IO26	61	62	JM4-IO57	D23	IO_L06P_0	42
30	IO_L35P_0	G12	JM4-IO27	63	64	JM4-IO58	A22	IO_L07N_0	36
				65	66	JM4-IO59	B23	IO_L07P_0	41
27	IO_L36N_0	B9	JM4-IO28	67	68	JM4-IO60	G17	IO_L08N_0	36
27	IO_L36P_0	A9	JM4-IO29	69	70	JM4-IO61	H17	IO_L08P_0	39
28	IO_L37N_0	D9	JM4-IO30	71	72				
34	IO_L37P_0	E10	JM4-IO31	73	74				
29	IO_L38N_0	B8	JM4-IO32	75	76				
28	IO_L38P_0	A8	JM4-IO33	77	78				
				79	80				

Table 42: trace length of signal pins of B2B connector JM4.