Trenz Electronic GmbH - TE0320-00-EV02B Datasheet

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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Not For New Designs
Module/Board Type	FPGA, USB Core
Core Processor	Spartan-3A DSP
Co-Processor	Cypress EZ-USB FX2LP
Speed	100MHz
Flash Size	4MB
RAM Size	128MB
Connector Type	B2B
Size / Dimension	2.7" x 1.9" (68mm x 48mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0320-00-ev02b

Key Features

- Industrial-grade **Xilinx Spartan-3A DSP** FPGA module (1800 k gates or 3400 k gates)
- USB 2.0 (**Hi-Speed USB**) interface with a signalling bit rate of up to 480 Mbit/s
- 32-bit wide 1 Gbit **DDR SDRAM**
- FPGA configuration through:
  - B2B connector
  - JTAG port
  - SPI Flash memory
- Large **SPI Flash** memory (for configuration and operation) accessible through:
  - B2B connector (SPI direct)
  - FPGA
  - JTAG port (SPI indirect)
  - USB bus (Firmware Upgrade Tool)
- On-board 100 MHz oscillator for high performance
- On-board 24 MHz oscillator available to user
- 3 on-board high-power, high-efficiency, switch-mode DC-DC converters capable of 3 A each
- Power supply range: 4.0 - 7.0 V
- Power supply via USB or B2B (carrier board)
- 4 LEDs, 2 push buttons, 8 DIP switches.
- Plug-on module with 2 female 1.27 mm pitch header connectors
- 109 FPGA I/O pins (+ 10 dual-purpose pins) available on B2B connectors
- Evenly spread supply pins for good signal integrity
- Assembly options for cost or performance optimization available on request

1 Block Diagram

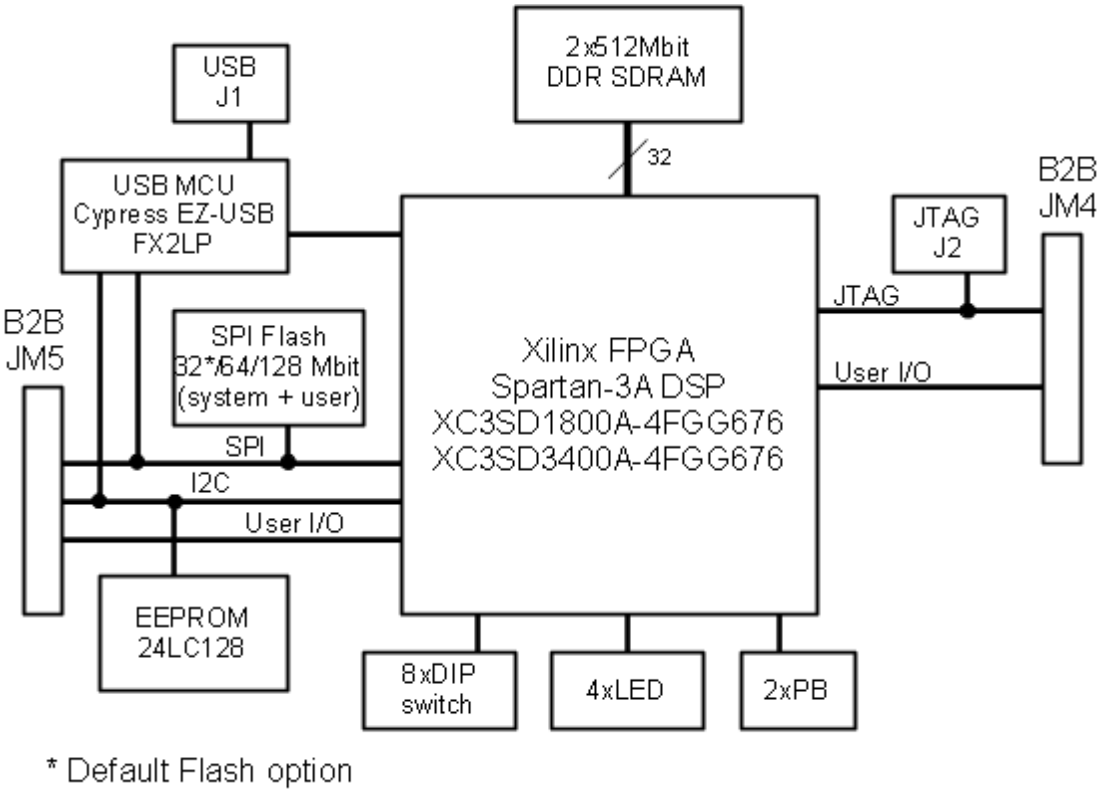


Figure 3: TE0320 block diagram

2 Module options

FPGA options

Module can be ordered with Spartan-3A DSP XC3SD1800A or XC3SD3400A chip.

Flash options

Module can be ordered with 32, 64 or 128 Mbit SPI Flash chip.

Temperature grade options

Module can be ordered in commercial or in extended (from -25 C° to +85 C°) temperature grade.

3 Specifications

- FPGA: Xilinx Spartan-3A DSP:
  - XC3SD1800A-4FGG676C, XC3SD1800A-4FGG676I or
  - XC3SD3400A-4FGG676C, XC3SD3400A-4FGG676I
- Cypress EZ-USB FX2LP™ USB microcontroller, high speed USB peripheral controller
  - CY7C68013A-56LTXC (commercial grade) or
  - CY7C68013A-56LTXI (industrial grade)
- Numonyx M25P32[1] / M25P64 / M25P128:
  low voltage, serial Flash memory with 75 MHz SPI bus interface
- 2 × 16-bit data-bus 512 Mbit DDR SDRAM (connected in parallel as a virtual 1 × 32-bit data-bus DDR SDRAM)
- Microchip Technology 24LC128I-ST
  128 kbit I2C CMOS serial EEPROM
- 3 × STMicroelectronics ST1S10:
  3 A, 900 kHz, monolithic synchronous step-down regulator
  3 A for each power rail: 1.2 V, 2.5 V, 3.3 V
- Texas Instruments TPS3705–33DGN
  processor supervisory circuits with power-fail and watchdog
- 100 MHz oscillator (system + user)
- 24 MHz oscillator (system + user)
- 2 × CviLux CBC1-80-2-M110-2P
  1.27 mm (50 mil = .050") pitch 80-pin double row socket (female) header board-to-board (B2B) connectors with key and pegs
- 109 FPGA IO Pins routed to the B2B connector
- 6-pin JTAG header
- 1 × USB mini-B receptacle (device)
- 1 × LED (system)
- 4 × LED (user)
- 2 × push button (user)
- 4 × DIP switches (system)
- 1 × slide switch (system)
- 8 × DIP switch (user)

1 Default module configuration contain 32 MBit Flash

Here there are two assembly options:

(a) if inductor L2 is not populated and the low-noise low drop-out regulator U6 is populated, VCCAUX power rail is supplied with its nominal voltage of 2.5 V. This is the recommended option for noise-sensitive circuitry such as clocking and timing infrastructures.

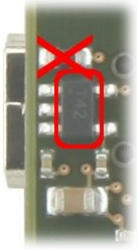


Figure 8: assembly option for VCCAUX = 2.5 V (bottom view).

(b) if the ferrite bead L2 is populated and U6 is not populated, the 3.3V power rail is simply filtered to generate VCCAUX power rail. This is the recommended option for cost-sensitive applications. In this case

(b.1) ensure the noise level on power rail VCCUAX is suitable to your application;

(b.2) avoid the connection of noise sources to power rail VCCUAX.

Figure 9: assembly option for VCCAUX = 3.3 V (bottom view).

Any other assembly combination of L2 and U6 is not allowed.

- VCCCIO0

VCCCIO0 supplies V_{CCO} to FPGA bank 0. The following assembly options are possible:

(a) if both resistors R131 and R132 are not populated, VCCCIO0 power can be supplied through pins 30 and 44 of B2B connector JM4.

Power supply inputs and outputs are made available at B2B connectors JM4 and JM5 for user applications.

Each pin of B2B connectors JM4 and JM5 is capable of a maximum current of 1.0 A.

power-rail name	nominal voltage (V)	maximum current (A)	power source	system supply	user supply
Vb2b	4.0 to 7.0	4.0 (4 pin × 1.0 A/pin)	JM5	module	-
Vusb	5.0	0.5	J1	module	-
Vsup	4.0 to 7.0	< 0.5	Vusb	3 × DC/DC DC/DC sync power-fail	JM5 (≤1.0 A)
		< 4	Vb2b		
3.3V	3.3	3.0	Vsup ► DC/DC	module	JM4 (≤1.0 A) JM5 (≤1.0 A)
2.5V	2.5	3.0	Vsup ► DC/DC	DDR SDRAM	JM5 (≤1.0 A)
1.2V	1.2	3.0	Vsup ► DC/DC	VCCINT	JM5 (≤1.0 A)
VCCAUX	2.5	0.3	3.3V ► LDO	VCCAUX	JM4 (≤1.0 A)
	3.3	< 3.0	3.3V		
VCCCIO0	2.5	< 3.0	2.5V	VCCO (bank 0)	JM4 (≤1.0 A)
	3.3	< 3.0	3.3V		JM4 (≤1.0 A)
	1.10 to 3.60	2.0 (2 pin × 1.0 A/pin)	JM4 (30 + 44)		JM4 (30 / 44)

Table 1: On-board power rails summary.

5.4 Power Supervision

5.4.1 Power-on Reset

During power-on, the /RESET line is first asserted. Thereafter, the supply voltage supervisor monitors the power supply rail 3.3V and keeps the /RESET line active (low) as long as the rail remains below the threshold voltage (2.93 V). An internal timer delays the return of the /RESET line to the inactive state (high) to ensure proper system reset. The delay time of 200 ms starts after the rail has risen above the threshold voltage.

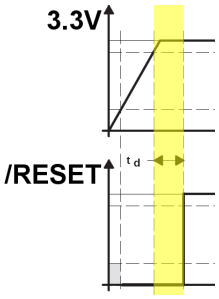


Figure 13: Power-on reset with fixed delay time of 200 ms.

After this delay, the /RESET line is reset high and the FPGA configuration can

6 Inputs and Outputs

6.1 Board-to-Board Connectors

The module has two B2B (board-to-board) connectors (JM4 and JM5) with the following features:

- gender: female
- overall number of contacts: 160
- contacts per connector: 80
- rows per connector: 2
- pitch: 1.27 mm = 50 mil = .050"

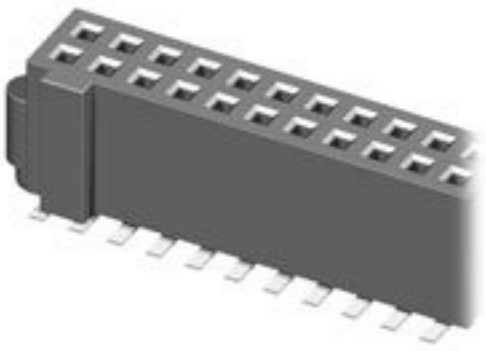


Figure 15: Board to board connector assembled on the TE0320.

Trenz Electronic recommends to mate the standard B2B connectors with the following ones:

- 2 x W+P 6110-080-00-10-PPTR
  1.27 mm (50 mil = .050") pitch 80-pin double row boxed plug (male) header board-to-board (B2B) connectors.

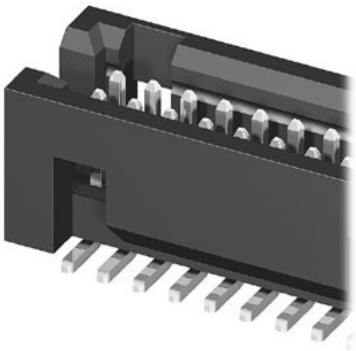


Figure 16: Close-up of the recommended mating B2B connector.

This connector couple offers the following two advantages:

- the module is protected against polarity inversion;
- the connection presents a mechanical resistance sufficient for most applications.

Ordering codes for connectors JM4 / JM5 and their mating connectors are given

detailed in Table 3. Ensure resistors R3 and R4 are populated to connect USB B2B pins B2B_D_P and B2B_D_P to USB lines D_P and D_P respectively.

pin number	pin name	signal name	description
4	B2B_D_P	D_P	USB data + (D+)
6	B2B_D_N	D_N	USB data - (D-)

Table 3: USB pins at B2B connector JM4.

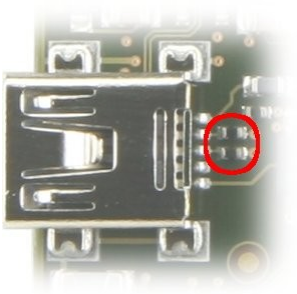


Figure 23: Resistors R3 and R4 required for USB communication over B2B connector JM4.

6.3 JTAG Interface

6.3.1 JTAG connector J2

JTAG signals are available on the gender-inverted standard 6-pin JTAG header connector J2 as shown in Figure 24.

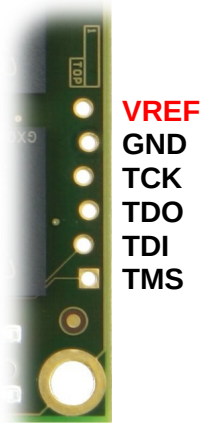


Figure 24: JTAG connector J2.

To connect your computer to JTAG connector J2 you typically need

- a JTAG cable with standard 6-pin JTAG female header;
- a 2.54 mm pitch 1 × 6 pin gender changer header.

Some examples of JTAG cable set are listed in Table 4.

JTAG cable	flying leads	software	gender changer
Xilinx Platform Cable USB	included	Xilinx iMPACT	1 × 6 pin
Digilent XUP USB-JTAG Programming Cable	XUP Fly Wire Assembly	Xilinx iMPACT	1 × 6 pin

6.3.2 JTAG lines at B2B connector JM4

JTAG signal lines are also available at B2B connector JM4. See Table 40 for additional information on these signals.

6.4 I2C bus

TE0320 has a flexible I2C bus on-board as outlined in Figure 28.

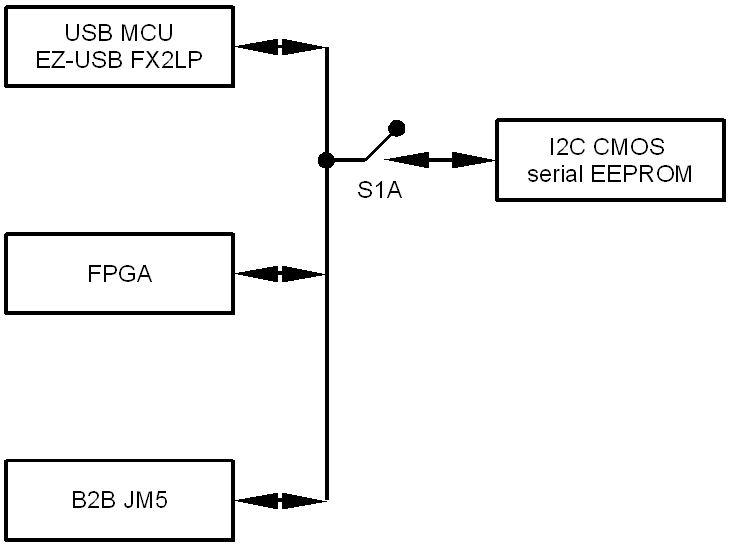


Figure 28: I2C bus topology.

The I2C signals on the TE0320 are listed and described in Table 5.

name	definition	description
SDA	serial data	This is a bidirectional pin used to transfer addresses and data into and out of a device.
SCL	serial clock	This signal is used to synchronize the data transfer to and from a device.

Table 5: I2C signals summary.

The I2C bus is typically used by the USB microcontroller to write USB firmware to the serial EEPROM. In this case,

- the I2C port of the FPGA must be set in slave mode (SCL pin as input),
- the device attached to the I2C port of B2B JM5 connector must be set to slave mode.

The USB microcontroller can operate just in I2C master mode (default operation). If the user wants to set another device attached to the I2C bus as master device, the USB microcontroller shall three-state (Z = high impedance) its SCL and SDA pins.

If the FPGA is set to I2C master mode, it can write to or read from serial EEPROM (always slave mode) and B2B connector JM5 (attached device set to slave mode).

If the device attached to the I2C port of B2B JM5 connector is set to master mode, it can write to or read from serial EEPROM (always slave mode) and FPGA I2C port (set to slave mode).

Possible I2C operation modes are summarized in Table 6.

core	EZ-USB FX2LP	FPGA (SDA = I/O)	B2B JM5	serial EEPROM
default	**master**	slave SCL = I	slave	slave
custom	inactive SCL = SDA = Z	**master** SCL = O	slave	slave
custom	inactive SCL = SDA = Z	slave SCL = I	**master**	slave

Table 6: I2C bus modes summary.

TE0320 reference design includes an HDL core managing the fast mode (400 kHz) I2C communication between the Xilinx MicroBlaze embedded soft-processor and the EZ-USB FX2LP USB microcontroller.

I2C pins on B2B connector JM5 cannot be used as GPIOs (general purpose I/Os),
as these bus signals are pulled up to 3.3V.

6.5 SPI bus

TE0320 has a flexible SPI bus on-board as outlined in Figure 29.

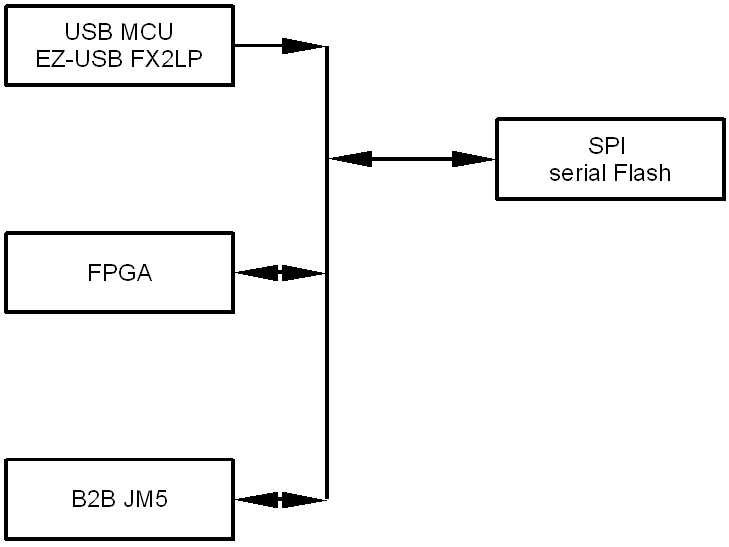


Figure 29: SPI bus topology.

SPI signals on the TE0320 are listed and described in Table 7.

name	definition	description
SPI_Q	serial data output	This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of SPI_/C.
SPI_D	serial data input	This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of SPI_/C
SPI_/C	serial clock	This input signal provides the timing of the serial interface. Instructions, addresses, or data present at SPI_D are latched on the rising edge of SPI_/C. Data on SPI_Q changes after the falling edge of SPI_/C.
SPI_/S	chip select	When this input signal is **high,** the device is **disabled** and SPI_Q is at high impedance (Z).
		When this input signal is **low**, the device is **enabled.**
		After power-up, a falling edge on SPI_/S is required prior to the start of any instruction to the Flash memory.

Table 7: SPI signals summary.

SPI signal pin-out of the TE0320 is summarized in Table 8.

name	FPGA ball	JM5 pin
SPI_Q	AF24	18
SPI_D	AB15	12
SPI_/C	AE24	22
SPI_/S	AA7	20

Table 8: SPI pin-out summary.

SPI pins on B2B connector JM5 cannot be used as GPIOs (general purpose I/Os).

The SPI bus can be used during configuration and operation in a plurality of ways as summarized respectively in Table 9 and Table 10. Any other usage of the SPI bus is neither supported nor recommended.

6.5.1 SPI bus for configuration

The SPI bus is used for configuration in two ways by default:

(d) EZ-USB ► Flash
the USB microcontroller (master) writes the PROM file (containing the FPGA configuration bitstream) to the SPI serial Flash memory (slave)

(e) FPGA ◄ Flash
the FPGA (master) configures itself in Master SPI mode from the SPI serial Flash memory (slave).

In case (a), the FPGA shall be turned off to release its shared SPI pins.

In case (b), the USB microcontroller shall three-state (Z = high impedance) its shared SPI pins.

Warning! on some boards, PB1 and PB2 labels might be exchanged. Please take Figure 31 as reference.

6.8 Switches

TE0320 is provided with the following slide switches:

- S1: 4 x DIP slide switches (system)
- S2: 1 x slide switch (system)
- S5: 8 × DIP slide switches (user)

6.8.1 DIP Slide Switches S1[A:D]

TE0320 is provided with 4 system DIP slide switches as shown in Figure 32: S1A, S1B, S1C, S1D.

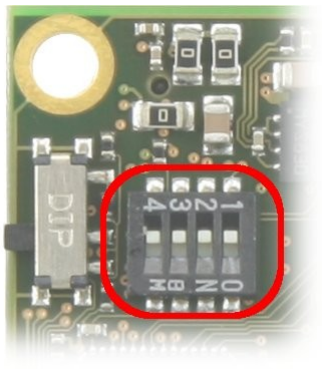


Figure 32: DIP slide switches S1[A:D].

Please note the 4 switch labels are on one side and the <ON> label is on the opposite side.

DIP slide switches S1[A:D] condition the value of some system signals as described in Table 13.

switch	S1 label	signal name	<OFF>	<ON>
S1A	1	EEPROM serial data	the USB microcontroller CANNOT read / write the serial EEPROM	the USB microcontroller can read / write the serial EEPROM
S1B	2	M2	mode pin M2 = 1	M2 = 0
S1C	3	M1	mode pin M1 = 1	M1 = 0
S1D	4	/MR (master reset)	module reset	module running

Table 13: S1X settings description.

DIP slide switches S1A is ON by default, to allow the USB microcontroller to read the serial EEPROM and enumerate as a custom/specific USB device. When DIP slide switches S1A is ON, the USB microcontroller can (re)write the serial EEPROM to, for example, store a (new) custom/specific firmware. When DIP slide switch is OFF, the USB microcontroller cannot read the serial EEPROM and enumerates as a generic USB device.

6.8.2 Slide Switch S2

TE0320 is provided with a slide switch S2.

Figure 33: Slide switch S2 (angle view).

Slide switch S2 conditions the value of signal PS_EN. Signal PS_EN enables (high) or disables (low) power rails 2.5V and 1.2V. According to the corresponding assembly option, power rail VCCCIO0 can depend or not on the 2.5V power rail. Power-rail 3.3V is not controlled by signal PS_EN and is unconditionally enabled. Table 14 summarizes all switching options implied by slide switch S2 under the standard assembly option.

power rail	S2= PON	S2 = FX2 PON FX2_PS_EN = 1	S2 = FX2 PON FX2_PS_EN = 0
2.5V	on	on	off
1.2V	on	on	off
VCCCIO0 (= 2.5V)	on	on	off
VCCCIO0 (= 3.3V)	on	on	on

Table 14: Slide switch S2 settings overview.

6.8.2.1 Slide Switch S2 = PON

When slide switch S2 is in the right position (PON = power rails unconditionally on), signal PS_EN is set to power rail 3.3V. Thus power rails 2.5V and 1.2V are unconditionally enabled.

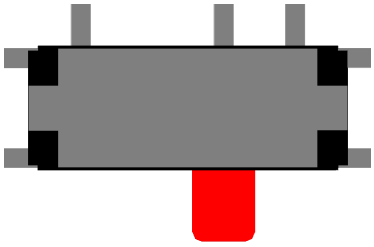


Figure 34: S2 on position PON.

6.8.2.2 Slide Switch S2 = FX2 PON

When slide switch S2 is in the left position (FX2 PON = power rails conditionally on depending on signal FX2_PS_EN), signal PS_EN is set to signal FX2_PS_EN driven by the EZ-USB FX2LP USB microcontroller under user control.

When the EZ-USB FX2LP USB microcontroller sets signal FX2_PS_EN (high), power rails 2.5V and 1.2V are enabled. This setting can be useful for dynamic

Assembly option when resistor R17 populated and R19 not populated is equivalent to slide switch S2 permanently set to FX2 PON.

Figure 38: Assembly option: S2 = FX2 PON.

Any other assembly options of R17 and R19 are not allowed.

6.8.3 DIP Slide Switches S5[A:H]

TE0320 is provided with 8 user DIP slide switches as shown in Figure 39: S5A to S5H.

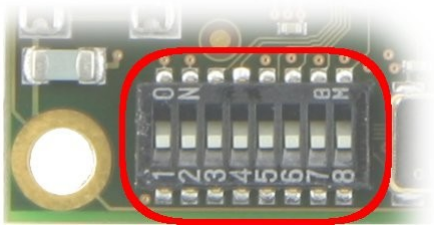


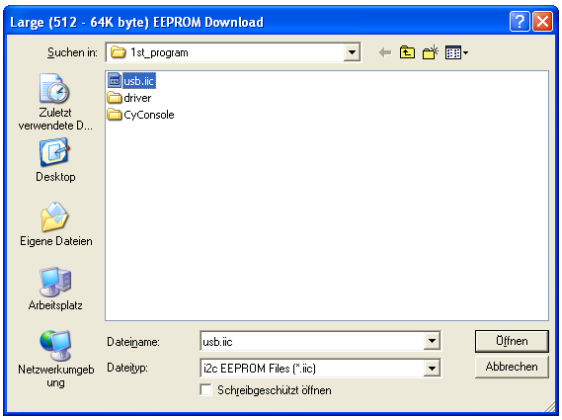
Figure 39: DIP slide switches S5[A:H].

Please note the 8 switch labels are on one side and the <ON> label is on the opposite side.

DIP slide switches S5[A:H] condition the value of some user signals as described in Table 15.

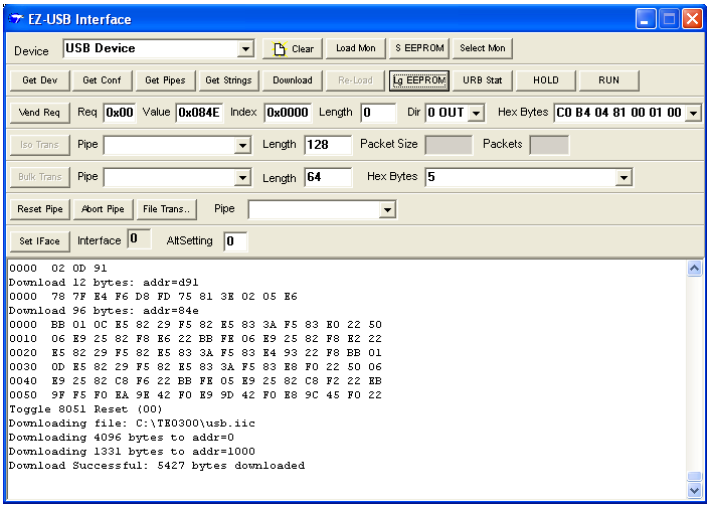
switch	S5 label	signal name	FPGA ball	FPGA pin	FPGA bank
S5A	1	US1	F24	IO_L54N_1	1
S5B	2	US2	E24	IO_L56P_1	1
S5C	3	US3	E26	IO_L60P_1	1
S5D	4	US4	D24	IO_L61N_1	1
S5E	5	US5	D26	IO_L60N_1	1
S5F	6	US6	D25	IO_L61P_1	1
S5G	7	US7	C26	IO_L63P_1 A22	1
S5H	8	US8	C25	IO_L63N_1 A23	1

Table 15: S1X settings description.



Select the *step2_factory/USB.iic* file in the TE0320 software package and press the “Open” button to start writing to EEPROM.

The display window shows the process of IIC file being programmed into the EEPROM and displays “Downloaded Successful” when completed.



10.2.3 specific USB device driver installation

TE0320 users are normally required to perform this step when a Trenz Electronic module with DEWESoft technology is connected to a computer on which the DEWESoft specific USB device driver is not yet installed.

Disconnect the TE0320 from the USB bus or leave it unconnected if it already is.

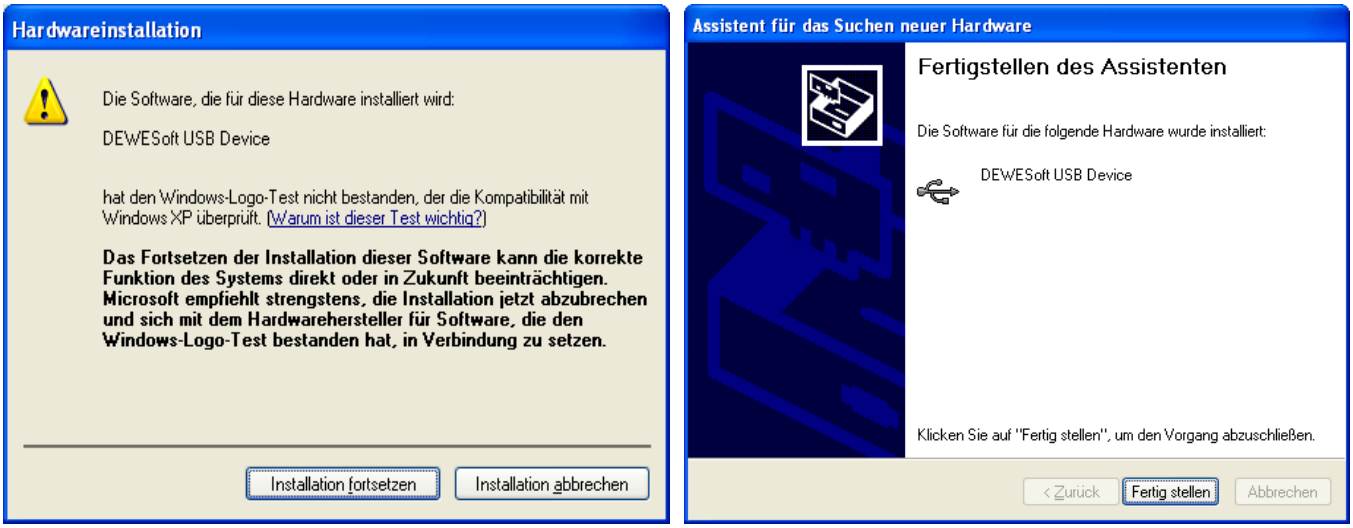
Ensure that DIP switch S1 is set as follows:

- S1A = ON

  this connect the serial data line between the USB microcontroller and the large EEPROM; in so doing, the USB microcontroller is able to read the large EEPROM and enumerate as a DEWESoft specific USB device
- S1B and S1C = do not care

  configuration mode is irrelevant for this step
- S1D = OFF

  master reset disabled



After successful installation of the specific device driver, TE0320 should be identified as “DEWESoft USB Device” and the Device Manager panel should look like Figure 50.

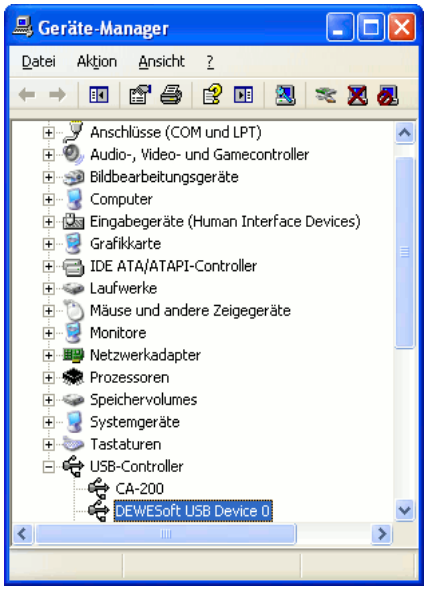


Figure 50: device manager after successful installation of the specific device driver.

Now the EZ-USB FX2LP USB microcontroller can be controlled from a computer by the DEWESoft API.

10.2.4 FWU file generation

In order to generate the FWU file you shall

(a) generate a bit-stream file from your Xilinx EDK design;

(b) generate a PROM file from the bit-stream file;

(c) generate a FWU file from the PROM file.

10.2.4.1 bit-stream file from your Xilinx EDK design

In order to generate a `.bit` bit-stream file from your Xilinx EDK design, you shall

```
Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)


Device speed data version:  "PRODUCTION 1.33 2010-02-13".



Design Summary Report:

 Number of External IOBs                          119 out of 519    22%

   Number of External Input IOBs                  30

      Number of External Input IBUFs              30
        Number of LOCed External Input IBUFs      30 out of 30    100%


   Number of External Output IOBs                 43

      Number of External Output DIFFMs             2
        Number of LOCed External Output DIFFMs     2 out of 2     100%

      Number of External Output DIFFSs             2
        Number of LOCed External Output DIFFSs     2 out of 2     100%

      Number of External Output IOBs              39
        Number of LOCed External Output IOBs      39 out of 39    100%


   Number of External Bidir IOBs                  46

      Number of External Bidir IOBs               46
        Number of LOCed External Bidir IOBs       46 out of 46    100%


   Number of BSCANs                             1 out of 1     100%
   Number of BUFGMUXs                           5 out of 24     20%
   Number of DCMs                               1 out of 8      12%
   Number of DSP48As                            3 out of 84      3%
   Number of RAMB16BWERs                       30 out of 84     35%
   Number of Slices                          7304 out of 16640  43%
      Number of SLICEMs                      1156 out of 8320   13%

   Number of LOCed Slices                      125 out of 7304    1%
      Number of LOCed SLICEMs                   83 out of 1156    7%



Overall effort level (-ol):   High
Router effort level (-rl):    High

--------------------------------------------------------------------------------
```

13 Verification

The quickest way to test most module functions is to execute the sample DMA test available in the `TE0320_API_Example\Release` folder of the TE0320 software package. Hereunder is reported a sample trace of a successful execution.

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
1
```

```
1
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
2
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
5
```

```
fifo_error: 0
current_mode: 1
flash_busy: 0
fpga_prog.: 170
booting: 1
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
```

```
6
```

```
Major version: 1
Minor version: 7
Device hi: 1
Device lo: 1
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
7
```

```
INT# : 1
Major version: 7
Minor version: 1
Release version: 2
Build version: 24
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
8
```

```
EP2 FIFO CS: 0x04
EP4 FIFO CS: 0x04
EP6 FIFO CS: 0x04
EP8 FIFO CS: 0x04
EP2 FIFO BCH: 0x00
EP4 FIFO BCH: 0x00
EP6 FIFO BCH: 0x00
EP8 FIFO BCH: 0x00
```

```
TE0320 DLL Example 1.0
        1 - Get number of modules
        2 - Connect module No 0
        3 - Connect module No 1
        4 - Disconnect
        5 - Get FX2 status
        6 - Get FX2 version
        7 - Get FPGA firmware version
        8 - Get FX2 FIFO Status
        9 - Reset FX2 FIFO Status
        w - Write high speed data (FPGA RX)
        r - Read high speed data (FPGA TX)
        0 - Exit
```

14 High Resolution Pictures

(a) Figure 53: TE0320 high resolution top view.

(b) Figure 54: TE0320 high resolution bottom view.

(c) Figure 55: TE0320 angle view.

Signal name	FPGA pin
VAR0	F17
VAR1	K16
VAR2	J16
VAR3	E17
VAR4	D20
VAR5	A20

Table 37: Assembly variants pins

To define low (zero) level VAR pin connected to ground rail through zero resistor, to define high (one) level VAR pin left float (open). These pins should be configured with "pullup" option in user design.

Available module assembly variants listed in Table 38.

VAR5	VAR4	VAR3	VAR2	VAR1	VAR0	Variant
1	1	1	1	1	1	EV01
1	1	1	1	1	0	EV02

Table 38: Module assembly variants

15.3 Availability

For the latest product details and available options, please visit

www.trenz-electronic.de

To order or obtain information, e.g. on pricing or delivery, please visit:

shop.trenz-electronic.de

19 Glossary of Abbreviations and Acronyms

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

A CAUTION notice denotes a risk. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in a fault. (undesired condition that can lead to an error) Do not proceed beyond a CAUTION notice until the indicated conditions are fully understood and met.

API	application programming interface
B2B	board-to-board
DSP	digital signal processing; digital signal processor
EDK	Embedded Development Kit
FUT	Firmware Upgrade Tool
FWU	Firmware Upgrade file
IOB	input / output blocks; I/O blocks
IP	intellectual property
ISP	In-System Programmability
PB	push button
SDK	Software Development Kit
TE	Trenz Electronic
XPS	Xilinx Platform Studio