Trenz Electronic GmbH - TE0320-00-EV02I Datasheet

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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Not For New Designs
Module/Board Type	FPGA, USB Core
Core Processor	Spartan-3A DSP
Co-Processor	Cypress EZ-USB FX2LP
Speed	100MHz
Flash Size	4MB
RAM Size	128MB
Connector Type	B2B
Size / Dimension	2.7" x 1.9" (68mm x 48mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0320-00-ev02i

Table of Contents

5 Power Supply

5.1 Power Supply Range

The power supply range of TE0320 is 4.0 V to 7.0 V.

5.2 Power Supply Sources

TE0320 can be power supplied in two ways:

- through USB connector J1,
- through B2B connector JM5 (pins 1 to 4).

The power supply source is determined by assembly option. See Figure 5.

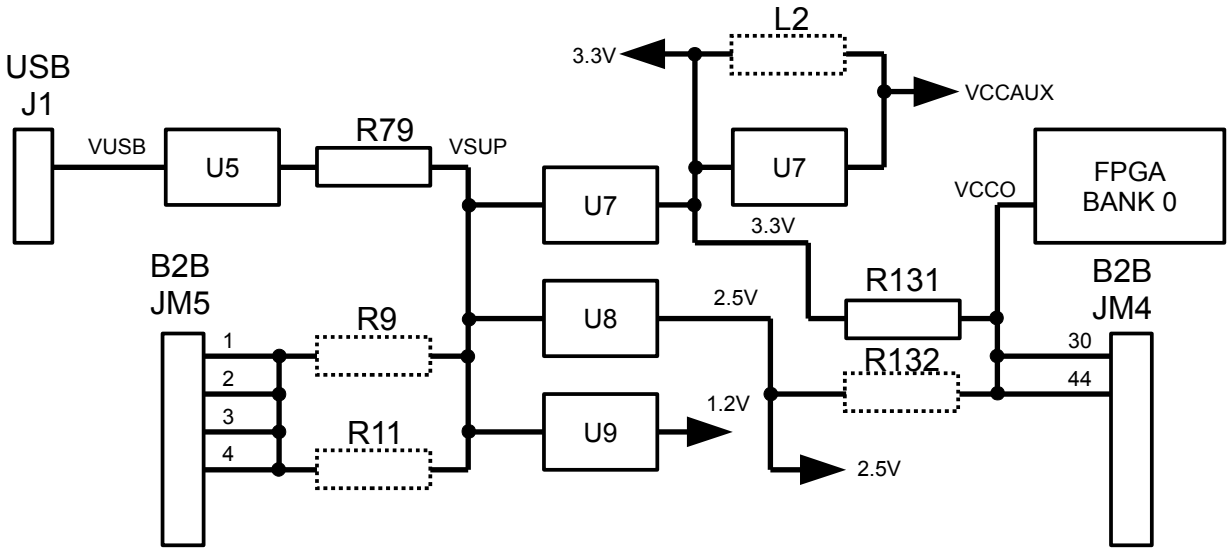


Figure 5: Power supply options diagram

If resistors R9 and R11 are populated and R12 is not populated, then TE0320 is power supplied through JM5 (B2B connector).

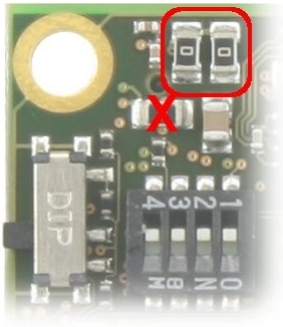


Figure 6: assembly combination for power supply through JM5.

If resistors R9 and R11 are not populated and R12 is populated, then TE0320 is power supplied through J1 (USB bus).

Figure 10: assembly option for VCCAUX = off (bottom view).

Pins 30 and 44 of JM4 are power supply **inputs** in this case.

(b) if resistor R131 is not populated and R132 is populated, VCCCIO0 power rail is set to power rail 2.5V (nominal voltage = 2.5 V).

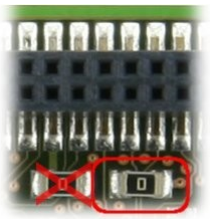


Figure 11: assembly option for VCCAUX = 2.5 V (bottom view).

Pins 30 and 44 of JM4 are power supply **outputs** in this case.

(c) if resistor R131 is populated and R132 is not populated, VCCCIO0 power rail is set to power rail 3.3V (nominal voltage = 3.3 V). This is the default.

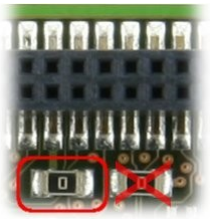


Figure 12: assembly option for VCCCIO0 = 3.3 V (bottom view).

Pins 30 and 44 of JM4 are power supply **outputs** in this case.

Assembly option where both R131 and R132 are populated is not allowed.

1.2 V, 2.5 V and 3.3 V voltage rails are provided by corresponding step-down regulator DC/DC converters, each one capable of providing up to 3 A of output current. These three regulators are synchronized to switch with 120° phase lag, to improve EMC, and to reduce input ripple. The synchronization circuit can be omitted in cost sensitive applications (please contact Trenz Electronic).

start. When the rail voltage drops below the threshold voltage, the /RESET line becomes active (low) again.

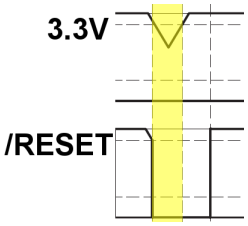


Figure 14: Reset assertion on power drop with fixed delay time of 200 ms.

5.4.2 Power Fail

TE0320 integrates a power-fail comparator which can be used for low-battery detection, power-fail warning, or for monitoring Vsup power rail.

An additional power-fail circuit can be used, to monitor the input voltage. At 4.4V, a power-fail signal (/PFO) is sent to the FPGA. Should you wish or need another threshold voltage, please contact Trenz Electronic.

6.3.2 JTAG lines at B2B connector JM4

JTAG signal lines are also available at B2B connector JM4. See Table 40 for additional information on these signals.

6.4 I2C bus

TE0320 has a flexible I2C bus on-board as outlined in Figure 28.

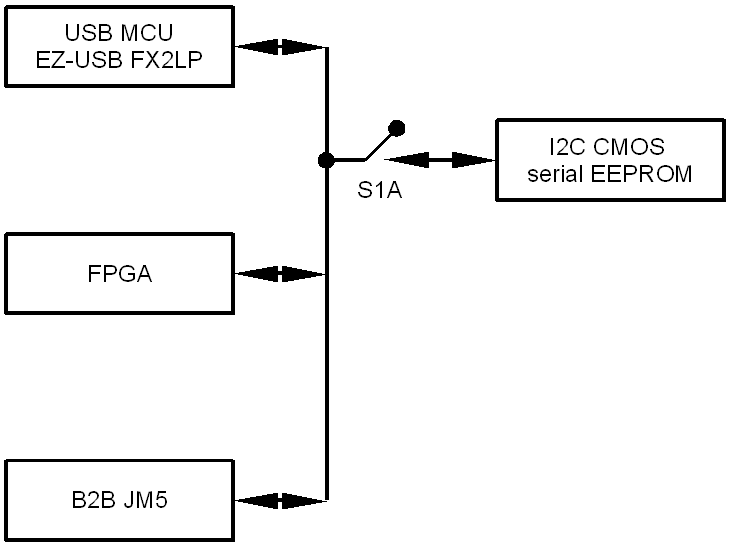


Figure 28: I2C bus topology.

The I2C signals on the TE0320 are listed and described in Table 5.

name	definition	description
SDA	serial data	This is a bidirectional pin used to transfer addresses and data into and out of a device.
SCL	serial clock	This signal is used to synchronize the data transfer to and from a device.

Table 5: I2C signals summary.

The I2C bus is typically used by the USB microcontroller to write USB firmware to the serial EEPROM. In this case,

- the I2C port of the FPGA must be set in slave mode (SCL pin as input),
- the device attached to the I2C port of B2B JM5 connector must be set to slave mode.

The USB microcontroller can operate just in I2C master mode (default operation). If the user wants to set another device attached to the I2C bus as master device, the USB microcontroller shall three-state (Z = high impedance) its SCL and SDA pins.

If the FPGA is set to I2C master mode, it can write to or read from serial EEPROM (always slave mode) and B2B connector JM5 (attached device set to slave mode).

If the device attached to the I2C port of B2B JM5 connector is set to master mode, it can write to or read from serial EEPROM (always slave mode) and FPGA I2C port (set to slave mode).

Possible I2C operation modes are summarized in Table 6.

name	definition	description
SPI_Q	serial data output	This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of SPI_/C.
SPI_D	serial data input	This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of SPI_/C
SPI_/C	serial clock	This input signal provides the timing of the serial interface. Instructions, addresses, or data present at SPI_D are latched on the rising edge of SPI_/C. Data on SPI_Q changes after the falling edge of SPI_/C.
SPI_/S	chip select	When this input signal is **high,** the device is **disabled** and SPI_Q is at high impedance (Z).
		When this input signal is **low**, the device is **enabled.**
		After power-up, a falling edge on SPI_/S is required prior to the start of any instruction to the Flash memory.

Table 7: SPI signals summary.

SPI signal pin-out of the TE0320 is summarized in Table 8.

name	FPGA ball	JM5 pin
SPI_Q	AF24	18
SPI_D	AB15	12
SPI_/C	AE24	22
SPI_/S	AA7	20

Table 8: SPI pin-out summary.

SPI pins on B2B connector JM5 cannot be used as GPIOs (general purpose I/Os).

The SPI bus can be used during configuration and operation in a plurality of ways as summarized respectively in Table 9 and Table 10. Any other usage of the SPI bus is neither supported nor recommended.

6.5.1 SPI bus for configuration

The SPI bus is used for configuration in two ways by default:

(d) EZ-USB ► Flash
the USB microcontroller (master) writes the PROM file (containing the FPGA configuration bitstream) to the SPI serial Flash memory (slave)

(e) FPGA ◄ Flash
the FPGA (master) configures itself in Master SPI mode from the SPI serial Flash memory (slave).

In case (a), the FPGA shall be turned off to release its shared SPI pins.

In case (b), the USB microcontroller shall three-state (Z = high impedance) its shared SPI pins.

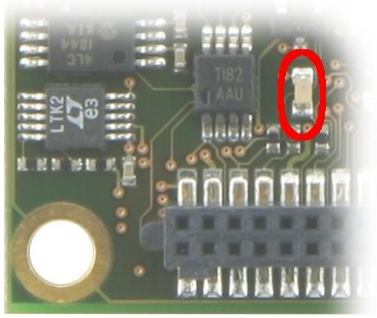


Figure 30: DONE LED D1 (bottom side).

6.6.2 User LEDs D[5:8]

TE0320 is provided with 4 user LEDs. A LED is lit when the corresponding signal listed in Table 11 is set high (logical 1).

LED	signal	FPGA ball	FPGA pin	bank
D5	UL1	R20	IO_L22N_1	1
D6	UL2	V23	IO_L21P_1	1
D7	UL3	R19	IO_L22P_1	1
D8	UL4	U24	IO_L23N_1 VREF_1	1

Table 11: user LEDs signal details..

6.7 Push-Buttons S[3:4]

TE0320 is provided with 2 user buttons. A signal listed in Table 12 is set low (logical 0) when a push button is pressed, and vice-versa.

switch	signal	FPGA ball	FPGA pin	bank	default input	input when pressed
S3	PB1	U23	IO_L23P_1	1	logical 1	logical 0
S4	PB2	R22	IO_L25N_1	1	logical 1	logical 0

Table 12: user push-buttons signal details.

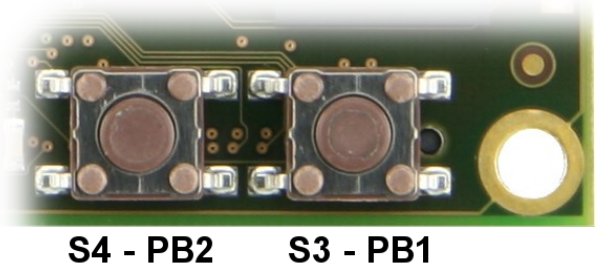


Figure 31: push buttons PB1 and PB2.

full power operation.

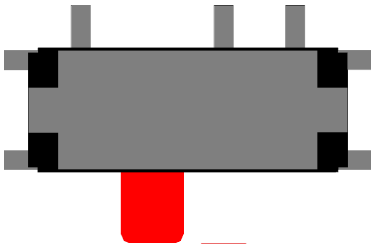


Figure 35: S2 on position FX2 PON (FX2_PS_EN = high).

When the EZ-USB FX2LP USB microcontroller resets signal FX2_PS_EN (low), the following components are switched off:

- FPGA core logic (1.2V)
- DDR SDRAM (2.5V)
- FPGA bank 3 (2.5V)
- VREF (2.5V)
- VCCCIO0 (2.5V) FPGA bank 0

This setting can be useful for dynamic **low power** operation.

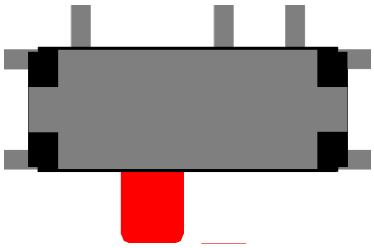


Figure 36: S2 on position FX2 PON (FX2_PS_EN = low).

6.8.2.3 Alternate Assembly Options for Slide Switch S2

Slide switch S2 can be replaced by one resistors in the following cases:

- cost sensitive applications
- applications where just one position of S2 is required
- application where switching of S2 is not allowed.

Assembly option when resistor R17 not populated and R19 populated is equivalent to slide switch S2 permanently set to PON.

Figure 37: assembly option: S2 = PON.

7 Timing

7.1 Main Clock Oscillator

The module has a main SMD clock oscillator providing a clock source for the FPGA as detailed in Table 3.

signal	FPGA pin	FPGA ball	FPGA bank
MAINCLK	IO_L27N_2 GCLK1	AA14	2

Table 16: Main clock signal details.

Standard frequency is 100 MHz. Should you wish or need another main clock oscillator frequency, please contact Trenz Electronic. The lower the main clock frequency, the lower the module power consumption. Moreover, as the main clock is preferably used as DDR SDRAM clock, a lower clock frequency makes easier for the development tools to meet the timing requirements (particularly for DDR SDRAM).

7.2 24 MHz Clock Oscillator

The module has a 24 MHz SMD clock oscillator providing a clock source for both the EZ-USB FX2LP USB microcontroller (XTALIN) and the FPGA as detailed in Table 17.

signal	FPGA pin	FPGA ball	FPGA bank
24MHZ1	IO_L28N_2 GCLK3	AE14	2

Table 17: 24 MHz clock signal details.

7.3 Interface Clock (IFCLK)

The IFCLK line synchronizes the communication between the EZ-USB FX2LP USB microcontroller and the FPGA as detailed in Table 18.

signal	FPGA pin	FPGA ball	FPGA bank
IFCLK	IO_L31N_1 TRDY1 RHCLK3	P25	1

Table 18: Interface clock signal details.

7.4 Digital Clock Manager (DCM)

The DCMs of the FPGA can be used to synthesize arbitrary clock frequencies from any on-board clock network, differential clock input pair or single-ended clock input. For further reference, please read Xilinx DS485:Digital Clock Manager (DCM) Module and the DCM chapter in Xilinx UG331: Spartan-3 Generation FPGA User Guide.

7.5 Watchdog

TE0320 has a watchdog timer that is periodically triggered by a positive or negative transition of the watchdog input (WDI) signal. When the supervising system fails to retrigger the watchdog circuit within the time-out interval (min 1.1

8 Memories

The TE0300 has three on-board memories:

- DDR SDRAM
- SPI Flash
- serial EEPROM

8.1 DDR SDRAM

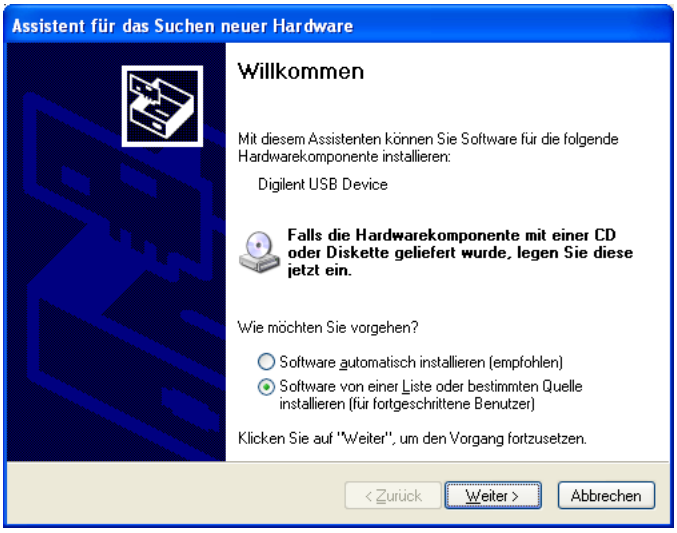
TE0320 modules have two 512Mb DDR SDRAM components each with a 16-bit data-bus connected in parallel to FPGA bank 3 as a virtual 512Mb DDR SDRAM component with a 32-bit data-bus. Memory available in industrial and commercial temperature grade.

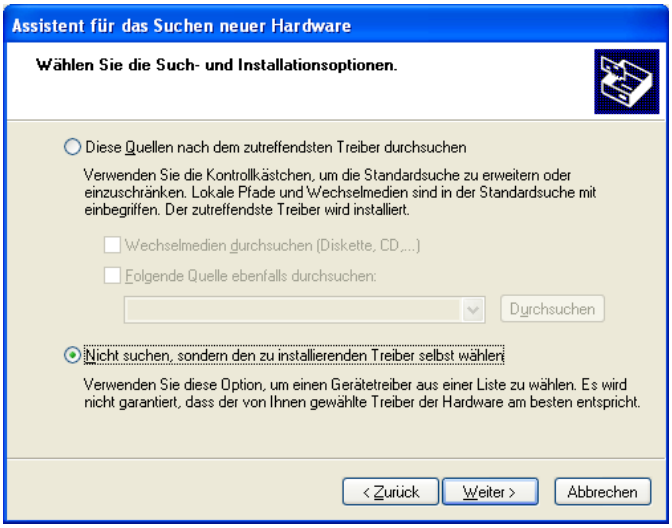
8.2 SPI Flash

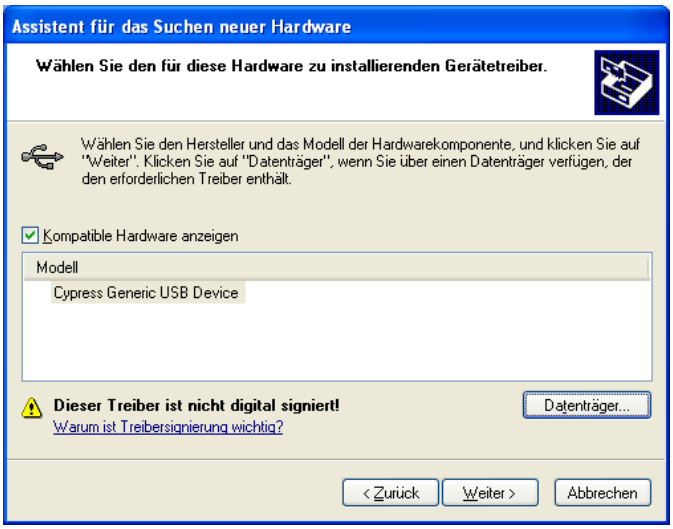
TE0320 has an STMicroelectronics M25P32/64/128 (32/64/128-Mbit), low voltage, serial Flash memory with 75 MHz SPI bus interface for configuration and operating storage accessible through USB or SPI. Default module configuration contain 32 Mbit Flash chip M25P32, others available by request.

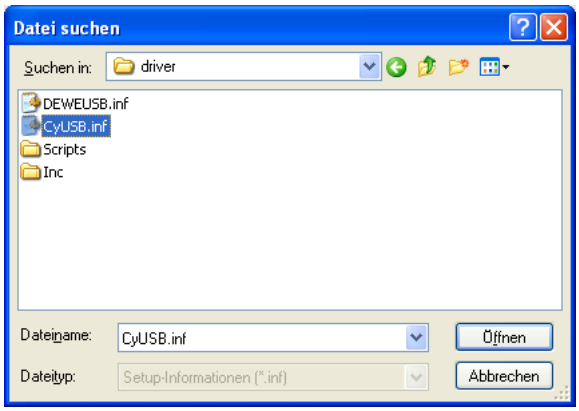
8.3 Serial EEPROM

TE0300 modules have a Micron Technology 24LC128 128 kbit I2C CMOS Serial EEPROM for EZ-USB FX2 firmware, vendor ID and device ID storage accessible through the EZ-USB FX2 microcontroller.

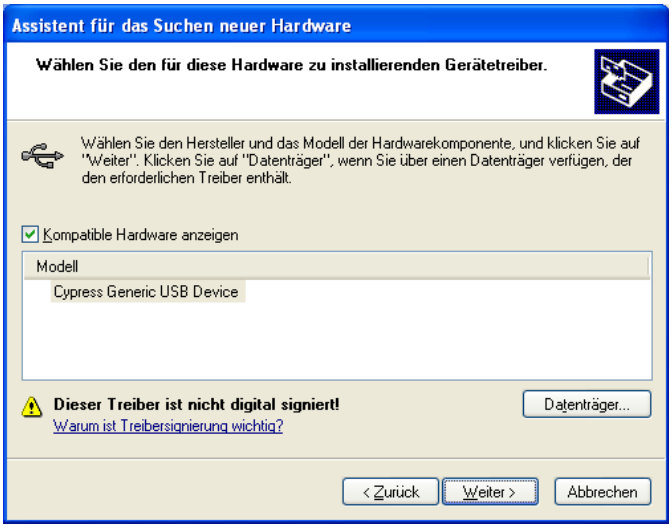

Assistent für das Suchen neuer Hardware
Willkommen
Mit diesem Assistenten können Sie Software für die folgende Hardwarekomponente installieren:
Digilent USB Device
Falls die Hardwarekomponente mit einer CD oder Diskette geliefert wurde, legen Sie diese jetzt ein.
Wie möchten Sie vorgehen?
Software automatisch installieren (empfohlen)
Software von einer Liste oder bestimmten Quelle installieren (für fortgeschrittene Benutzer)
Klicken Sie auf "Weiter", um den Vorgang fortzusetzen.
< Zurück
Weiter >
Abbrechen

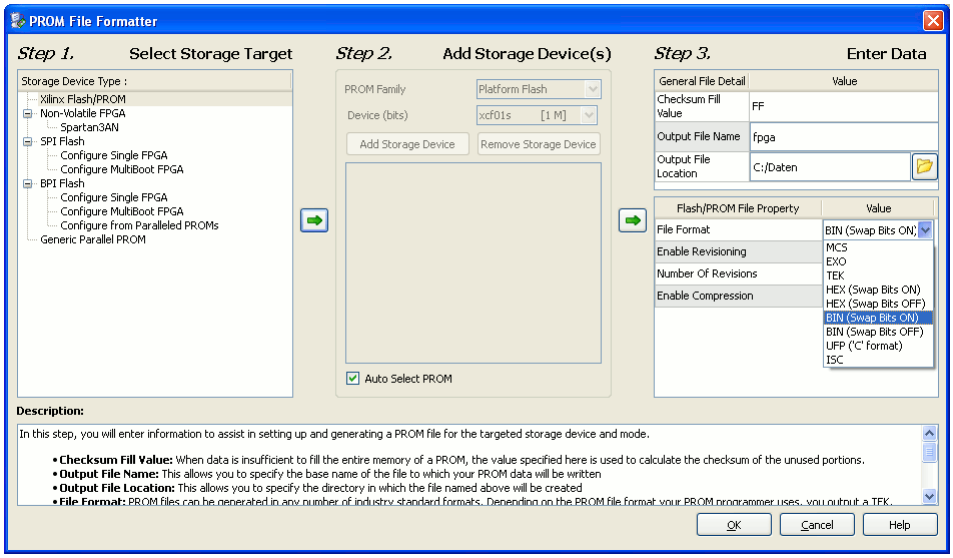

Assistent für das Suchen neuer Hardware
Wählen Sie die Such- und Installationsoptionen.
Diese Quellen nach dem zutreffendsten Treiber durchsuchen
Verwenden Sie die Kontrollkästchen, um die Standardsuche zu erweitern oder einzuschränken. Lokale Pfade und Wechselmedien sind in der Standardsuche mit einbegriffen. Der zutreffendste Treiber wird installiert.
Wechselmedien durchsuchen (Diskette, CD,...)
Folgende Quelle ebenfalls durchsuchen:
Durchsuchen
Nicht suchen, sondern den zu installierenden Treiber selbst wählen
Verwenden Sie diese Option, um einen Gerätetreiber aus einer Liste zu wählen. Es wird nicht garantiert, dass der von Ihnen gewählte Treiber der Hardware am besten entspricht.
< Zurück
Weiter >
Abbrechen


Assistent für das Suchen neuer Hardware
Wählen Sie den für diese Hardware zu installierenden Gerätetreiber.
Wählen Sie den Hersteller und das Modell der Hardwarekomponente, und klicken Sie auf "Weiter". Klicken Sie auf "Datenträger", wenn Sie über einen Datenträger verfügen, der den erforderlichen Treiber enthält.
Kompatible Hardware anzeigen
Modell
Cypress Generic USB Device
Dieser Treiber ist nicht digital signiert!
Warum ist Treibersignierung wichtig?
Datenträger...
< Zurück
Weiter >
Abbrechen


Datei suchen
Suchen in:
driver
DEWEUSB.inf
CyUSB.inf
Scripts
Inc
Dateiname:
CyUSB.inf
Öffnen
Dateityp:
Setup-Informationen (*.inf)
Abbrechen

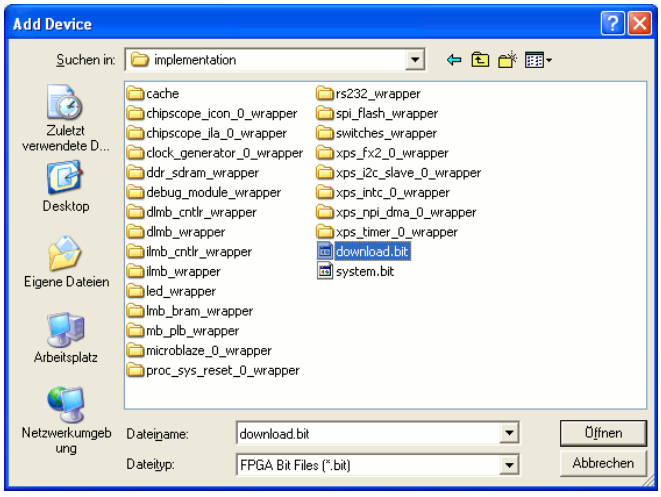

Installation von Datenträger
Legen Sie den Installationsdatenträger des Herstellers ein und stellen Sie sicher, dass weiter unten das richtige Laufwerk ausgewählt ist.
OK
Abbrechen
Dateien des Herstellers kopieren von:
E:\TE0320\1st_program\driver
Durchsuchen...


Assistent für das Suchen neuer Hardware
Wählen Sie den für diese Hardware zu installierenden Gerätetreiber.
Wählen Sie den Hersteller und das Modell der Hardwarekomponente, und klicken Sie auf "Weiter". Klicken Sie auf "Datenträger", wenn Sie über einen Datenträger verfügen, der den erforderlichen Treiber enthält.
Kompatible Hardware anzeigen
Modell
Cypress Generic USB Device
Dieser Treiber ist nicht digital signiert!
Warum ist Treibersignierung wichtig?
Datenträger...
< Zurück
Weiter >
Abbrechen

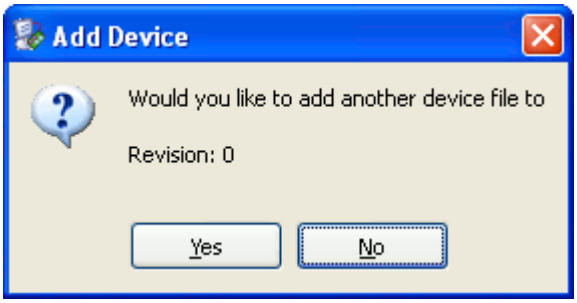


Any other name than ***fpga*** for the `output file name` input field is not allowed.

Just acknowledge the pup-up message.

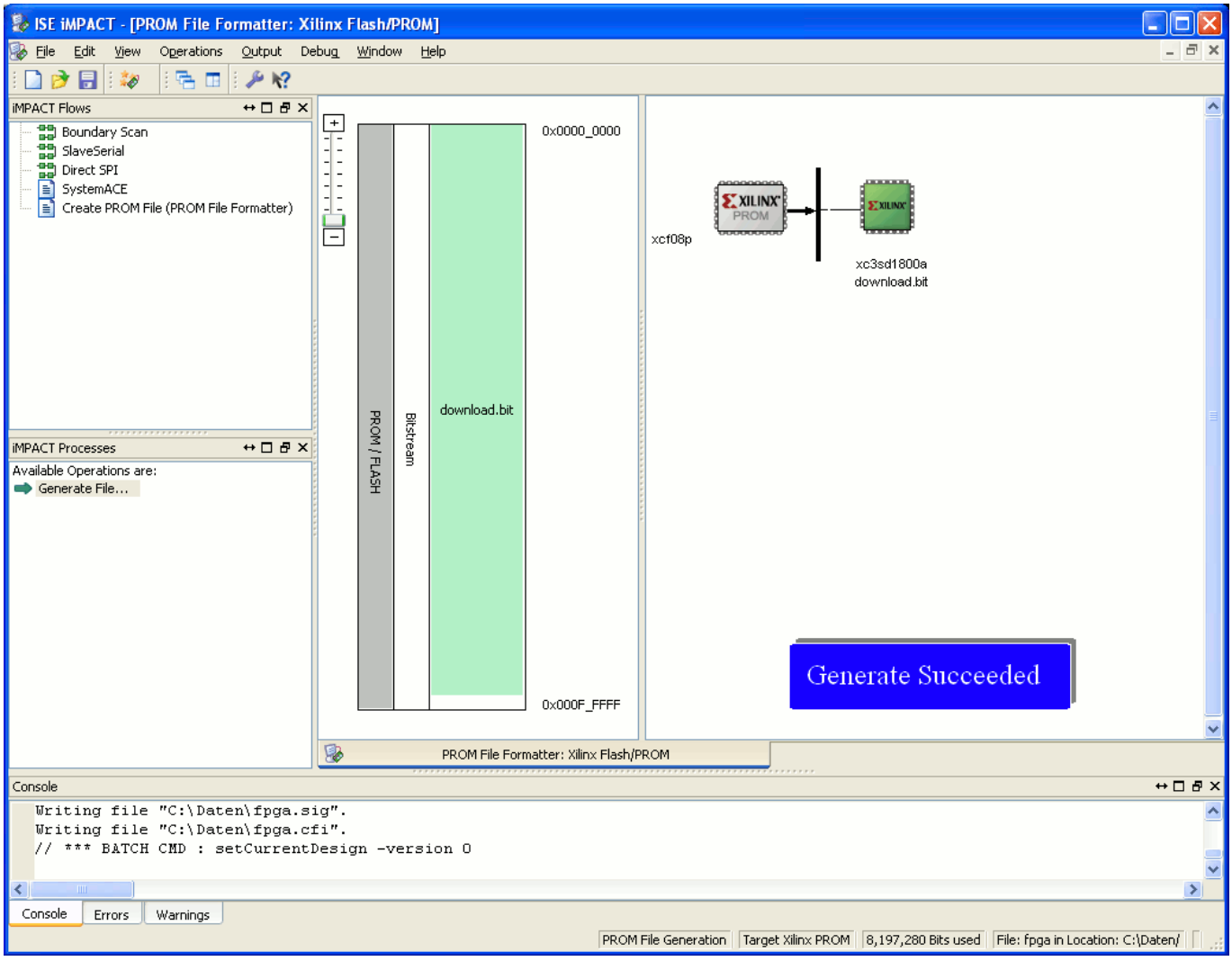


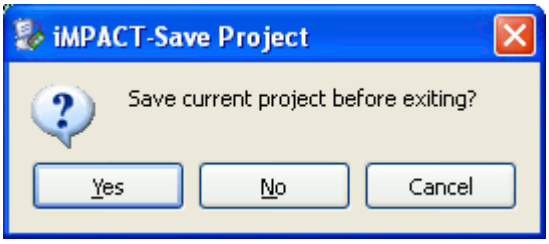
Browse to the `./implementation/` folder of your "`.`" project folder and select the bit-stream file `download.bit`.
Press the ***open*** button in the bottom left corner of the current window.



Your design likely consist of just one device file. So deny the request by pressing the ***NO*** button.

You should see the following message in the main panel: `generate succeeded.`





You might now want to save your Xilinx iMPACT project settings for future use.

In the folder corresponding to the path you chose as the `output file location`, you should find the `fpga.bin` PROM file.

10.2.4.3 FWU file from the PROM file

Once you have got your `fpga.bin` PROM file, you can proceed and generate your FWU (= FirmWare Upgrade) file. The FWU file is a ZIP archive containing 3 files:

- `Bootload.ini` – TE0320 booting settings (see paragraph 10.2.4.3.1 Bootload.ini file)
- `fpga.bin` – FPGA configuration PROM file

10.3 Configuration Using Indirect SPI Configuration Mode

Similar to the traditional configuration memories, SPI serial Flash memories must be loaded with the configuration data. SPI serial Flash memories have a single interface for programming, but there are multiple methods to deliver the data to this interface. This section discusses the hardware setup, the PROM file generation flow and the software flow for ISP (indirect in-system programming) of a Trenz Electronic TE0320 SPI serial Flash configuration PROM through the JTAG interface of a Xilinx Spartan-3A DSP FPGA using Xilinx iMPACT 11.5.

To write the SPI Flash memory, perform the following steps:

(a) disable the master reset S1D (do not care about all other switches at write time);

(b) connect the Xilinx platform cable to JTAG connector J2 as described in paragraph 6.3.1 JTAG connector J2;

(c) generate or locate the FPGA bit-stream file you want to store on the memory;

(d) prepare an SPI PROM file using the ISE iMPACT graphical software from the FPGA bit-stream file;

(e) use the ISE iMPACT graphical software to in-system program the SPI PROM.

In order to have the module to configure from its SPI Flash memory next time it is (re)booted, ensure one of following DIP switch settings:

switch	S1A (EEPROM serial data)	S1B (M2)	S1C (M1)	S1D (/MR master reset)	S2 (PS_EN)
state	0 = ON	0 = ON	0 = ON	1 = OFF	X = do note care
state	1 = OFF	0 = ON	0 = ON	1 = OFF	FX2 PON

Table 31: S1 settings for booting from SPI Flash memory.

For your convenience, a reference video is available on the TrenzElectronic's Channel at YouTube.

For further reference, please read Xilinx XAPP974: Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs.

11 Recommended Design Tools Settings

11.1 DONE LED

When the configuration process successfully completes, the FPGA either actively drives the DONE pin High (*DriveDone*) or allows the DONE pin to float High using either an internal or external pull-up resistor, controlled by the *DonePin* bitstream generator option. To have DONE LED D1 lit after successful FPGA configuration, DriveDone and DonePin bitstream generator options for the DONE pin have to be set to have DONE actively driving its line (see Figure 52 and Table 32).

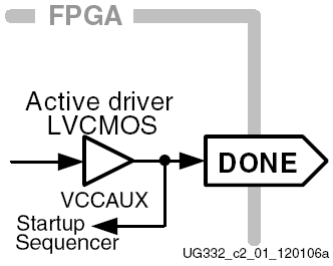


Figure 52: DriveDone and DonePin set to have DONE actively driving its line.

DriveDone defines whether the DONE pin is an active driver or an open-drain output.

DonePin defines whether or not the DONE pin has an internal pull-up resistor.

bitstream generator (BitGen) option	Setting
DriveDone	Yes
DonePin	Pullnone

Table 32: DriveDone and DonePin settings for having DONE actively driving its line.

See Xilinx UG332: Spartan-3 Generation Configuration User Guide (paragraph "DONE Pin") for additional information on these signals.

This options are set graphically in Xilinx ISE Software Project Navigator by selecting the following:

- Generate Programming File > Process Properties > Startup Options > Drive Done Pin High > check the box
- Generate Programming File > Process Properties > Configuration Options > Configuration Pin Done > float

Xilinx ISE Project Navigator option	setting
Drive Done Pin High	√ (checked)
Configuration Pin Done	Float

Table 33: Xilinx ISE Project Navigator settings for having DONE actively driving its line.

Consult *ISE Help* about the Process Properties of the Generate Programming File process in the Processes pane for additional information on these properties.

12.2 Reference Design Summary for Xilinx Spartan-3A DSP 3400

```
--------------------------------------------------------------------------

platgen -p xc3sd3400afg676-4 -lang vhdl -lp x:/xxx/projects_EDK/  system.mhs
Release 11.5 - platgen Xilinx EDK 11.5 Build EDK_LS5.70 (nt)
Copyright (c) 1995-2009 Xilinx, Inc.  All rights reserved.

--------------------------------------------------------------------------

Command Line: platgen -p xc3sd3400afg676-4 -lang vhdl -lp

Running post-placement packing...

Design Summary:
Number of errors:      0
Number of warnings: 1272
Logic Utilization:
  Number of Slice Flip Flops:         6,442 out of  47,744   13%
  Number of 4 input LUTs:             8,290 out of  47,744   17%
Logic Distribution:
  Number of occupied Slices:          7,889 out of  23,872   33%
    Number of Slices containing only related logic:   7,889 out of   7,889 100%
    Number of Slices containing unrelated logic:          0 out of   7,889   0%
      *See NOTES below for an explanation of the effects of unrelated logic.
  Total Number of 4 input LUTs:       8,662 out of  47,744   18%
    Number used as logic:             6,212
    Number used as a route-thru:        372
    Number used for Dual Port RAMs:   1,892
      (Two LUTs used per Dual Port RAM)
    Number used as Shift registers:     186

  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

  Number of bonded IOBs:                119 out of     469   25%
    IOB Flip Flops:                      39
    IOB Master Pads:                      2
    IOB Slave Pads:                       2
  Number of ODDR2s used:                 44
    Number of DDR_ALIGNMENT = NONE       44
    Number of DDR_ALIGNMENT = C0          0
    Number of DDR_ALIGNMENT = C1          0
  Number of BUFGMUXs:                     5 out of      24   20%
  Number of DCMs:                         1 out of       8   12%
  Number of BSCANs:                       1 out of       1  100%
  Number of DSP48As:                      3 out of     126    2%
  Number of RAMB16BWERs:                 30 out of     126   23%
  Number of BSCAN_SPARTAN3As:             1 out of       1  100%

  Number of RPM macros:           1
Average Fanout of Non-Clock Nets:               3.56

--------------------------------------------------------------------------
```

```
Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)


Device speed data version:  "PRODUCTION 1.33 2010-02-13".



Design Summary Report:

 Number of External IOBs                          119 out of 469    25%

   Number of External Input IOBs                  30

      Number of External Input IBUFs              30
        Number of LOCed External Input IBUFs      30 out of 30    100%


   Number of External Output IOBs                 43

      Number of External Output DIFFMs             2
        Number of LOCed External Output DIFFMs     2 out of 2     100%

      Number of External Output DIFFSs             2
        Number of LOCed External Output DIFFSs     2 out of 2     100%

      Number of External Output IOBs              39
        Number of LOCed External Output IOBs      39 out of 39    100%


   Number of External Bidir IOBs                  46

      Number of External Bidir IOBs               46
        Number of LOCed External Bidir IOBs       46 out of 46    100%


   Number of BSCANs                             1 out of 1     100%
   Number of BUFGMUXs                           5 out of 24     20%
   Number of DCMs                               1 out of 8      12%
   Number of DSP48As                            3 out of 126     2%
   Number of RAMB16BWERs                       30 out of 126    23%
   Number of Slices                          7889 out of 23872  33%
      Number of SLICEMs                      1156 out of 11936   9%

   Number of LOCed Slices                     125 out of 7889    1%
      Number of LOCed SLICEMs                  83 out of 1156    7%



Overall effort level (-ol):   High
Router effort level (-rl):    High

--------------------------------------------------------------------------------
```

14.1 Top View

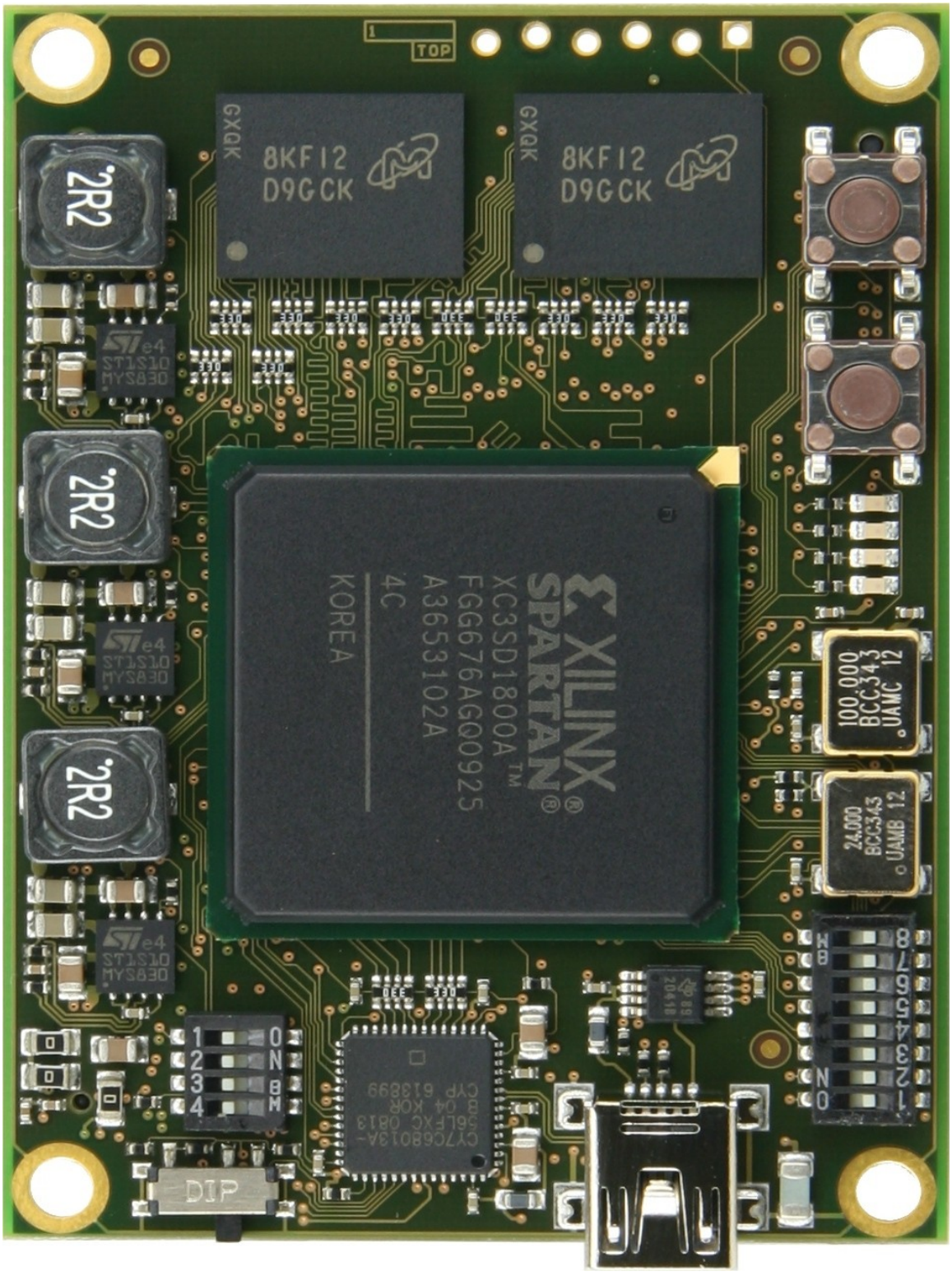


Figure 53: TE0320 high resolution top view.

17 Related Materials and References

The following documents provide supplementary information useful with this user manual.

17.1 Data Sheets

- Xilinx DS485: Digital Clock Manager (DCM) Module Data Sheet
  This is the data sheet for the Digital Clock Manager (DCM) Module core.
  www.xilinx.com/support/documentation/ip_documentation/dcm_module.pdf
- Xilinx DS610: Spartan-3A DSP FPGA Family: Complete Data Sheet
  The Spartan®-3A DSP family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high-volume, cost-sensitive, high-performance DSP applications.
  www.xilinx.com/support/documentation/data_sheets/ds610.pdf

17.2 User Guides

- Xilinx UG331: Spartan-3 Generation FPGA User Guide
  Functional description of the Spartan®-3 generation FPGA architecture and how to use it. Includes the Spartan-3A, Spartan-3AN, Spartan-3A DSP, Spartan-3E, and Spartan-3 platforms.
  www.xilinx.com/support/documentation/user_guides/ug331.pdf
- Xilinx UG332: Spartan-3 Generation Configuration User Guide
  Describes the configuration features of the Spartan®-3 Generation FPGAs. Includes the Spartan-3A, Spartan-3AN, Spartan-3A DSP, Spartan-3E, and Spartan-3 FPGA families.
  www.xilinx.com/support/documentation/user_guides/ug332.pdf
- EZ-USB® Technical Reference Manual (TRM)
  www.cypress.com/?rID=14667

17.3 Tutorials

- (Xilinx) ISE (10.1) In-Depth Tutorial
  Chapter 7: iMPACT Tutorial
  www.xilinx.com/direct/ise10_tutorials/ise10tut.pdf
- Xilinx UG695: ISE In-Depth Tutorial
  Chapter 7: iMPACT Tutorial
  http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/ise11tut.pdf

17.4 Application Notes

- Xilinx XAPP104: A Quick JTAG ISP Checklist
  Most Xilinx CPLDs, PROMs, and FPGAs have an IEEE Standard 1149.1 (JTAG) port. Xilinx devices with a JTAG port are in-system programmable (ISP) through the JTAG port. The ISP feature is beneficial for fast prototype development. This application note describes a short list of considerations needed to get the best performance from your ISP designs.
  www.xilinx.com/support/documentation/application_notes/xapp104.pdf
- Xilinx XAPP974: Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs

18.4 Signal Integrity Considerations

Traces of differential signals pairs are NOT routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length. For applications where traces length has to be matched or timing differences have to be compensated, Table 42 and Table 43 list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 60 ohm.

Pairs of pins that form a differential I/O pair appear colored together in the table. An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.