Trenz Electronic GmbH - TE0320-00-EV02IB Datasheet

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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Not For New Designs
Module/Board Type	FPGA, USB Core
Core Processor	Spartan-3A DSP
Co-Processor	Cypress EZ-USB FX2LP
Speed	100MHz
Flash Size	4MB
RAM Size	128MB
Connector Type	B2B
Size / Dimension	2.7" x 1.9" (68mm x 48mm)
Operating Temperature	-40°C ~ 85°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0320-00-ev02ib

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1 Block Diagram

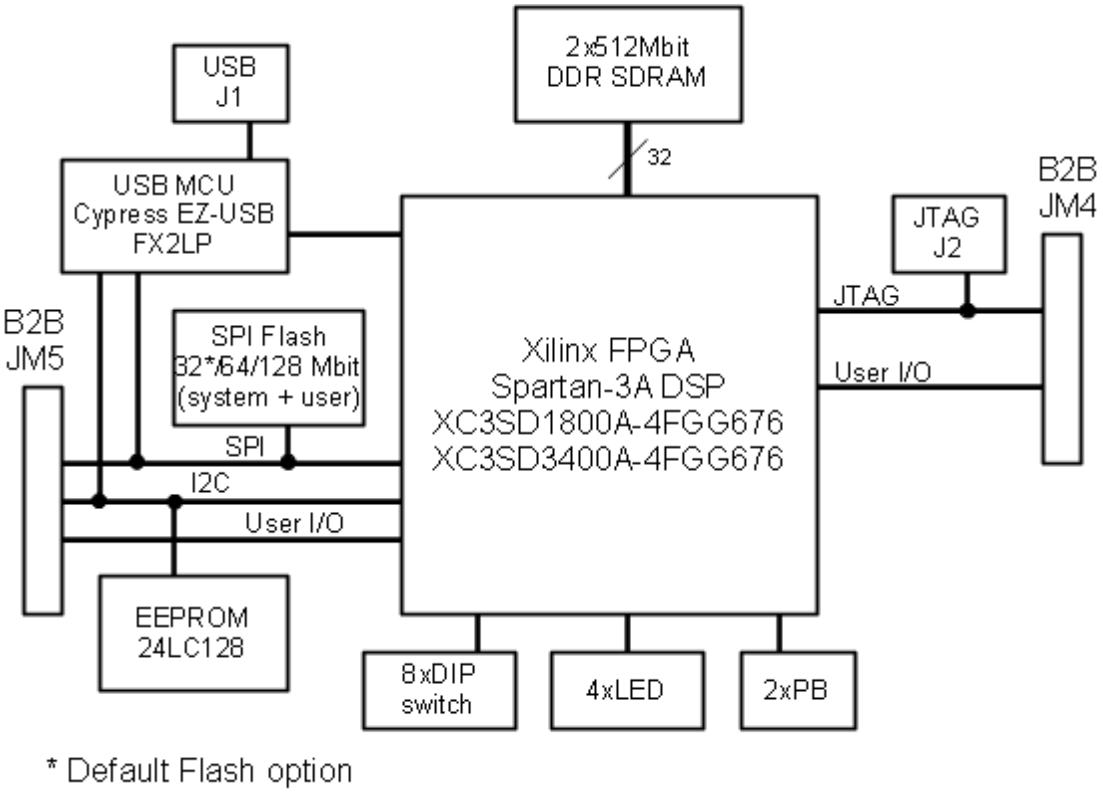


Figure 3: TE0320 block diagram

2 Module options

FPGA options

Module can be ordered with Spartan-3A DSP XC3SD1800A or XC3SD3400A chip.

Flash options

Module can be ordered with 32, 64 or 128 Mbit SPI Flash chip.

Temperature grade options

Module can be ordered in commercial or in extended (from -25 C° to +85 C°) temperature grade.

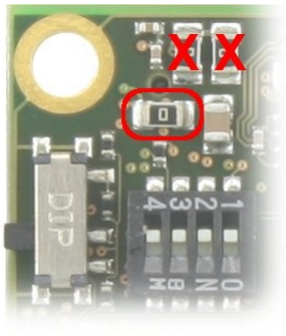


Figure 7: assembly combination for power supply through J1.

Any other assembly combination of R9, R11 and R12 is not allowed.

5.3 On-Board Power Rails

According to the Xilinx Spartan-3A DSP literature, there are the following power supply pin types:

- V_{CCAUX}: dedicated auxiliary power supply pins
- V_{CCINT}: dedicated internal core logic power supply pins
- V_{CCO}: supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards.

TE0320 has the following power rails on-board:

- Vsup

  It is the main internal power rail irrespective of the external power supply. It is supplied by either Vb2b or Vusb. It manages power distribution, conversion and supervision. It is routed also to connector JM5 as a user power supply output.
- Vb2b

  It is the main power rail when the module is supplied from B2B connector JM5.
- Vusb

  It is the main power rail when the module is supplied from USB mini-B connector J1. The maximum current than can be provided to J1 is determined by the USB power source.
- 3.3V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the module and connectors JM4 and JM5.
- 2.5V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the DDR SDRAM and connectors JM5.
- 1.2V

  It is converted from Vsup by a step-down DC/DC converter and can provide up to 3.0 A to the V_{CCINT} power supply pins and connectors JM5.
- VCCAUX

in Table 2.

	gender	W+P	Trenz Electronic
B2B connector JM4 + JM5	female	6060-080-46-00-10-10-PPTR	23758
B2B mating connector	male	6110-080-00-10-PPTR	23749

Table 2: Ordering codes of recommended B2B connectors.

The mating height of connectors 6060-080-46-00-10-10-PPTR and 6110-080-00-10-PPTR is 6mm.

Connectors JM4 and JM5 can mate also with any 1.27 mm (50 mil = .050") pitch male header connectors with up to 2 × 40 pins. Figure 17.

Figure 17: sample matching header connector.

Connectors JM4 and JM5 and are placed on the bottom side of the module as shown in Figure 18.

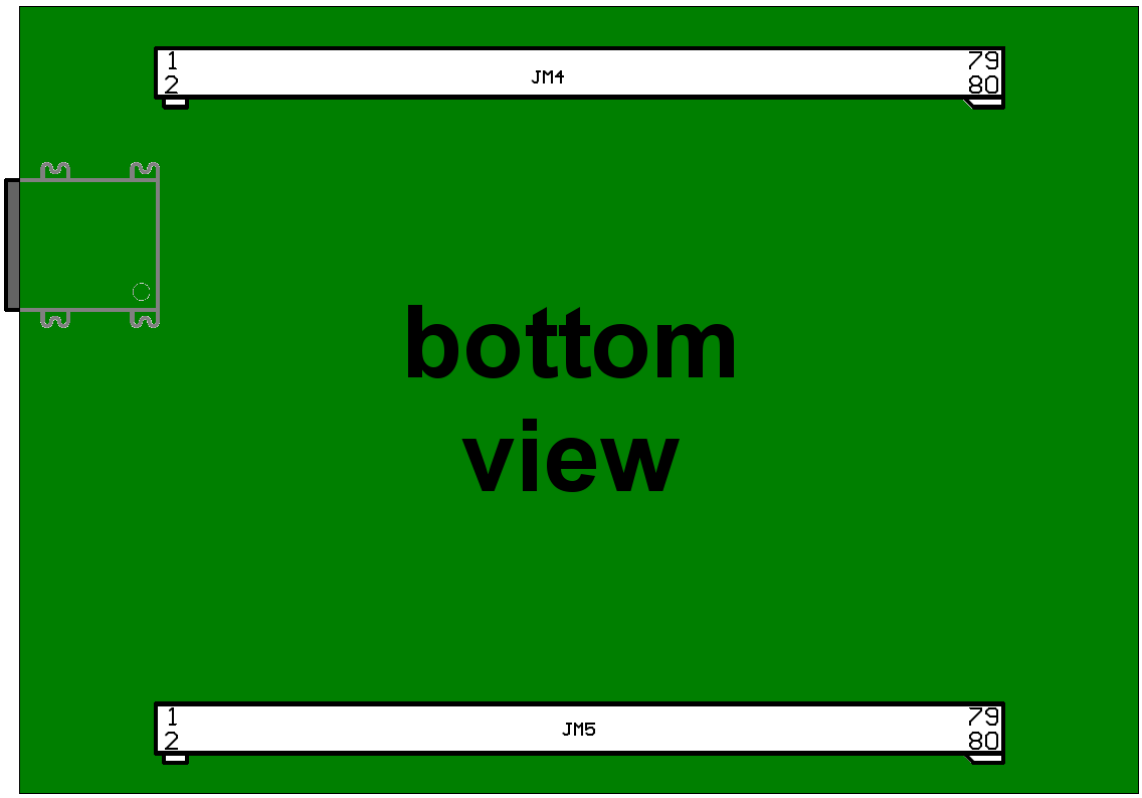


Figure 18: female header connectors JM4 and JM5 (bottom view).

detailed in Table 3. Ensure resistors R3 and R4 are populated to connect USB B2B pins B2B_D_P and B2B_D_P to USB lines D_P and D_P respectively.

pin number	pin name	signal name	description
4	B2B_D_P	D_P	USB data + (D+)
6	B2B_D_N	D_N	USB data - (D-)

Table 3: USB pins at B2B connector JM4.

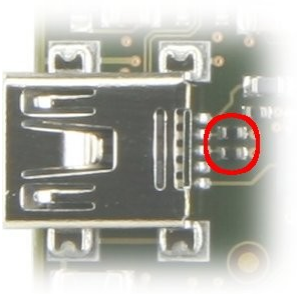


Figure 23: Resistors R3 and R4 required for USB communication over B2B connector JM4.

6.3 JTAG Interface

6.3.1 JTAG connector J2

JTAG signals are available on the gender-inverted standard 6-pin JTAG header connector J2 as shown in Figure 24.

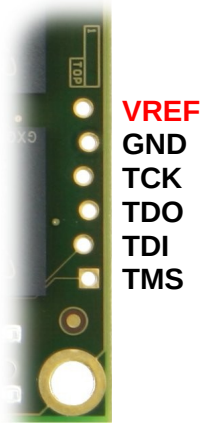


Figure 24: JTAG connector J2.

To connect your computer to JTAG connector J2 you typically need

- a JTAG cable with standard 6-pin JTAG female header;
- a 2.54 mm pitch 1 × 6 pin gender changer header.

Some examples of JTAG cable set are listed in Table 4.

JTAG cable	flying leads	software	gender changer
Xilinx Platform Cable USB	included	Xilinx iMPACT	1 × 6 pin
Digilent XUP USB-JTAG Programming Cable	XUP Fly Wire Assembly	Xilinx iMPACT	1 × 6 pin

7 Timing

7.1 Main Clock Oscillator

The module has a main SMD clock oscillator providing a clock source for the FPGA as detailed in Table 3.

signal	FPGA pin	FPGA ball	FPGA bank
MAINCLK	IO_L27N_2 GCLK1	AA14	2

Table 16: Main clock signal details.

Standard frequency is 100 MHz. Should you wish or need another main clock oscillator frequency, please contact Trenz Electronic. The lower the main clock frequency, the lower the module power consumption. Moreover, as the main clock is preferably used as DDR SDRAM clock, a lower clock frequency makes easier for the development tools to meet the timing requirements (particularly for DDR SDRAM).

7.2 24 MHz Clock Oscillator

The module has a 24 MHz SMD clock oscillator providing a clock source for both the EZ-USB FX2LP USB microcontroller (XTALIN) and the FPGA as detailed in Table 17.

signal	FPGA pin	FPGA ball	FPGA bank
24MHZ1	IO_L28N_2 GCLK3	AE14	2

Table 17: 24 MHz clock signal details.

7.3 Interface Clock (IFCLK)

The IFCLK line synchronizes the communication between the EZ-USB FX2LP USB microcontroller and the FPGA as detailed in Table 18.

signal	FPGA pin	FPGA ball	FPGA bank
IFCLK	IO_L31N_1 TRDY1 RHCLK3	P25	1

Table 18: Interface clock signal details.

7.4 Digital Clock Manager (DCM)

The DCMs of the FPGA can be used to synthesize arbitrary clock frequencies from any on-board clock network, differential clock input pair or single-ended clock input. For further reference, please read Xilinx DS485:Digital Clock Manager (DCM) Module and the DCM chapter in Xilinx UG331: Spartan-3 Generation FPGA User Guide.

7.5 Watchdog

TE0320 has a watchdog timer that is periodically triggered by a positive or negative transition of the watchdog input (WDI) signal. When the supervising system fails to retrigger the watchdog circuit within the time-out interval (min 1.1

s, typ 1.6 s, max 2.3 s), the watchdog output becomes active and asserts the master reset (/MR) signal. This event also reinitializes the watchdog timer.

If resistors R135 and R165 are not populated, the watchdog is disabled.

If resistors R135 and R165 are populated, the watchdog can be enabled. In this case there are still two options.

- To enable the watchdog after module power-up, drive the WDI signal to generate a transition (no matter if positive or negative).
- To keep the watchdog disabled, set the WDI FPGA signal output to high-impedance. One way to reach this goal is to leave FPGA pin V24 (FPGA signal IO_L19P_1) undeclared in the user constraints file (UCF) and set the Xilinx Project Navigator options as follows:
project properties > configuration options > unused IOB pins > float.

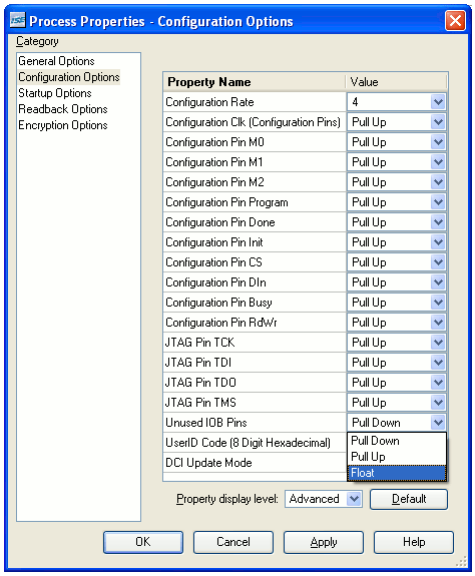


Figure 40: configuration option in Xilinx ISE Project Navigator.

9 System Requirements

9.1 Power Supply Requirements

TE0320 can be power supplied by one of the following power sources:

- USB bus, 5 V;
- JM5[1:4], 4 V to 7 V power supply (5 V recommended).

System current consumption is design dependent.

USB buses able to supply only 100 mA are not supported.

See paragraph 5.2 Power Supply Sources for additional information on this topic.

9.2 Hardware Design Requirements

PUDC_B (pull-up during configuration, active Low) pin in TE0320 modules is hard-wired high, determining user-I/O pins to float before and during configuration. Turning off pull-up resistors in hot-swap or hot-insertion applications, disables potential current paths to the I/O power rail. However, external pull-up or pull-down resistors may be required on each individual I/O pin depending on the specific application.

9.3 USB Requirements

Recommended USB bus classes are 1.1 and 2.0.

TE0320 can be connected to a USB bus through connector either J1 or JM4[4, 6].

SPI serial Flash memory can be written through the Firmware Upgrade Tool and the API.

Data communication over USB can be implemented through the API.

9.4 JTAG Requirements

TE0320 can be configured and debugged over JTAG through connector either J2 or JM4[74, 76, 78, 80].

See paragraph 6.3 JTAG Interface for additional information on this topic.

9.4.1 Software Requirements

Software requirements depend on the intended design goal.

design goal	ISE WebPACK	EDK
HDL design	•	
MicroBlaze design	•	•
reference design	•	•

Table 19: software requirements chart.

EDK: Xilinx Embedded Development Kit = XPS + SDK;

XPS = Xilinx Platform Studio (for hardware engineers);

SDK: Xilinx Software Development Kit (for software engineers).

Xilinx ISE WebPACK is a **free** development environment featuring

- Xilinx ISE Foundation (device limited)
- Xilinx ISE Simulator (ISim)
- Xilinx PlanAhead

TE0320 reference design requires Xilinx EDK.

Please visit the official Xilinx ISE Design Suite page for latest information about Xilinx design tools.

9.5 Operating System Support

Xilinx ISE Design Suite is supported on both 32-bit and 64 bit versions of both Microsoft Windows and GNU/Linux operating systems. Please consult the Xilinx ISE Design Suite Product Table and Xilinx ISE Design Suite Software Matrix on the official Xilinx ISE Design Suite page for latest information about Xilinx ISE Design Suite operating system support.

TE0320 software package includes EZ-USB FX2LP USB microcontroller device drivers for the 32 bit version of Microsoft Windows operating system.

TE0320 software package includes the Firmware Upgrade Tool for the 32 bit version of Microsoft Windows operating system.

Cypress generic USB device

- S1B and S1C = do not care

  configuration mode is irrelevant for this step
- S1D = OFF

  master reset disabled

switch	S1 label	signal name	status
S1A	1	EEPROM serial data	OFF
S1B	2	M2	X
S1C	3	M1	X
S1D	4	/MR (master reset)	OFF

Table 26: S1 settings for forcing the EZ-USB FX2LP USB microcontroller to enumerate as a generic USB device driver.

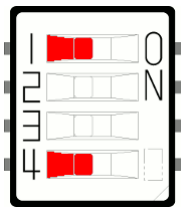


Figure 47: S1 settings for forcing the EZ-USB FX2LP USB microcontroller to enumerate as a generic USB device driver.

Connect the TE0320 to a USB port on your computer using a USB cable.

The USB microcontroller should now enumerate as a Cypress generic USB device.

Toggle S1A to ON; this will

- Connect the serial data line between the USB microcontroller and the large EEPROM;
- Allow the EZ-USB FX2LP USB microcontroller to program the large EEPROM;
- Prevent the EZ-USB FX2LP USB microcontroller to enumerate again for any content of the large EEPROM.

switch	S1 label	signal name	status
S1A	1	EEPROM serial data	ON
S1B	2	M2	X
S1C	3	M1	X
S1D	4	/MR (master reset)	OFF

Table 27: S1 settings for programming EZ-USB FX2LP USB microcontroller large EEPROM.

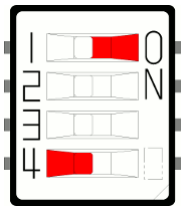


Figure 48: S1 settings for programming EZ-USB FX2LP USB microcontroller large EEPROM.

switch	S1 label	signal name	status
S1A	1	EEPROM serial data	ON
S1B	2	M2	X
S1C	3	M1	X
S1D	4	/MR (master reset)	OFF

Table 28: S1 settings for installing specific USB device driver.

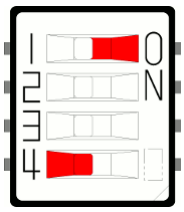
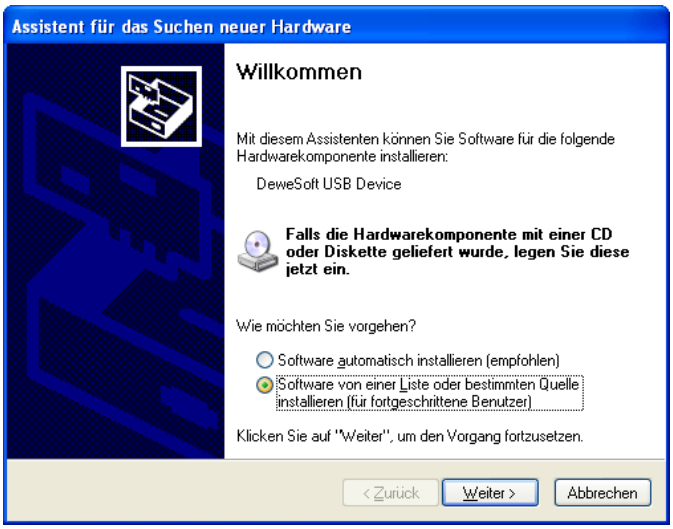
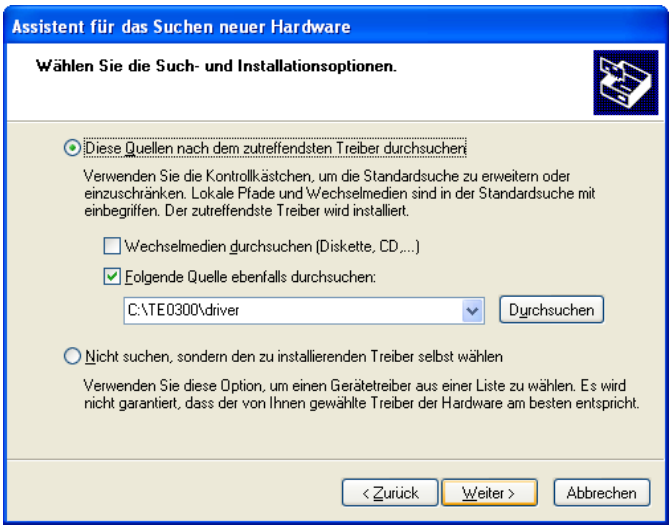


Figure 49: S1 settings for installing pecific USB device driver.

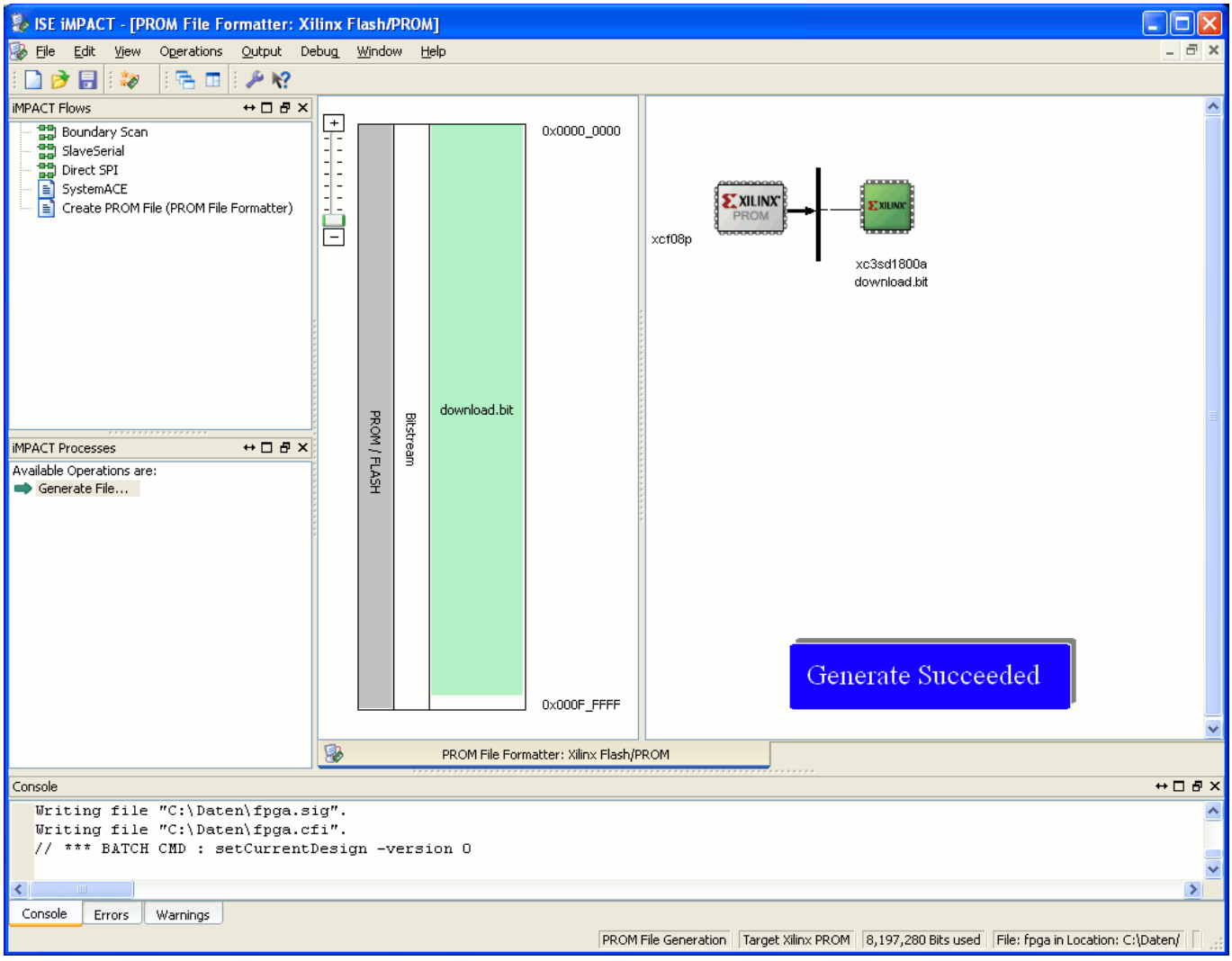
Connect the TE0320 to a USB port on your computer using a USB cable.

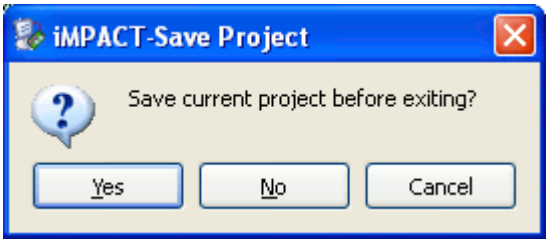
Follow the “Found New Hardware” wizard to install the driver, if necessary, as shown in the following example. You need to look for the *step3_user/DEWESOFT.inf* device driver information file in the TE0320 software package.





You should see the following message in the main panel: `generate succeeded.`





You might now want to save your Xilinx iMPACT project settings for future use.

In the folder corresponding to the path you chose as the `output file location`, you should find the `fpga.bin` PROM file.

10.2.4.3 FWU file from the PROM file

Once you have got your `fpga.bin` PROM file, you can proceed and generate your FWU (= FirmWare Upgrade) file. The FWU file is a ZIP archive containing 3 files:

- `Bootload.ini` – TE0320 booting settings (see paragraph 10.2.4.3.1 Bootload.ini file)
- `fpga.bin` – FPGA configuration PROM file

- `usb.bin` – EZ-USB FX2LP USB microcontroller firmware

To create your FWU file, you shall

- replace the existing `step4_user\fpga.bin` with the latest `fpga.bin` (once per design)
- zip the 3 files
- rename the `zip` file extension to `fwu`
- upload the file as explained in paragraph 10.2.5 Firmware Upgrade Tool utilization.

Warning! file and path names are given and must not be changed!

10.2.4.3.1 Bootload.ini file

The `step4_user\Bootload.ini` file defines some module start-up options. Version 1.0 of Bootload.ini has the following structure:

- `[Info]` – information section (do not edit this section)
  - `Version` – Bootload.ini file format version
  - `DeviceType` – 3 stands for current device type
- [Settings]: settings section
  - `FPGABitSwap` – see Xilinx UG332: Spartan-3 Generation Configuration User Guide, chapter SelectMAP Data Ordering (default = 1 = do bit swapping)
  - `FPGAPowerON` – value of FX2_PS_EN after SPI Flash memory programming (see paragraph 6.8.2 Slide Switch S2) (default = 1 = power on after upgrade)

10.2.4.3.2 usb.bin file

The `step4_user\usb.bin` file contains the firmware to be written in the large EEPROM of the EZ-USB FX2LP USB microcontroller and loaded at module start-up to implement the DEWESoft instruction set.

10.2.5 Firmware Upgrade Tool utilization

10.2.5.1 Switch Settings

For the Firmware Upgrade Tool to operate correctly, switch S1 and S2 shall be set properly.

10.2.5.2 DIP Switch S1

Ensure that DIP switch S1 is set to

- USB microcontroller large EEPROM enabled (S1A set to ON)
- configuration mode set to Master SPI (S1B and S1C set to ON)

10.3 Configuration Using Indirect SPI Configuration Mode

Similar to the traditional configuration memories, SPI serial Flash memories must be loaded with the configuration data. SPI serial Flash memories have a single interface for programming, but there are multiple methods to deliver the data to this interface. This section discusses the hardware setup, the PROM file generation flow and the software flow for ISP (indirect in-system programming) of a Trenz Electronic TE0320 SPI serial Flash configuration PROM through the JTAG interface of a Xilinx Spartan-3A DSP FPGA using Xilinx iMPACT 11.5.

To write the SPI Flash memory, perform the following steps:

(a) disable the master reset S1D (do not care about all other switches at write time);

(b) connect the Xilinx platform cable to JTAG connector J2 as described in paragraph 6.3.1 JTAG connector J2;

(c) generate or locate the FPGA bit-stream file you want to store on the memory;

(d) prepare an SPI PROM file using the ISE iMPACT graphical software from the FPGA bit-stream file;

(e) use the ISE iMPACT graphical software to in-system program the SPI PROM.

In order to have the module to configure from its SPI Flash memory next time it is (re)booted, ensure one of following DIP switch settings:

switch	S1A (EEPROM serial data)	S1B (M2)	S1C (M1)	S1D (/MR master reset)	S2 (PS_EN)
state	0 = ON	0 = ON	0 = ON	1 = OFF	X = do note care
state	1 = OFF	0 = ON	0 = ON	1 = OFF	FX2 PON

Table 31: S1 settings for booting from SPI Flash memory.

For your convenience, a reference video is available on the TrenzElectronic's Channel at YouTube.

For further reference, please read Xilinx XAPP974: Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs.

```
Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)


Device speed data version:  "PRODUCTION 1.33 2010-02-13".



Design Summary Report:

 Number of External IOBs                          119 out of 469    25%

   Number of External Input IOBs                  30

      Number of External Input IBUFs              30
        Number of LOCed External Input IBUFs      30 out of 30    100%


   Number of External Output IOBs                 43

      Number of External Output DIFFMs             2
        Number of LOCed External Output DIFFMs     2 out of 2     100%

      Number of External Output DIFFSs             2
        Number of LOCed External Output DIFFSs     2 out of 2     100%

      Number of External Output IOBs              39
        Number of LOCed External Output IOBs      39 out of 39    100%


   Number of External Bidir IOBs                  46

      Number of External Bidir IOBs               46
        Number of LOCed External Bidir IOBs       46 out of 46    100%


   Number of BSCANs                             1 out of 1     100%
   Number of BUFGMUXs                           5 out of 24     20%
   Number of DCMs                               1 out of 8      12%
   Number of DSP48As                            3 out of 126     2%
   Number of RAMB16BWERs                       30 out of 126    23%
   Number of Slices                          7889 out of 23872  33%
      Number of SLICEMs                      1156 out of 11936   9%

   Number of LOCed Slices                     125 out of 7889    1%
      Number of LOCed SLICEMs                  83 out of 1156    7%



Overall effort level (-ol):   High
Router effort level (-rl):    High

--------------------------------------------------------------------------------
```

14.2 Bottom View

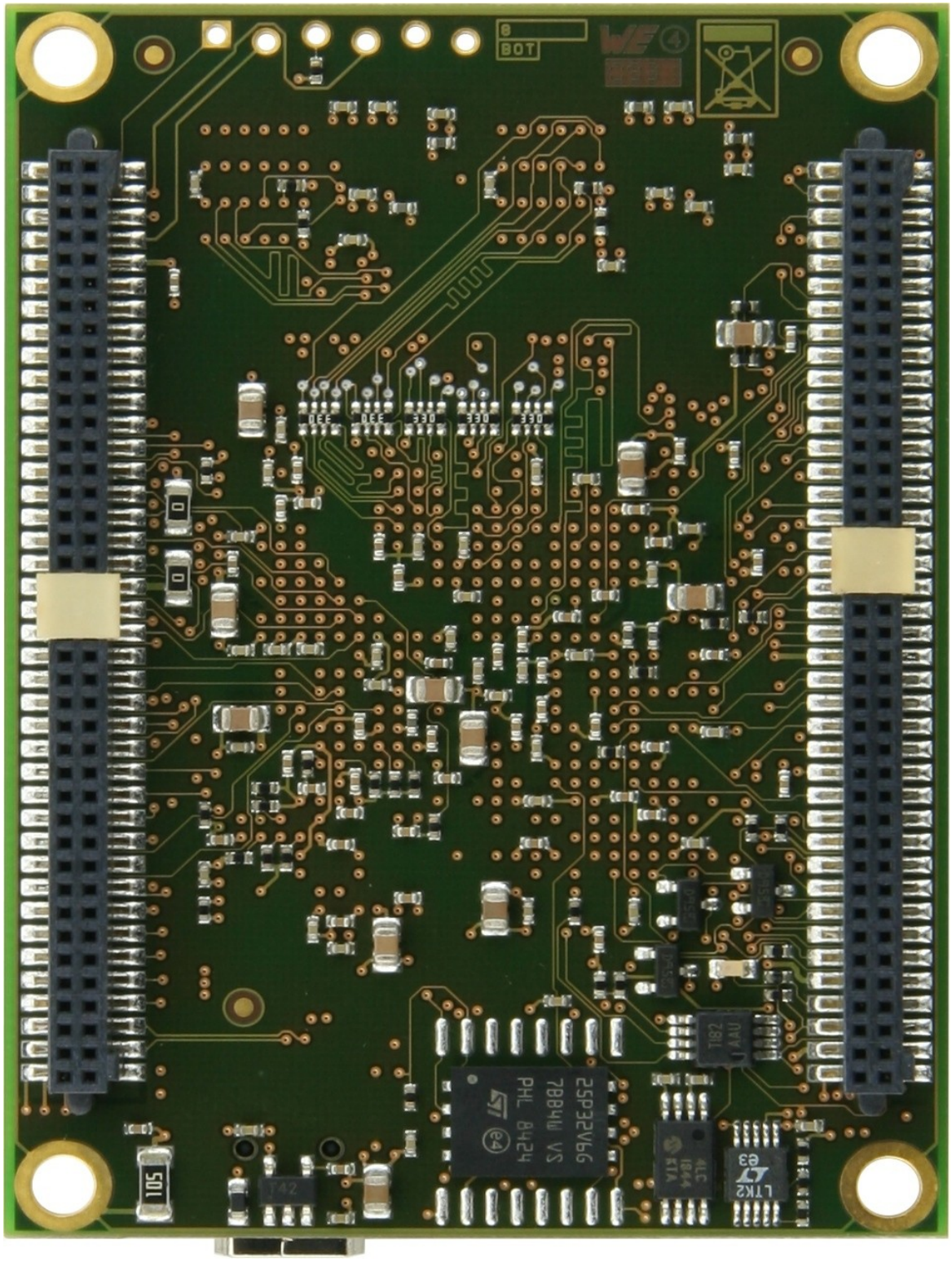


Figure 54: TE0320 high resolution bottom view.

17 Related Materials and References

The following documents provide supplementary information useful with this user manual.

17.1 Data Sheets

- Xilinx DS485: Digital Clock Manager (DCM) Module Data Sheet
  This is the data sheet for the Digital Clock Manager (DCM) Module core.
  www.xilinx.com/support/documentation/ip_documentation/dcm_module.pdf
- Xilinx DS610: Spartan-3A DSP FPGA Family: Complete Data Sheet
  The Spartan®-3A DSP family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high-volume, cost-sensitive, high-performance DSP applications.
  www.xilinx.com/support/documentation/data_sheets/ds610.pdf

17.2 User Guides

- Xilinx UG331: Spartan-3 Generation FPGA User Guide
  Functional description of the Spartan®-3 generation FPGA architecture and how to use it. Includes the Spartan-3A, Spartan-3AN, Spartan-3A DSP, Spartan-3E, and Spartan-3 platforms.
  www.xilinx.com/support/documentation/user_guides/ug331.pdf
- Xilinx UG332: Spartan-3 Generation Configuration User Guide
  Describes the configuration features of the Spartan®-3 Generation FPGAs. Includes the Spartan-3A, Spartan-3AN, Spartan-3A DSP, Spartan-3E, and Spartan-3 FPGA families.
  www.xilinx.com/support/documentation/user_guides/ug332.pdf
- EZ-USB® Technical Reference Manual (TRM)
  www.cypress.com/?rID=14667

17.3 Tutorials

- (Xilinx) ISE (10.1) In-Depth Tutorial
  Chapter 7: iMPACT Tutorial
  www.xilinx.com/direct/ise10_tutorials/ise10tut.pdf
- Xilinx UG695: ISE In-Depth Tutorial
  Chapter 7: iMPACT Tutorial
  http://www.xilinx.com/support/documentation/sw_manuals/xilinx11/ise11tut.pdf

17.4 Application Notes

- Xilinx XAPP104: A Quick JTAG ISP Checklist
  Most Xilinx CPLDs, PROMs, and FPGAs have an IEEE Standard 1149.1 (JTAG) port. Xilinx devices with a JTAG port are in-system programmable (ISP) through the JTAG port. The ISP feature is beneficial for fast prototype development. This application note describes a short list of considerations needed to get the best performance from your ISP designs.
  www.xilinx.com/support/documentation/application_notes/xapp104.pdf
- Xilinx XAPP974: Indirect Programming of SPI Serial Flash PROMs with Spartan-3A FPGAs

18 B2B Connectors Pin Descriptions

This section describes how the various pins on B2B connectors JM4 and JM5 connect with TE0320 on-board components. In this chapter, most of naming conventions and colour coding scheme are taken from the official Xilinx Spartan-3A DSP documentation.

18.1 Pin Labelling

The pin label is abbreviated but descriptive for each pin. All I/O pins begin with IO. If a pin can be used as a differential signal, the name includes an _Lxxy_b suffix, where

- L indicates that the pin is part of a differential pair
- xx is a two-digit integer, unique for each bank, that identifies a differential pin-pair
- y is the signal polarity and is replaced by P for the positive signal or N for the negative. These two pins form one differential pin-pair
- b is an integer, 0 through 2 for TE0320, indicating the associated I/O bank.

Dual- or multi-purpose pins have a name composed of the signal names referring to each possible pin function (e. g. IO_L52P_2 / D0 / DIN / MISO). _B is used as the active-Low designator, as in CSI_B.

A differential clock input requires two global clock inputs. The P and N inputs follow the same configuration as for standard inputs on those pins. The clock inputs that get paired together are consecutive pins in clock number, an even clock number and the next higher odd value. For example, GCLK0 and GCLK1 are a differential pair.

18.2 Pin Types

Most pins of B2B connectors JM4 and JM5 are general-purpose, user-defined I/O pins (GPIOs). There are, however, up to 9 different functional types of pins on the TE0320, as outlined in Table 39. In pin-out tables 40 and 41, the individual pins are colour-coded according to pin type as in Table 39.

type colour code	description
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See Xilinx UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.
VREF	VREF0 provides a reference voltage input for certain I/O standards. See paragraph 6.9 Voltage Reference VREF0 for additional information on this signal.
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Packages have 16 global clock inputs that optionally clock the entire device. See the Using Global Clock Resources chapter in UG331: Spartan-3 Generation FPGA User Guide for additional information on these signals.
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See Xilinx UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.
PWRMGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by VCCAUX. AWAKE is a Dual-Purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.

18.3 B2B Connectors Pin-Out

18.3.1 JM4 Pin-Out

supply	bank	type	FPGA pin	FPGA ball	JM4 singal	JM4	pin	JM4 singal	FPGA ball	FPGA pin	type	bank	supply
3.3 V	-	out	-	-	3.3V	1	2	GND	-	-	GND	GND	GND
VcccIO0	0	I/O	IO_L20P_0	F15	JM4-IO01	3	4	B2B_D_P	-	-	I/O	-	USB
VcccIO0	0	I/O	IO_L21N_0	C16	JM4-IO02	5	6	B2B_D_N	-	-	I/O	-	USB
GND	GND	GND	-	-	GND	7	8	JM4-IO34	K12	IO_L39N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L21P_0	D17	JM4-IO03	9	10	JM4-IO35	J12	IO_L39P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L22N_0	C15	JM4-IO04	11	12	JM4-IO36	D8	IO_L40N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L22P_0	D16	JM4-IO05	13	14	JM4-IO37	C8	IO_L40P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L23N_0	A15	JM4-IO06	15	16	GND	-	-	GND	GND	GND
VcccIO0	0	I/O	IO_L23P_0	B15	JM4-IO07	17	18	JM4-IO38	C6	IO_L41N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L24N_0	F14	JM4-IO08	19	20	JM4-IO39	B6	IO_L41P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L24P_0	E14	JM4-IO09	21	22	JM4-IO40	C7	IO_L42N_0	I/O	0	VcccIO0
GND	GND	GND	-	-	GND	23	24	JM4-IO41	B7	IO_L42P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L25N_0 GCLK5	J14	JM4-IO10	25	26	JM4-IO42	K11	IO_L43N_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L25P_0 GCLK4	K14	JM4-IO11	27	28	JM4-IO43	J11	IO_L43P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L26N_0 GCLK7	A14	JM4-IO12	29	30	VcccIO0	-	-	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L26P_0 GCLK6	B14	JM4-IO13	31	32	JM4-IO44	D6	IO_L44N_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L27N_0 GCLK9	G13	JM4-IO14	33	34	JM4-IO45	C5	IO_L44P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L27P_0 GCLK8	F13	JM4-IO15	35	36	JM4-IO46	B4	IO_L45N_0	I/O	0	VcccIO0
VREF	0	in	-	-	VREF0	37	38	JM4-IO47	A4	IO_L45P_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L28N_0 GCLK11	C13	JM4-IO16	39	40	JM4-IO48	H10	IO_L46N_0	I/O	0	VcccIO0
VcccIO0	0	I/O GCLK	IO_L28P_0 GCLK10	B13	JM4-IO17	41	42	JM4-IO49	G10	IO_L46P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L29N_0	B12	JM4-IO18	43	44	VcccIO0	-	-	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L29P_0	A12	JM4-IO19	45	46	JM4-IO50	H9	IO_L47N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L30N_0	C12	JM4-IO20	47	48	JM4-IO51	G9	IO_L47P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L30P_0	D13	JM4-IO21	49	50	JM4-IO52	E7	IO_L48N_0	I/O	0	VcccIO0
GND	GND	GND	-	-	GND	51	52	JM4-IO53	F7	IO_L48P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L33N_0	B10	JM4-IO22	53	54	JM4-IO54	B3	IO_L51N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L33P_0	A10	JM4-IO23	55	56	JM4-IO55	A3	IO_L51P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L34N_0	D10	JM4-IO24	57	58	GND	-	-	GND	GND	GND
VcccIO0	0	I/O	IO_L34P_0	C10	JM4-IO25	59	60	JM4-IO56	C23	IO_L06N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L35N_0	H12	JM4-IO26	61	62	JM4-IO57	D23	IO_L06P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L35P_0	G12	JM4-IO27	63	64	JM4-IO58	A22	IO_L07N_0	I/O	0	VcccIO0
GND	GND	GND	-	-	GND	65	66	JM4-IO59	B23	IO_L07P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L36N_0	B9	JM4-IO28	67	68	JM4-IO60	G17	IO_L08N_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L36P_0	A9	JM4-IO29	69	70	JM4-IO61	H17	IO_L08P_0	I/O	0	VcccIO0
VcccIO0	0	I/O	IO_L37N_0	D9	JM4-IO30	71	72	VccAux	-	-	out	VccAux	VccAux
VcccIO0	0	I/O	IO_L37P_0	E10	JM4-IO31	73	74	TDI	G7	TDI	JTAG	VccAux	VccAux
VcccIO0	0	I/O	IO_L38N_0	B8	JM4-IO32	75	76	TDO	E23	TDO	JTAG	VccAux	VccAux
VcccIO0	0	I/O	IO_L38P_0	A8	JM4-IO33	77	78	TCK	D4	TCK	JTAG	VccAux	VccAux
GND	GND	GND	-	-	GND	79	80	TMS	A25	TMS	JTAG	VccAux	VccAux

Table 40: pin-out of B2B connector JM4.

18.4 Signal Integrity Considerations

Traces of differential signals pairs are NOT routed symmetrically (as symmetric pairs).

Traces of differential signals pairs are NOT routed with equal length. For applications where traces length has to be matched or timing differences have to be compensated, Table 42 and Table 43 list the trace length of I/O signal lines measured from FPGA balls to B2B connector pins.

Traces of differential signals pairs are routed with a differential impedance between the two traces of 60 ohm.

Pairs of pins that form a differential I/O pair appear colored together in the table. An electronic version of these pin-out tables are available for download from the Trenz Electronic support area of the web site.