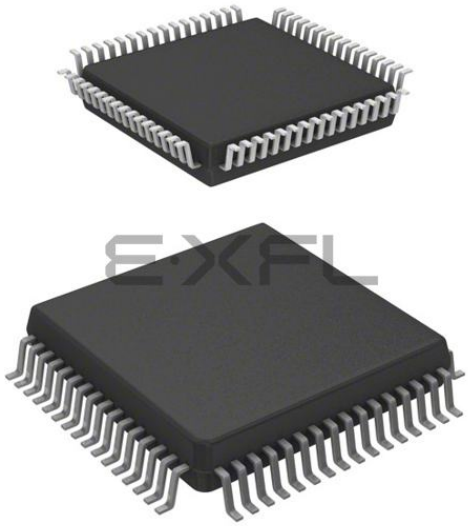

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8.4MHz
Connectivity	CANbus, SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	52
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 15x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908az60amfu

Chapter 1
General Description

1.1 Introduction

The MC68HC908AS60A, MC68HC908AZ60A, and MC68HC908AZ60E are members of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

These parts are designed to emulate the MC68HC08ASxx and MC68HC08AZxx automotive families and may offer extra features which are not available on those devices. It is the user's responsibility to ensure compatibility between the features used on the MC68HC908AS60A, MC68HC908AZ60A, and MC68HC908AZ60E and those which are available on the device which will ultimately be used in the application.

For detailed information regarding the MC68HC908AZ60E refer to Appendix B MC68HC908AZ60E.

1.2 Features

Features of the MC68HC908AS60A and MC68HC908AZ60A include:

- High-Performance M68HC08 Architecture
- Fully Upward-Compatible Object Code with M6805, M146805, and M68HC05 Families
- 8.4 MHz Internal Bus Frequency
- 60 Kbytes of FLASH Electrically Erasable Read-Only Memory (FLASH)
- FLASH Data Security
- 1 Kbyte of On-Chip Electrically Erasable Programmable Read-Only Memory with Security Option (EEPROM)
- 2 Kbyte of On-Chip RAM
- Clock Generator Module (CGM)
- Serial Peripheral Interface Module (SPI)
- Serial Communications Interface Module (SCI)
- 8-Bit, 15-Channel Analog-to-Digital Converter (ADC-15)
- 16-Bit, 6-Channel Timer Interface Module (TIMA-6)
- Programmable Interrupt Timer (PIT)
- System Protection Features
  - Computer Operating Properly (COP) with Optional Reset
  - Low-Voltage Detection with Optional Reset
  - Illegal Opcode Detection with Optional Reset
  - Illegal Address Detection with Optional Reset
- Low-Power Design (Fully Static with Stop and Wait Modes)

Figure 1-4 shows the MC68HC908AS60A 64-pin QFP pin assignments.

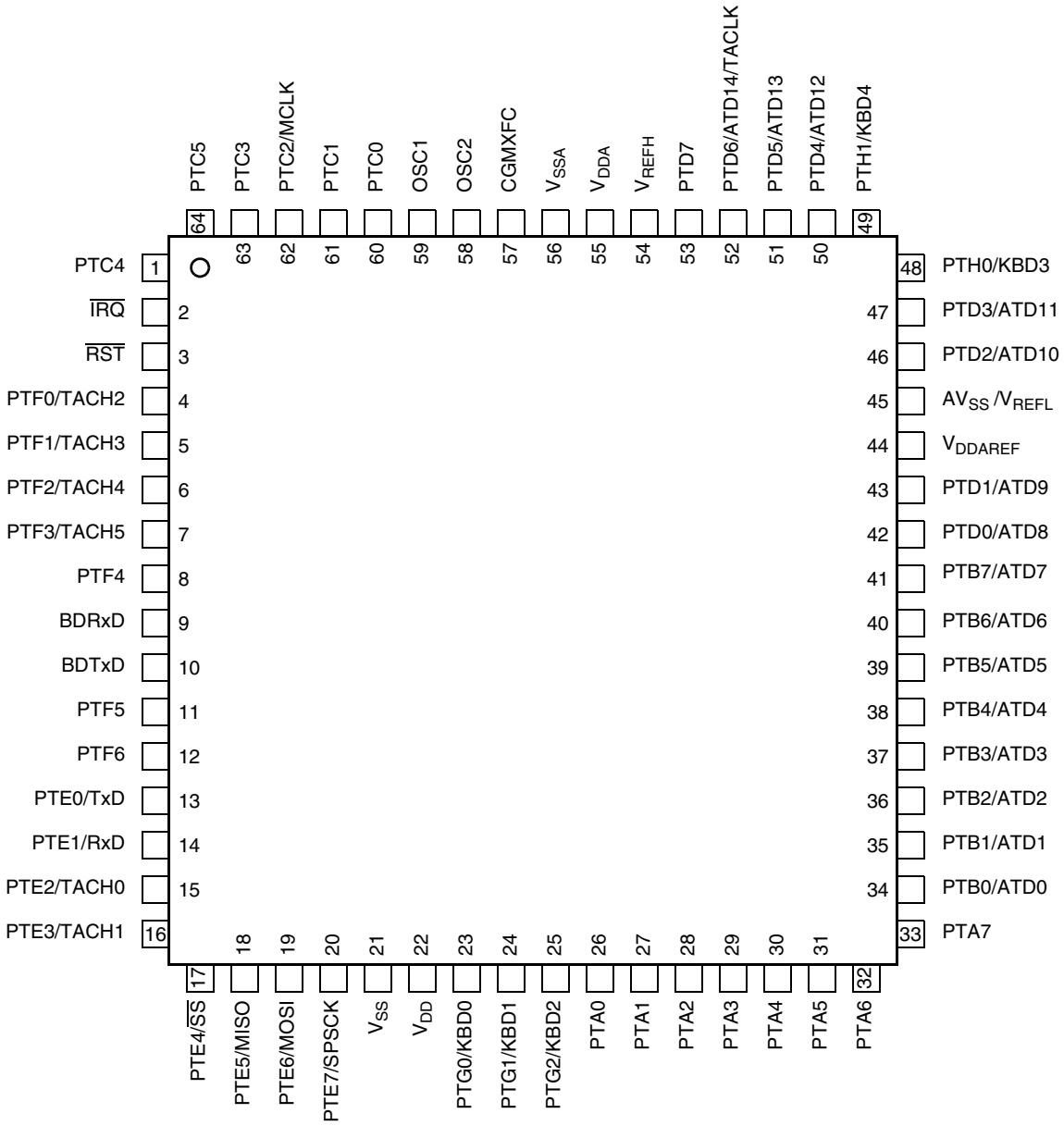


Figure 1-4. MC68HC908AS60A (64-Pin QFP)

1.4.5 Analog Power Supply Pin (V_{DDA})

V_{DDA} is the power supply pin for the analog portion of the Clock Generator Module (CGM). See Chapter 10 Clock Generator Module (CGM).

1.4.6 Analog Ground Pin (V_{SSA})

V_{SSA} is the ground connection for the analog portion of the Clock Generator Module (CGM). See Chapter 10 Clock Generator Module (CGM).

1.4.7 External Filter Capacitor Pin (CGMXFC)

CGMXFC is an external filter capacitor connection for the Clock Generator Module (CGM). See Chapter 10 Clock Generator Module (CGM).

1.4.8 ADC Analog Power Supply Pin (V_{DDAREF})

V_{DDAREF} is the power supply pin for the analog portion of the Analog-to-Digital Converter (ADC). See Chapter 26 Analog-to-Digital Converter (ADC).

1.4.9 ADC Analog Ground Pin (AV_{SS}/V_{REFL})

The AV_{SS}/V_{REFL} pin provides both the analog ground connection and the reference low voltage for the Analog-to-Digital Converter (ADC). See Chapter 26 Analog-to-Digital Converter (ADC).

1.4.10 ADC Reference High Voltage Pin (V_{REFH})

V_{REFH} provides the reference high voltage for the Analog-to-Digital Converter (ADC). See Chapter 26 Analog-to-Digital Converter (ADC).

1.4.11 Port A Input/Output (I/O) Pins (PTA7–PTA0)

PTA7–PTA0 are general-purpose bidirectional I/O port pins. See Chapter 22 Input/Output Ports.

1.4.12 Port B I/O Pins (PTB7/ATD7–PTB0/ATD0)

Port B is an 8-bit special function port that shares all eight pins with the Analog-to-Digital Converter (ADC). See Chapter 26 Analog-to-Digital Converter (ADC) and Chapter 22 Input/Output Ports.

1.4.13 Port C I/O Pins (PTC5–PTC0)

PTC5–PTC3 and PTC1–PTC0 are general-purpose bidirectional I/O port pins. PTC2/MCLK is a special function port that shares its pin with the system clock which has a frequency equivalent to the system clock. See Chapter 22 Input/Output Ports.

1.4.14 Port D I/O Pins (PTD7–PTD0/ATD8)

Port D is an 8-bit special-function port that shares seven of its pins with the Analog-to-Digital Converter module (ADC-15), one of its pins with the Timer Interface Module A (TIMA), and one more of its pins with the Timer Interface Module B (TIMB). See Chapter 25 Timer Interface Module A (TIMA), Chapter 20 Timer Interface Module B (TIMB), Chapter 26 Analog-to-Digital Converter (ADC) and Chapter 22 Input/Output Ports.

EEDIVSECD — EEPROM-1 Divider Security Disable

This bit enables/disables the security feature of the EE1DIV registers. When EE1DIV security feature is enabled, the state of the registers EE1DIVH and EE1DIVL are locked (including EEDIVSECD bit). The EE1DIVHNVR and EE1DIVLNVR nonvolatile memory registers are also protected from being erased/programmed.

1 = EE1DIV security feature disabled
0 = EE1DIV security feature enabled

EEDIV[10:0] — EEPROM-1 timebase prescaler

These prescaler bits store the value of EE1DIV which is used as the divisor to derive a timebase of 35μs from the selected reference clock source (CGMXCLK or bus block in the CONFIG-2 register) for the EEPROM-1 related internal timer and circuits. EEDIV[10:0] bits are readable at any time. They are writable when EELAT = 0 and EEDIVSECD = 1.

The EE1DIV value is calculated by the following formula:

$$EE1DIV = INT[Reference\ Frequency(Hz) \times 35 \times 10^{-6} + 0.5]$$

Where the result inside the bracket is rounded down to the nearest integer value

For example, if the reference frequency is 4.9152MHz, the EE1DIV value is 172

NOTE

Programming/erasing the EEPROM with an improper EE1DIV value may result in data lost and reduce endurance of the EEPROM device.

6.5.5 EEPROM-1 Timebase Divider Nonvolatile Register

The 16-bit EEPROM-1 timebase divider nonvolatile register consists of two 8-bit registers: EE1DIVHNVR and EE1DIVLNVR. The contents of these two registers are respectively loaded into the EEPROM-1 timebase divider registers, EE1DIVH and EE1DIVL, after a reset.

These two registers are erased and programmed in the same way as an EEPROM-1 byte.

Address: $FE10

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EEDIVS-ECD	R	R	R	R	EEDIV10	EEDIV9	EEDIV8
Reset:	Unaffected by reset; $FF when blank							

R = Reserved

Figure 6-7. EEPROM-1 Divider Nonvolatile Register High (EE1DIVHNVR))

Address: $FE11

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EEDIV7	EEDIV6	EEDIV5	EEDIV4	EEDIV3	EEDIV2	EEDIV1	EEDIV0
Reset:	Unaffected by reset; $FF when blank							

Figure 6-8. EEPROM-1 Divider Nonvolatile Register Low (EE1DIVLNVR)

8.7 Instruction Set Summary

Table 8-1 provides a summary of the M68HC08 instruction set.

Table 8-1. Instruction Set Summary (Sheet 1 of 6)

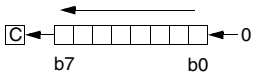
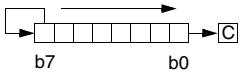
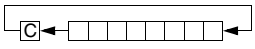
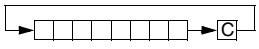
Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X ADC *opr*,SP ADC *opr*,SP	Add with Carry	A ← (A) + (M) + (C)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A9 B9 C9 D9 E9 F9 9EE9 9ED9	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X ADD *opr*,SP ADD *opr*,SP	Add without Carry	A ← (A) + (M)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	AB BB CB DB EB FB 9EEB 9EDB	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
AIS #*opr*	Add Immediate Value (Signed) to SP	SP ← (SP) + (16 « M)	–	–	–	–	–	–	IMM	A7	ii	2
AIX #*opr*	Add Immediate Value (Signed) to H:X	H:X ← (H:X) + (16 « M)	–	–	–	–	–	–	IMM	AF	ii	2
AND #*opr* AND *opr* AND *opr* AND *opr*,X AND *opr*,X AND ,X AND *opr*,SP AND *opr*,SP	Logical AND	A ← (A) & (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A4 B4 C4 D4 E4 F4 9EE4 9ED4	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X ASL *opr*,SP	Arithmetic Shift Left (Same as LSL)		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR *opr*,X ASR *opr*,SP	Arithmetic Shift Right		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	37 47 57 67 77 9E67	dd ff ff	4 1 1 4 3 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + rel ? (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BCLR *n*, *opr*	Clear Bit n in M	Mn ← 0	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? (Z) = 1	–	–	–	–	–	–	REL	27	rr	3
BGE *opr*	Branch if Greater Than or Equal To (Signed Operands)	PC ← (PC) + 2 + *rel* ? (N ⊕ V) = 0	–	–	–	–	–	–	REL	90	rr	3
BGT *opr*	Branch if Greater Than (Signed Operands)	PC ← (PC) + 2 + *rel* ? (Z) ǀ (N ⊕ V) = 0	–	–	–	–	–	–	REL	92	rr	3
BHCC *rel*	Branch if Half Carry Bit Clear	PC ← (PC) + 2 + *rel* ? (H) = 0	–	–	–	–	–	–	REL	28	rr	3
BHCS *rel*	Branch if Half Carry Bit Set	PC ← (PC) + 2 + *rel* ? (H) = 1	–	–	–	–	–	–	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? (C) ǀ (Z) = 0	–	–	–	–	–	–	REL	22	rr	3

Table 8-1. Instruction Set Summary (Sheet 5 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
PULA	Pull A from Stack	SP ← (SP + 1); Pull (A)	–	–	–	–	–	–	INH	86		2
PULH	Pull H from Stack	SP ← (SP + 1); Pull (H)	–	–	–	–	–	–	INH	8A		2
PULX	Pull X from Stack	SP ← (SP + 1); Pull (X)	–	–	–	–	–	–	INH	88		2
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X ROL *opr*,SP	Rotate Left through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	39 49 59 69 79 9E69	dd ff ff	4 1 1 4 3 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X ROR *opr*,SP	Rotate Right through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	4 1 1 4 3 5
RSP	Reset Stack Pointer	SP ← $FF	–	–	–	–	–	–	INH	9C		1
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	↕	INH	80		7
RTS	Return from Subroutine	SP ← SP + 1; Pull (PCH) SP ← SP + 1; Pull (PCL)	–	–	–	–	–	–	INH	81		4
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X SBC *opr*,SP SBC *opr*,SP	Subtract with Carry	A ← (A) – (M) – (C)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A2 B2 C2 D2 E2 F2 9EE2 9ED2	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
SEC	Set Carry Bit	C ← 1	–	–	–	–	–	1	INH	99		1
SEI	Set Interrupt Mask	I ← 1	–	–	1	–	–	–	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X STA *opr*,SP STA *opr*,SP	Store A in M	M ← (A)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	B7 C7 D7 E7 F7 9EE7 9ED7	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
STHX *opr*	Store H:X in M	(M:M + 1) ← (H:X)	0	–	–	↕	↕	–	DIR	35	dd	4
STOP	Enable Interrupts, Stop Processing, Refer to MCU Documentation	I ← 0; Stop Processing	–	–	0	–	–	–	INH	8E		1
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X STX *opr*,SP STX *opr*,SP	Store X in M	M ← (X)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	BF CF DF EF FF 9EEF 9EDF	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X SUB *opr*,SP SUB *opr*,SP	Subtract	A ← (A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5

Chapter 12
Configuration Register (CONFIG-2)

12.1 Introduction

This chapter describes the configuration register (CONFIG-2). This register contains bits that configure these options:

- Configures the device to either the MC68HC08AZxx emulator or the MC68HC08ASxx emulator
- Disables the CAN module

12.2 Functional Description

The configuration register is a write-once register. Out of reset, the configuration register will read the default. Once the register is written, further writes will have no effect until a reset occurs.

Address: $FE09

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	EEDIV CLK	R	R	MSCAND	AT60A	R	R	AZxx
Write:					R			
Reset:	0	0	0	1	1	0	0	0

R = Reserved

Figure 12-1. Configuration Register (CONFIG-2)

AT60A — Device Indicator

This read-only bit is used to distinguish an MC68HC908AS60A and MC68HC908AZ60A from older non-'A' suffix versions.

1 = 'A' version
0 = Non-'A' version

EEDIVCLK — EEPROM Timebase Divider Clock Select Bit

This bit selects the reference clock source for the EEPROM-1 and EEPROM-2 timebase divider modules.

1 = EExDIV clock input is driven by internal bus clock
0 = EExDIV clock input is driven by CGMXCLK

MSCAND — MSCAN Disable Bit

MSCAND disables the MSCAN module. (See Chapter 23 MSCAN Controller (MSCAN08)).

1 = MSCAN module disabled
0 = MSCAN Module enabled

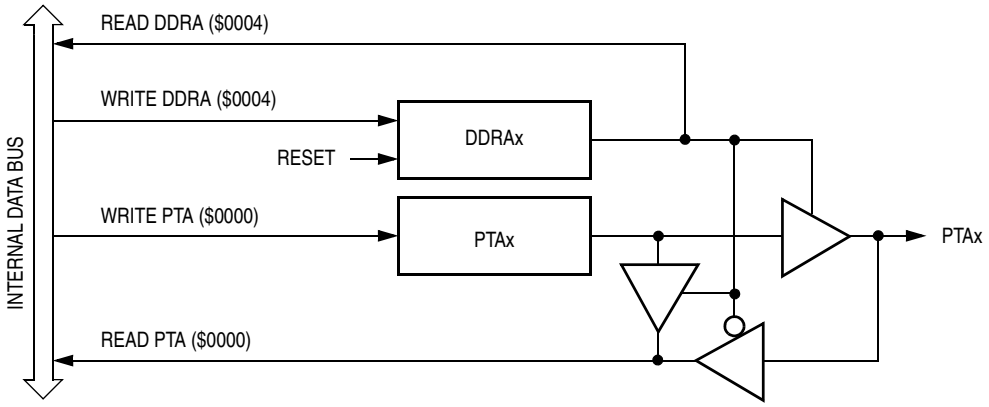


Figure 22-4. Port A I/O Circuit

When bit DDRAx is a logic 1, reading address $0000 reads the PTAx data latch. When bit DDRAx is a logic 0, reading address $0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. Table 22-1 summarizes the operation of the port A pins.

Table 22-1. Port A Pin Functions

DDRA Bit	PTA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PTA	
			Read/Write	Read	Write
0	X	Input, Hi-Z	DDRA[7:0]	Pin	PTA[7:0](1)
1	X	Output	DDRA[7:0]	PTA[7:0]	PTA[7:0]

X = don't care
Hi-Z = high impedance
1. Writing affects data register, but does not affect input.

22.3.2 Data Direction Register B

Data direction register B determines whether each port B pin is an input or an output. Writing a logic 1 to a DDRB bit enables the output buffer for the corresponding port B pin; a logic 0 disables the output buffer.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Reset:	0	0	0	0	0	0	0	0

Figure 22-6. Data Direction Register B (DDRB)

DDRB[7:0] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[7:0], configuring all port B pins as inputs.

1 = Corresponding port B pin configured as output
0 = Corresponding port B pin configured as input

NOTE

Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1.

Figure 22-7 shows the port B I/O logic.

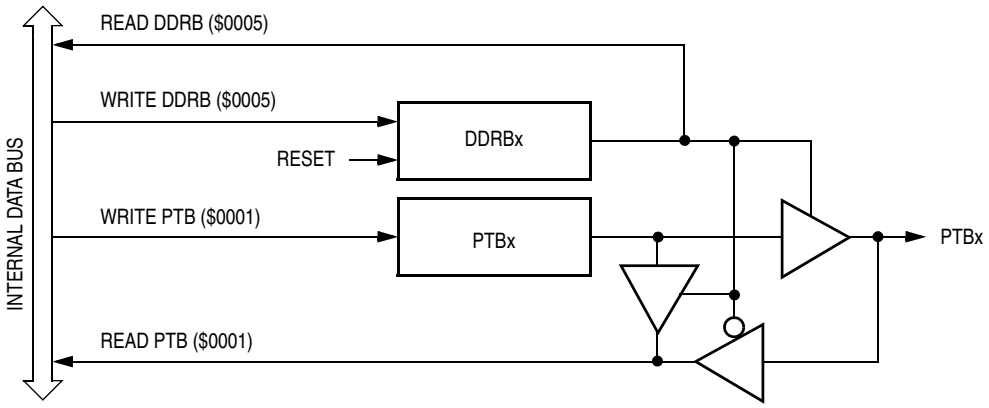


Figure 22-7. Port B I/O Circuit

When bit DDRBx is a logic 1, reading address $0001 reads the PTBx data latch. When bit DDRBx is a logic 0, reading address $0001 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. Table 22-2 summarizes the operation of the port B pins.

Table 22-2. Port B Pin Functions

DDRB Bit	PTB Bit	I/O Pin Mode	Accesses to DDRB	Accesses to PTB	
			Read/Write	Read	Write
0	X	Input, Hi-Z	DDRB[7:0]	Pin	PTB[7:0](1)
1	X	Output	DDRB[7:0]	PTB[7:0]	PTB[7:0]

X = don't care
Hi-Z = high impedance
1. Writing affects data register, but does not affect input.

22.8 Port G

Port G is a 3-bit special function port that shares all of its pins with the keyboard interrupt module (KBD). Note that Port G is only available on 64-pin package options.

22.8.1 Port G Data Register

The port G data register contains a data latch for each of the three port G pins.

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	PTG2	PTG1	PTG0
Write:	R	R	R	R	R			
Reset:	Unaffected by Reset							
Alternative Function:						KBD2	KBD1	KBD0

R = Reserved

Figure 22-20. Port G Data Register (PTG)

PTG[2:0] — Port G Data Bits

These read/write bits are software programmable. Data direction of each port G pin is under the control of the corresponding bit in data direction register G. Reset has no effect on PTG[2:0].

KBD[2:0] — Keyboard Wakeup pins

The keyboard interrupt enable bits, KBIE[2:0], in the keyboard interrupt control register, enable the port G pins as external interrupt pins (See Chapter 24 Keyboard Module (KBI)). Enabling an external interrupt pin will override the corresponding DDRGx.

22.8.2 Data Direction Register G

Data direction register G determines whether each port G pin is an input or an output. Writing a logic 1 to a DDRG bit enables the output buffer for the corresponding port G pin; a logic 0 disables the output buffer.

Address: $000E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	DDRG2	DDRG1	DDRG0
Write:	R	R	R	R	R			
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 22-21. Data Direction Register G (DDRG)

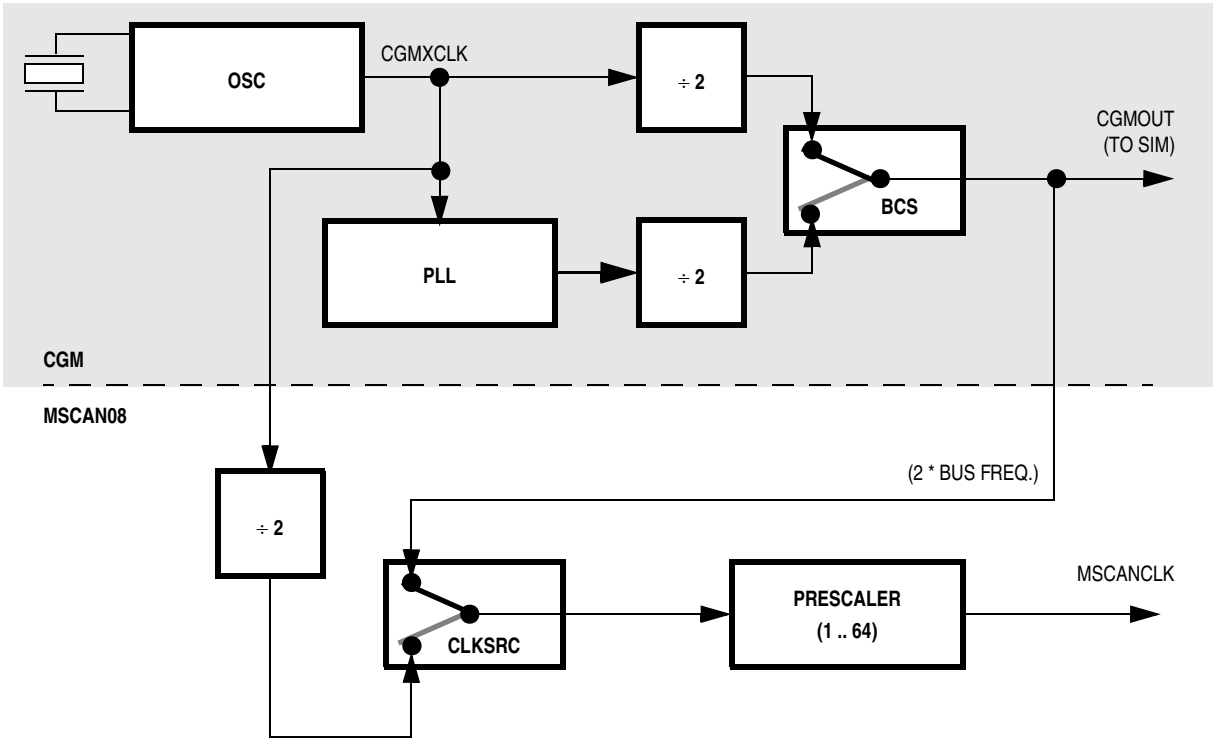


Figure 23-7. Clocking Scheme

The clock source bit (CLKSRC) in the MSCAN08 module control register (CMCR1) (see 23.13.1 MSCAN08 Module Control Register 0) defines whether the MSCAN08 is connected to the output of the crystal oscillator or to the PLL output.

The clock source has to be chosen such that the tight oscillator tolerance requirements (up to 0.4%) of the CAN protocol are met.

NOTE

If the system clock is generated from a PLL, it is recommended to select the crystal clock source rather than the system clock source due to jitter considerations, especially at faster CAN bus rates.

A programmable prescaler is used to generate out of the MSCAN08 clock the time quanta (Tq) clock. A time quantum is the atomic unit of time handled by the MSCAN08.

$$f_{Tq} = \frac{f_{MSCANCLK}}{\text{Presc value}}$$

A bit time is subdivided into three segments[1] (see Figure 23-8).

- SYNC_SEG: This segment has a fixed length of one time quantum. Signal edges are expected to happen within this section.
- Time segment 1: This segment includes the PROP_SEG and the PHASE_SEG1 of the CAN standard. It can be programmed by setting the parameter TSEG1 to consist of 4 to 16 time quanta.

1. For further explanation of the underlying concepts please refer to ISO/DIS 11 519-1, Section 10.3.

23.13.10 MSCAN08 Receive Error Counter

Address: $050E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 23-24. Receiver Error Counter (CRXERR)

This register reflects the status of the MSCAN08 receive error counter. The register is read only.

23.13.11 MSCAN08 Transmit Error Counter

Address: $050F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 23-25. Transmit Error Counter (CTXERR)

This register reflects the status of the MSCAN08 transmit error counter. The register is read only.

NOTE

Both error counters may only be read when in Sleep or Soft Reset mode.

Another way to avoid a false interrupt:

1. Configure the keyboard pins as outputs by setting the appropriate DDRG bits in data direction register G.
2. Configure the keyboard pins as outputs by setting the appropriate DDRH bits in data direction register H.
3. Write logic 1s to the appropriate port G and port H data register bits.
4. Enable the KBI pins by setting the appropriate KBIEx bits in the keyboard interrupt enable register.

24.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low-power-consumption standby modes.

24.5.1 Wait Mode

The keyboard module remains active in wait mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of wait mode.

24.5.2 Stop Mode

The keyboard module remains active in stop mode. Clearing the IMASKK bit in the keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode.

24.6 Keyboard Module During Break Interrupts

The BCFE bit in the break flag control register (BFCR) enables software to clear status bits during the break state. See Chapter 13 Break Module (BRK).

To allow software to clear the KEYF bit during a break interrupt, write a logic 1 to the BCFE bit. If KEYF is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the KEYF bit during the break state, write a logic 0 to the BCFE bit. With BCFE at logic 0, writing to the keyboard acknowledge bit (ACKK) in the keyboard status and control register during the break state has no effect. See 24.7.1 Keyboard Status and Control Register.

24.7 I/O Registers

The following registers control and monitor operation of the keyboard module:

- Keyboard status and control register (KBSCR)
- Keyboard interrupt enable register (KBIER)

Register Name and Address TACH4H — $0033

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	Indeterminate after Reset							

Register Name and Address TACH4L — $0034

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	Indeterminate after Reset							

Register Name and Address TACH5H — $0036

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	Indeterminate after Reset							

Register Name and Address TACH5L — $0037

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	Indeterminate after Reset							

Figure 25-9. TIMA Channel Registers (TACH0H/L–TACH5H/L) (Sheet 3 of 3)

27.3.1 BDLC Operating Modes

The BDLC has five main modes of operation which interact with the power supplies, pins, and the remainder of the MCU as shown in Figure 27-3.

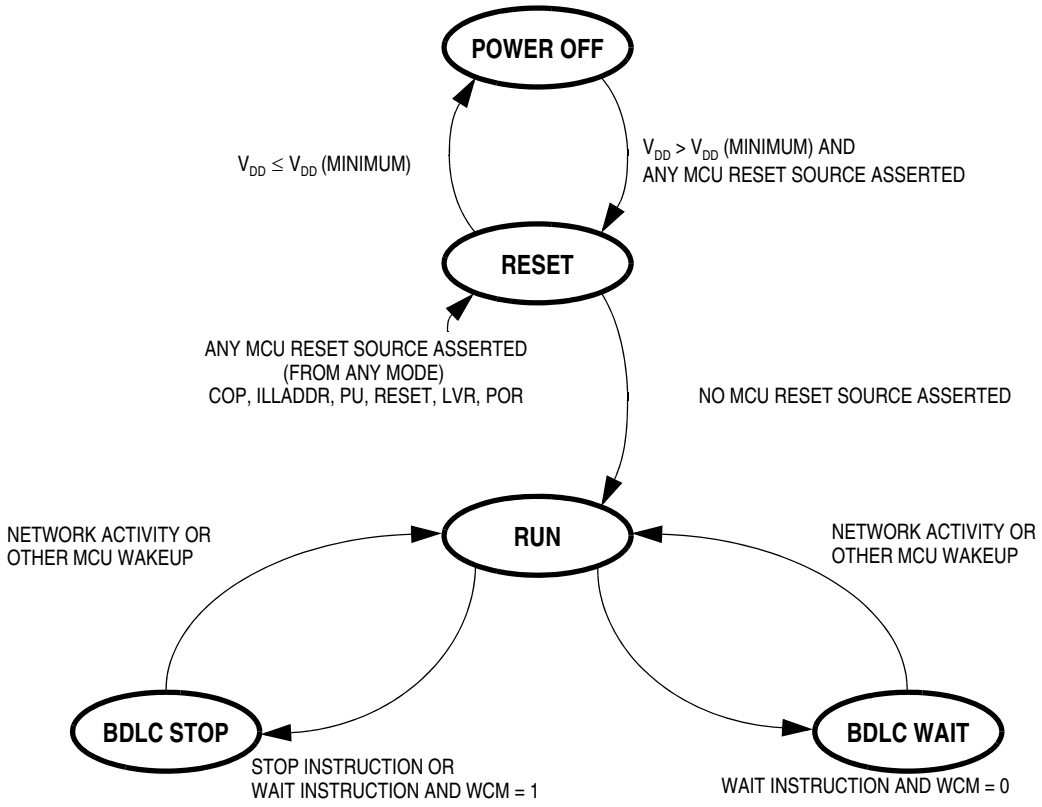


Figure 27-3. BDLC Operating Modes State Diagram

27.3.1.1 Power Off Mode

This mode is entered from reset mode whenever the BDLC supply voltage, V_{DD}, drops below its minimum specified value for the BDLC to guarantee operation. The BDLC will be placed in reset mode by low-voltage reset (LVR) before being powered down. In this mode, the pin input and output specifications are not guaranteed.

27.3.1.2 Reset Mode

This mode is entered from the power off mode whenever the BDLC supply voltage, V_{DD}, rises above its minimum specified value (V_{DD} –10%) and some MCU reset source is asserted. The internal MCU reset must be asserted while powering up the BDLC or an unknown state will be entered and correct operation cannot be guaranteed. Reset mode is also entered from any other mode as soon as one of the MCU's possible reset sources (such as LVR, POR, COP watchdog, and reset pin, etc.) is asserted.

In reset mode, the internal BDLC voltage references are operative; V_{DD} is supplied to the internal circuits which are held in their reset state; and the internal BDLC system clock is running. Registers will assume their reset condition. Outputs are held in their programmed reset state. Therefore, inputs and network activity are ignored.

28.1.10 CGM Acquisition/Lock Time Information

Description[1]	Symbol	Min	Typ[2]	Max[2]	Unit	Notes
Manual Mode Time to Stable	t_{ACQ}	—	$(8 \times V_{DDA}) / (f_{CGMXCLK} \times K_{ACQ})$	—	s	If C_F Chosen Correctly
Manual Stable to Lock Time	t_{AL}	—	$(4 \times V_{DDA}) / (f_{CGMXCLK} \times K_{TRK})$	—	s	If C_F Chosen Correctly
Manual Acquisition Time	t_{LOCK}	—	$t_{ACQ}+t_{AL}$	—	s	
Tracking Mode Entry Frequency Tolerance	D_{TRK}	0	—	± 3.6	%	
Acquisition Mode Entry Frequency Tolerance	D_{UNT}	± 6.3	—	± 7.2	%	
LOCK Entry Freq. Tolerance	D_{LOCK}	0	—	± 0.9	%	
LOCK Exit Freq. Tolerance	D_{UNL}	± 0.9	—	± 1.8	%	
Reference Cycles per Acquisition Mode Measurement	n_{ACQ}	—	32	—	—	
Reference Cycles per Tracking Mode Measurement	n_{TRK}	—	128	—	—	
Automatic Mode Time to Stable	t_{ACQ}	n_{ACQ}/f_{XCLK}	$(8 \times V_{DDA}) / (f_{XCLK} \times K_{ACQ})$		s	If C_F Chosen Correctly
Automatic Stable to Lock Time	t_{AL}	n_{TRK}/f_{XCLK}	$(4 \times V_{DDA}) / (f_{XCLK} \times K_{TRK})$	—	s	If C_F Chosen Correctly
Automatic Lock Time	t_{LOCK}	—	0.65	25	ms	
PLL Jitter, Deviation of Average Bus Frequency over 2 ms[3]		0	—	± (f_{CRYS}) x (.025%) x (N/4)	%	N = VCO Freq. Mult.
K value for automatic mode time to stable	K_{acq}	—	0.2	—	—	
K value	K_{trk}	—	0.004	—	—	

1. V_{DD} = 5.0 Vdc ± 0.5 V, V_{SS} = 0 Vdc, T_A = –40°C to T_A (MAX), unless otherwise noted.
2. Conditions for typical and maximum values are for Run mode with $f_{CGMXCLK}$ = 8 MHz, f_{BUSDES} = 8 MHz, N = 4, L = 7, discharged C_F = 15 nF, V_{DD} = 5 Vdc.
3. Guaranteed by not tested. Refer to Chapter 10 Clock Generator Module (CGM) for guidance on the use of the PLL.

B.7 Configuration Register (CONFIG-3)

This section describes the configuration register (CONFIG-3). This register is unused on the MC68HC908AZ60A. This register contains one bit that configures the following option:

Disables slew rate control for the SPI pins

The configuration register is a write-once register. Once the register is written, further writes will have no effect until a reset occurs.

Address: $FE0B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	R	R	R	R	R	R	SPISRD	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure B-4. Configuration Register (CONFIG-3)

SPISRD — SPI Slew Rate Disable

This bit disables the slew rate controlled outputs for SCK, MOSI, and MISO pins.

1 = SPI slew rate is disabled
0 = SPI slew rate is enabled

B.8 SCI

The incorrect operation, signified by the "Note" in the Idle Characters paragraph of the SCI section of this document has been corrected. The following note does not apply to the MC68HC908AZ60E.

NOTE

When a break sequence is followed immediately by an idle character, this SCI design exhibits a condition in which the break character length is reduced by one half bit time. In this instance, the break sequence will consist of a valid start bit, eight or nine data bits (as defined by the M bit in SCC1) of logic 0 and one half data bit length of logic 0 in the stop bit position followed immediately by the idle character. To ensure a break character of the proper length is transmitted, always queue up a byte of data to be transmitted while the final break sequence is in progress.

B.9 MSCAN

The MSCAN08 errata on the MC68HC908AZ60A has been fixed on the MC68HC908AZ60E. For 32-bit and 16-bit identifier acceptance modes, an extended ID CAN frame with a stuff bit between ID16 and ID15 will not be rejected. No software work around is required.

Major Changes Between Revision 2.0 and Revision 1.0

The following table lists the major changes between the current revision of the MC68HC908AZ60A Technical Data Book, Rev 2.0, and the previous revision, Rev 1.0.

Section affected	Description of change
Timer Interface Module B (TIMB)	Various changes for clarification.
Programmable Interrupt Timer (PIT)	
Timer Interface Module A (TIMA)	

Major Changes Between Revision 1.0 and Revision 0.0

The following table lists the major changes between the current revision of the MC68HC908AZ60A Technical Data Book, Rev 1.0, and the previous revision, Rev 0.0.

Section affected	Description of change
General Description	Highlighted that Keyboard Interrupt Module only available in 64 QFP. Corrected device name in Figure 5 title. Added ADC supply and reference pins to pin descriptions. Corrected text in numerous pin descriptions. Added VDDA and VSSA pins to Table 1-External Pins Summary. Added Table 2-Clock Signal Naming Conventions. Added FLASH and RAM to Table 3-Clock Source Summary. Corrected part numbers in Table 4-MC Order Numbers.
Memory Map	Corrected type errors. Corrected various addresses and register names in Figure 1-Memory Map. Corrected numerous register bit descriptions in Figure 2-I/O Data, Status and Control Registers to match module sections. Added Additional Status and Control Registers section and moved register descriptions accordingly. Corrected bit descriptions to match module sections. Added Vector Addresses and Priority section and moved Table 4-Vector Addresses accordingly.
FLASH-1 and FLASH-2	Both sections altered significantly to better align module descriptions across groups within Freescale using 0.5µ TSMC/SST FLASH. Numerous additions submitted by applications engineering for further clarification of functional operation.
EEPROM-1 and EEPROM-2	Both sections altered significantly to better align module descriptions across groups within Freescale using 0.5µ TSMC/SST FLASH. Numerous additions submitted by applications engineering for further clarification of functional operation.
Clock Generator Module (CGM)	Corrected clock signal names and associated timing parameters for consistency and to match signal naming conventions. Additional textual description added to Reaction Time Calculation subsection.
Configuration Register 2 (CONFIG-2)	Corrected Figure 1-Configuration Register reserved bit descriptions for consistency.