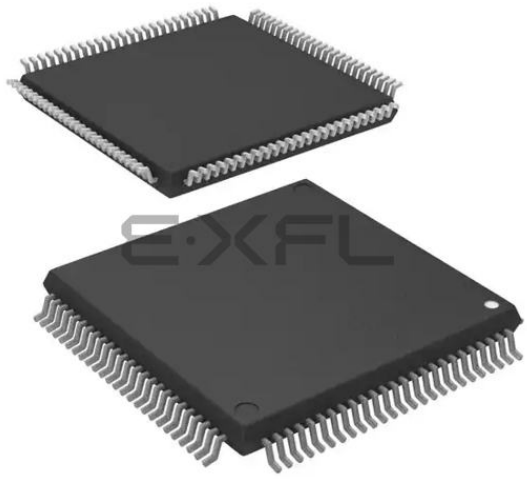
Renesas Electronics America Inc - UPD70F3761GC-UEU-AX Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	77
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3761gc-ueu-ax

How to Use This Manual

Readers

This manual is intended for users who wish to understand the functions of the V850ES/JG3-H and V850ES/JH3-H and design application systems using the V850ES/JG3-H and V850ES/JH3-H.

Purpose

This manual is intended to give users an understanding of the hardware functions of the V850ES/JG3-H and V850ES/JH3-H shown in the **Organization** below.

Organization

The manual of these products is divided into two volumes: Hardware (this volume) and Architecture (**V850ES Architecture User's Manual**).

Hardware	Architecture
• Pin functions	• Data types
• CPU function	• Register set
• On-chip peripheral functions	• Instruction format and instruction set
• Flash memory programming	• Interrupts and exceptions
• Electrical specifications	• Pipeline operation

How to Read This Manual

It is assumed that the readers of this manual have general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

To understand the overall functions of the V850ES/JG3-H and V850ES/JH3-H
→Read this manual according to the **CONTENTS**.

To find the details of a register where the name is known
→Use **APPENDIX C REGISTER INDEX**.

Register format
→The name of the bit whose number is in angle brackets (<>) in the figure of the register format of each register is defined as a reserved word in the device file.

To understand the details of an instruction function
→Refer to the **V850ES Architecture User's Manual** available separately.

To know the electrical specifications of the V850ES/JG3-H and V850ES/JH3-H
→Refer to the **CHAPTER 33 ELECTRICAL SPECIFICATIONS**.

The "yyy bit of the xxx register" is described as the "xxx.yyy bit" in this manual. Note with caution that if "xxx.yyy" is described as is in a program, however, the compiler/assembler cannot recognize it correctly.

The mark <R> shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what: " field.

3.2 CPU Register Set

The registers of the V850ES/JG3-H and V850ES/JH3-H can be classified into two types: general-purpose program registers and dedicated system registers. All the registers are 32 bits wide.

For details, refer to the **V850ES Architecture User's Manual**.

(1) Program register set

31		0
r0	(Zero register)	
r1	(Assembler-reserved register)	
r2		
r3	(Stack pointer (SP))	
r4	(Global pointer (GP))	
r5	(Text pointer (TP))	
r6		
r7		
r8		
r9		
r10		
r11		
r12		
r13		
r14		
r15		
r16		
r17		
r18		
r19		
r20		
r21		
r22		
r23		
r24		
r25		
r26		
r27		
r28		
r29		
r30	(Element pointer (EP))	
r31	(Link pointer (LP))	

31		0
PC	(Program counter)	

(2) System register set

31		0
EIPC	(Interrupt status saving register)	
EIPSW	(Interrupt status saving register)	

FEPC	(NMI status saving register)
FEPSW	(NMI status saving register)

ECR	(Interrupt source register)

PSW	(Program status word)

CTPC	(CALLT execution status saving register)
CTPSW	(CALLT execution status saving register)

DBPC	(Exception/debug trap status saving register)
DBPSW	(Exception/debug trap status saving register)

CTBP	(CALLT base pointer)

(2) Internal RAM area

Up to 60 KB are reserved as the internal RAM area.

The V850ES/JG3-H and V850ES/JH3-H include a data-only RAM of 8 KB in addition to the internal RAM.

The RAM capacity of V850ES/JG3-H and V850ES/JH3-H is as follows.

Table 3-3 RAM area

Generic Name	Product Name	Internal RAM	Data-only RAM	Total RAM
V850ES/JG3-H	μPD70F3760, 70F3770	32 KB	8 KB	40 KB
	μPD70F3761	40 KB		48 KB
	μPD70F3762	48 KB		56 KB
V850ES/JH3-H	μPD70F3765, 70F3771	32 KB		40 KB
	μPD70F3766	40 KB		48 KB
	μPD70F3767	48 KB		56KB

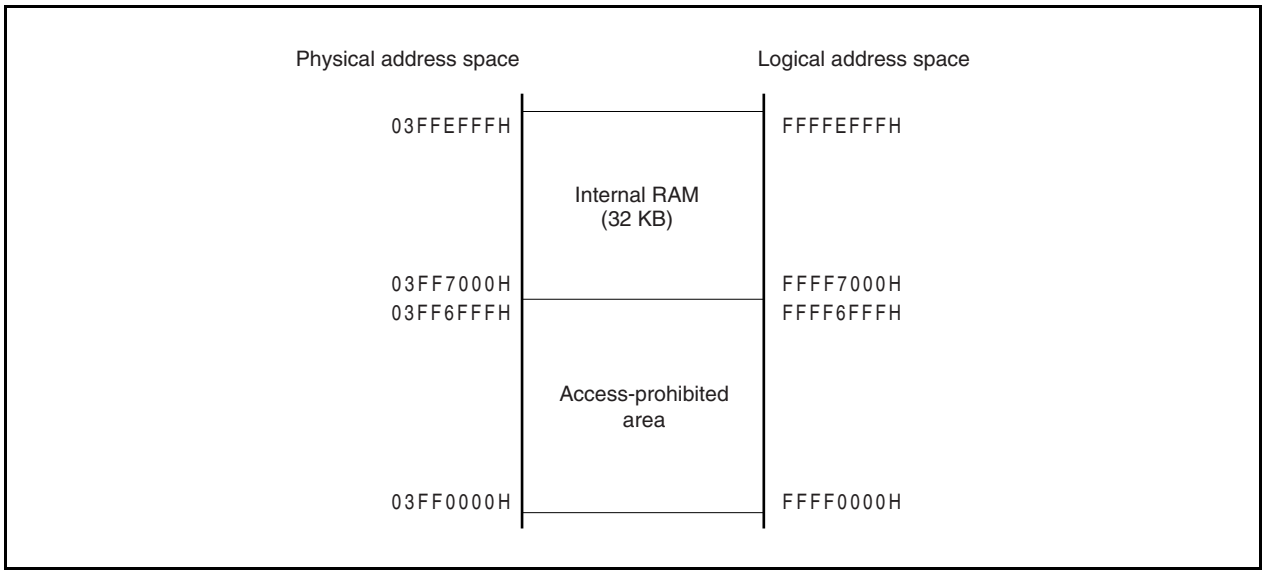
(a) Internal RAM (32 KB)

32 KB are allocated to addresses 03FF7000H to 03FFEFFFH in the following products.

Accessing addresses 03FF0000H to 03FF6FFFH is prohibited.

- μPD70F3760, 70F3770, 70F3765, 70F3771

Figure 3-7. Internal RAM Area (32 KB)



(3) Port 9 mode control register (PMC9)

After reset: 0000H R/W Address: PMC9 FFFFF452H,
PMC9L FFFFF452H, PMC9H FFFFF453H

	15	14	13	12	11	10	9	8
PMC9 (PMC9H)	PMC915	PMC914	PMC913	PMC912	PMC911	PMC910	PMC99	PMC98

	7	6	5	4	3	2	1	0
(PMC9L)	PMC97	PMC96	PMC95	PMC94	PMC93	PMC92	PMC91	PMC90

PMC915	Specification of P915 pin operation mode
0	I/O port
1	TIAA50 input/TOAA50 output/INTP18 input/A15 output[Note]

PMC914	Specification of P914 pin operation mode
0	I/O port
1	TIAA51 input/TOAA51 output/INTP17 input/A14 output[Note]

PMC913	Specification of P913 pin operation mode
0	I/O port
1	TOAB1OFF input/INTP16 input/A13 output[Note]

PMC912	Specification of P912 pin operation mode
0	I/O port
1	$\overline{\text{SCKF3}}$ I/O/A12 output[Note]

PMC911	Specification of P911 pin operation mode
0	I/O port
1	SOF3 output/RXDC2 input/INTP15 input/A11 output[Note]

PMC910	Specification of P910 pin operation mode
0	I/O port
1	SIF3 input/TXDC2 output/INTP14 input/A10 output[Note]

PMC99	Specification of P99 pin operation mode
0	I/O port
1	$\overline{\text{SCKF1}}$ I/O/INTP13 input/A9 output[Note]

PMC98	Specification of P98 pin operation mode
0	I/O port
1	SOF1 output/INTP12 input/A8 output[Note]

Note V850ES/JH3-H only

Remarks 1. The PMC9 register can be read or written in 16-bit units.
However, when using the higher 8 bits of the PMC9 register as the PMC9H register and the lower 8 bits as the PMC9L register, they can be read or written in 8-bit or 1-bit units.

2. To read/write bits 8 to 15 of the PMC9 register in 8-bit or 1-bit units, specify them as bits 0 to 7 of the PMC9H register.

4.3.12 Port CT

Port CT is a 2-bit (V850ES/JG3-H)/4-bit (V850ES/JH3-H) port for which I/O settings can be controlled in 1-bit units.

Port CT includes the following alternate-function pins.

Table 4-17. Port CT Alternate-Function Pins

Pin Name	Pin No.		Alternate-Function Pin Name	I/O	Remark
	V850ES/JG3-H	V850ES/JH3-H			
PCT0	58	76	$\overline{WR0}$	Output	–
PCT1	59	77	$\overline{WR1}$	Output	
PCT4	–	87	$\overline{RD}$	Output	
PCT6	–	88	ASTB	Output	

(1) Port CT register (PCT)

(a) V850ES/JG3-H

After reset: 00H (output latch) R/W Address: FFFFF00AH

	7	6	5	4	3	2	1	0
PCT	0	0	0	0	0	0	PCT1	PCT0

PCTn	Output data control (in output mode) (n = 0, 1)
0	Outputs 0.
1	Outputs 1.

(b) V850ES/JH3-H

After reset: 00H (output latch) R/W Address: FFFFF00AH

	7	6	5	4	3	2	1	0
PCT	0	PCT6	0	PCT4	0	0	PCT1	PCT0

PCMn	Output data control (in output mode) (n = 0, 1, 4, 6)
0	Outputs 0.
1	Outputs 1.

Figure 7-27. Register Setting for Operation in One-Shot Pulse Output Mode (2/2)

(d) TAAn I/O control register 2 (TAAnIOC2)

	TAAnEES1	TAAnEES0	TAAnETS1	TAAnETS0
TAAnIOC2	0	0	0/1	0/1

Select valid edge of external trigger input

(e) TAAn counter read buffer register (TAAnCNT)

The value of the 16-bit counter can be read by reading the TAAnCNT register.

(f) TAAn capture/compare registers 0 and 1 (TAAnCCR0 and TAAnCCR1)

If D_0 is set to the TAAnCCR0 register and D_1 to the TAAnCCR1 register, the active level width and output delay period of the one-shot pulse are as follows.

Active level width = $(D_0 - D_1 + 1) \times$ Count clock cycle

Output delay period = $(D_1) \times$ Count clock cycle

Caution One-shot pulses are not output even in the one-shot pulse output mode, if the set value of the TAAnCCR1 register is greater than the set value of the TAAnCCR0 register.

Remarks 1. TAAn I/O control register 1 (TAAnIOC1) and TAAn option register 0 (TAAnOPT0) are not used in the one-shot pulse output mode.

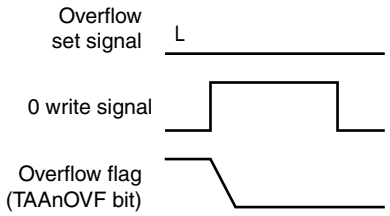
2. n = 0 to 3, 5

(2) Operation timing in pulse width measurement mode

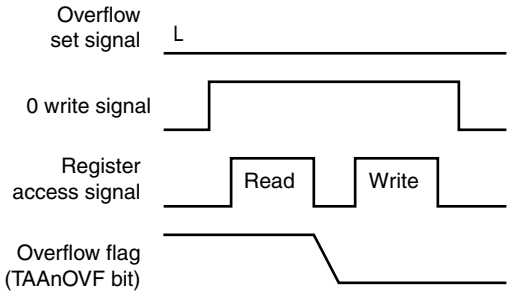
(a) Clearing overflow flag

The overflow flag can be cleared to 0 by clearing the TAAnOVF bit to 0 with the CLR instruction and by writing 8-bit data (bit 0 is 0) to the TAAnOPT0 register. To accurately detect an overflow, read the TAAnOVF bit when it is 1, and then clear the overflow flag by using a bit manipulation instruction.

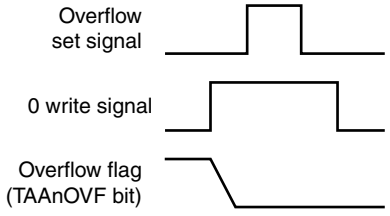
(i) Operation to write 0 (without conflict with setting)



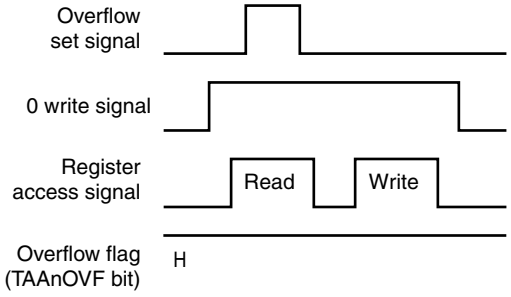
(iii) Operation to clear to 0 (without conflict with setting)



(ii) Operation to write 0 (conflict with setting)



(iv) Operation to clear to 0 (conflict with setting)



Remark n = 0 to 3, 5

To clear the overflow flag to 0, read the overflow flag to check if it is set to 1, and clear it with the CLR instruction. If 0 is written to the overflow flag without checking if the flag is 1, the set information of the overflow may be erased by writing 0 ((ii) in the above chart). Therefore, software may judge that no overflow has occurred even when an overflow has actually occurred.

If execution of the CLR instruction conflicts with occurrence of an overflow when the overflow flag is cleared to 0 with the CLR instruction, the overflow flag remains set (1) even after execution of the clear instruction.

7.6.2 PWM output mode (during timer-tuned operation)

This section explains the PWM output mode of timer-tuned operation. For combinations of timer-tuned operations, see **Table 7-7**. This section presents an example of a timer-tuned operation with TAB0 and TAA5.

The TAB0CCR0 register of the master timer (TAB0) is used as a compare register for cycle, and the TAB0CCR1, TAB0CCR2, and TAB0CCR3 registers of the master timer (TAB0) and the TAA5CCR0 and TAA5CCR1 registers of the slave timer (TAA5) are used as compare registers for duty.

The compare registers can be rewritten during operation and the rewriting method is batch writing.

Batch writing is enabled when the TAB0CCR1 register of the master timer (TAB0) is written, and all the compare registers of the master and slave timers are rewritten or the same value is written to them when an interrupt, which is generated if the value of the TAB0CCR0 register of the master timer (TAB0) matches the value of the timer counter, is generated.

(1) Settings in PWM output mode

[Initials setting]

Master timer: TAB0CTL0.TAB0CE = 0 (operation disabled)
Slave timer: TAA5CTL0.TAA5CE = 0 (operation disabled)

[Initial settings of master timer (TAB0)]

- TAB0CTL1.TAB0MD2 to TAB0CTL1.TAB0MD0 = 100 (setting of PWM output mode)
- TAB0OPT0.TAB0CCS3 to TAB0OPT0.TAB0CCS0 = 0000 (setting of capture/compare select bit to “compare”.)
- TAB0CCR0, TAB0CCR1, TAB0CCR2, and TAB0CCR3 registers are set.

[Initial settings of slave timer (TAA5)]

- TAA5CTL1.TAA5SYE = 1 (setting of timer-tuned operation)
- TAA5CTL1.TAA5MD2 to TAA5CTL1.TAA5MD0 = 101 (setting of free-running timer mode)
- TAA5OPT0.TAA5CCS1 and TAA5OPT0.TAA5CCS0 = 00 (setting of capture/compare select bit to “compare”.)
- TAA5CCR0 and TAA5CCR1 registers are set.

Remark The initial settings of the master timer and slave timer may be performed in any order.

[Starting counting]

<1> Set TAB0CTL0.TAB0CE of the master timer to 1.
<2> Start counting.
<3> Changing the setting of the register during operation
- The compare register can be rewritten (batch rewrite).

[End condition]

- Set TAB0CTL0.TAB0CE of the master timer to 0.

(b) Basic timing 2

[Register setting condition]

- TT0CTL2.TT0ECM1 and TT0CTL2.TT0ECM0 bits = 00
  The 16-bit counter is not cleared even when its count value matches the value of the CCRn buffer register (a = 0, 1).
- TT0CTL2.TT0LDE bit = 0
  The set value of the TT0CCR0 register is not transferred to the 16-bit counter after the counter underflows.
- TT0IOC3.TT0SCE bit = 0, and TT0IOC3.TT0ECS1 and TT0IOC3.TT0ECS0 bits = 00
  Specification of clearing the 16-bit counter when the edge of the encoder clear input signal (TECR0 pin) is detected (no edge specified)

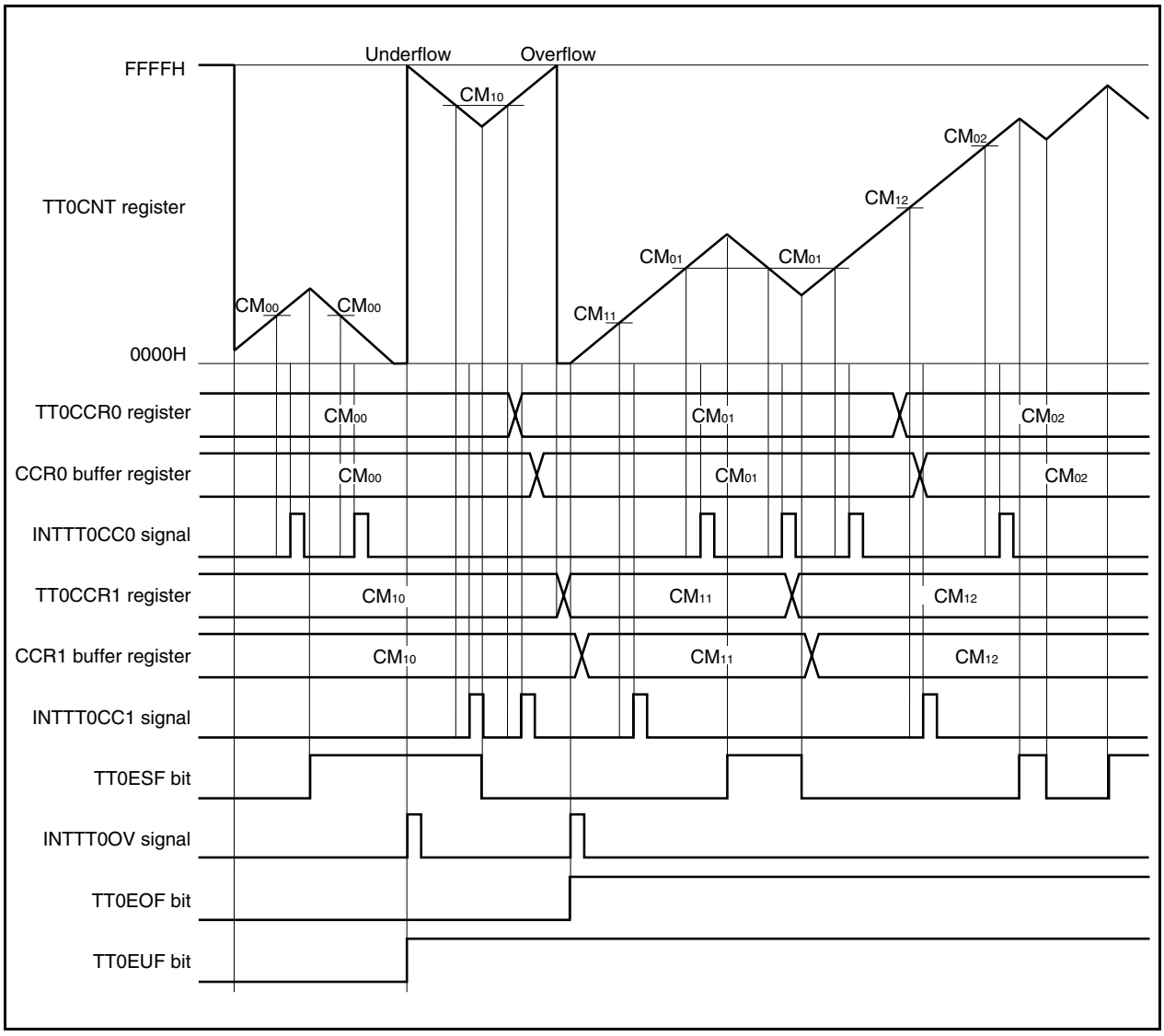
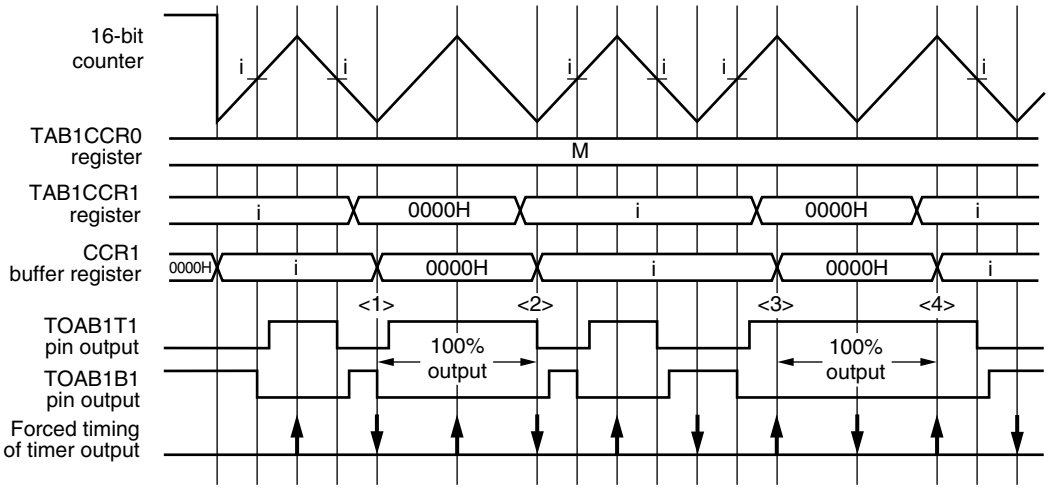


Figure 11-10. 100% PWM Output Waveform (With Dead Time)



<1> 100% output is selected by the valley interrupt (with a match with the 16-bit counter).
The valley interrupt forcibly lowers the timer output, but raising the timer output takes precedence when the value of the TAB1CCRm register matches the value of the 16-bit counter. As a result, the 100% output is produced.

<2> 100% output is canceled by the valley interrupt (without a match with the 16-bit counter).
The valley interrupt forcibly lowers the timer output. This cancels the 100% output.

<3> 100% output is selected by the crest interrupt (without a match with the 16-bit counter).
The crest interrupt forcibly raises the timer output. This produces the 100% output.

<4> 100% output is canceled by the crest interrupt (without a match with the 16-bit counter).
The crest interrupt forcibly raises the timer output. This cancels the 100% output.

Remarks 1. ↑ means forcible raising and ↓ means forcible lowering.

2. m = 1 to 3

(4) Real-time counter control register 3 (RC1CC3)

The RC1CC3 register is an 8-bit register that controls the interval interrupt function and RTCDIV pin.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFFAE0H

	7	6	5	4	3	2	1	0
RC1CC3	RINTE	CLOE2	CKDIV	0	0	ICT2	ICT1	ICT0

RINTE	Interval interrupt (INTRTC2) control
0	Does not generate interval interrupt.
1	Generates interval interrupt.

CLOE2	RTCDIV pin output control
0	Disables RTCDIV pin output.
1	Enables RTCDIV pin output.

CKDIV	RTCDIV pin output frequency selection
0	Outputs 512 Hz (1.95 ms) from RTCDIV pin.
1	Outputs 16.384 kHz (0.061 ms) from RTCDIV pin.

ICT2	ICT1	ICT0	Interval interrupt (INTRTC2) selection
0	0	0	$2^6/f_{XT}$ (1.953125 ms)
0	0	1	$2^7/f_{XT}$ (3.90625 ms)
0	1	0	$2^8/f_{XT}$ (7.8125 ms)
0	1	1	$2^9/f_{XT}$ (15.625 ms)
1	0	0	$2^{10}/f_{XT}$ (31.25 ms)
1	0	1	$2^{11}/f_{XT}$ (62.5 ms)
1	1	×	$2^{12}/f_{XT}$ (125 ms)

Cautions 1. See 12.4.7 Changing INTRTC2 interrupt setting during the real-time counter operation when rewriting the RINTE bit during real-time counter operation (RC1PWR bit = 1).

2. The RTCDIV output operates as follows when the CLOE2 bit setting is changed.

- **When changed from 0 to 1: A pulse set by the CKDIV bit is output after two clocks (2 x 32.768 kHz) or less.**
- **When changed from 1 to 0: Output of the RTCDIV output is stopped after two clocks (2 x 32.768 kHz) or less (fixed to low level).**

3. See 12.4.7 Changing INTRTC2 interrupt setting during the real-time counter operation when rewriting the ICT2 to ICT0 bits while the real-time counter operates (RC1PWR bit = 1).

19.4 Registers

I²C00 to I²C02 are controlled by the following registers.

- IIC control registers 0 to 2 (IICC0 to IICC2)
- IIC status registers 0 to 2 (IICS0 to IICS2)
- IIC flag registers 0 to 2 (IICF0 to IICF2)
- IIC clock select registers 0 to 2 (IICCL0 to IICCL2)
- IIC function expansion registers 0 to 2 (IICX0 to IICX2)
- IIC division clock select registers 0, 1 (OCKS0, OCKS1)

The following registers are also used.

- IIC shift registers 0 to 2 (IIC0 to IIC2)
- Slave address registers 0 to 2 (SVA0 to SVA2)

Remark For the alternate-function pin settings, see **Table 4-20 Settings When Port Pins Are Used for Alternate Functions**.

(1) IIC control registers 0 to 2 (IICC0 to IICC2)

The IICCn registers enable/stop I²C0n operations, set the wait timing, and set other I²C operations (n = 0 to 2).

These registers can be read or written in 8-bit or 1-bit units. However, set the SPIEn, WTIMn, and ACKEn bits when the IICEn bit is 0 or during the wait period. When changing the IICEn bit from “0” to “1”, these bits can also be set at the same time.

Reset sets these registers to 00H.

<3> Mask setting for CAN module 1 (mask 1) (Example)
(Using CAN1 address mask 1 registers L and H (C1MASK1L and C1MASK1H))

CMID28	CMID27	CMID26	CMID25	CMID24	CMID23	CMID22	CMID21	CMID20	CMID19	CMID18
1	0	0	0	0	1	0	1	1	1	1

CMID17	CMID16	CMID15	CMID14	CMID13	CMID12	CMID11	CMID10	CMID9	CMID8	CMID7
1	1	1	1	1	1	1	1	1	1	1

CMID6	CMID5	CMID4	CMID3	CMID2	CMID1	CMID0
1	1	1	1	1	1	1

1: Not compared (masked)
0: Compared

The CMID27 to CMID24 and CMID22 bits are cleared to 0, and the CMID28, CMID23, and CMID21 to CMID0 bits are set to 1.

(25) UF0 INT clear 4 register (UF0IC4)

This register controls clearing the interrupt sources indicated by the UF0IS4 register.

This register is write-only, in 8-bit units. If this register is read, the value FFH is read.

FW can clear an interrupt source by writing 0 to the corresponding bit of this register. Even a bit that is automatically cleared to 0 by hardware can be cleared by FW before it is cleared by hardware. Writing 0 to a bit of this register automatically sets the bit to 1. Writing 1 is invalid.

The related bits are invalid if each endpoint is not supported by the setting of the UF0EnIM register (n = 1 to 4, 7) and the current setting of the interface.

	7	6	5	4	3	2	1	0	Address	After reset
UF0IC4	1	1	SETINTC	1	1	1	1	1	00200044H	FFH

Bit position	Bit name	Function
5	SETINTC	This bit clears the SET_INT interrupt. 0: Clear

21.6.9 Bulk-out register

(1) UF0 EP2 bulk-out transfer data register (UF0EP2BO)

The UF0EP2BO register writes the bulk-out transfer data of EP2.

The UF0EP2BO register can be read or written in 8-bit or 16-bit units.

After reset: 0000H R Address: 00210000H

	15	14	13	12	11	10	9	8
UF0EP2BO	0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
EP2BO7	EP2BO6	EP2BO5	EP2BO4	EP2BO3	EP2BO2	EP2BO1	EP2BO0

Bit position	Bit name	Function
7 to 0	EP2BO7 to EP2BO0	Reading the bulk-out transfer data of EP2. Reading the input data from the EPC macro from this register. If using this register, setting the address (00210000H) in DMA source address register (DSAn (n = 0 to 3)) of DMAC. In addition, set the RQnUR0E (n = 0 to 3) bit of the UFDRQEN register to 1 to assign a DMA channel.

Caution If either of the following operations is performed, the data stored in this register is read out and the next bulk-out transfer data is stored into this register.

- **The UF0EP2BO register is read during program execution.**
- **The UF0EP2BO register is monitored on the memory window while the debugger is being used.**

21.7 STALL Handshake or No Handshake

Errors of USBF are defined to be handled as follows.

Transfer Type	Transaction	Target Packet	Error Type	Function Response	Processing
Control transfer/ bulk transfer/ interrupt transfer	IN/OUT/SETUP	Token	Endpoint not supported	No response	None
			Endpoint transfer direction mismatch	No response	None
			CRC error	No response	None
			Bit stuffing error	No response	None
Control transfer/ bulk transfer	OUT/SETUP	Data	Timeout	No response	None
			PID check error	No response	None
			Unsupported PID (other than Data PID)	No response	None
			CRC error	No response	Discard received data
			Bit stuffing error	No response	Discard received data
	OUT	Data	Data PID mismatch	ACK	Discard received data
Control transfer (SETUP stage)	SETUP	Data	Overrun	No response	Discard received data
Control transfer (data stage)	OUT	Data	Overrun	No response[Note 1]	Set SNDSTL bit of UF0SDS register to 1 and discard received data
Control transfer (status stage)	OUT	Data	Overrun	ACK or no response[Note 2]	Set SNDSTL bit of UF0SDS register to 1 and discard received data
Bulk transfer	OUT	Data	Overrun	No response[Note 1]	Set EnHALT bit of UF0EnSL register (n = 0 to 4, 7) to 1
Control transfer/ bulk transfer/ interrupt transfer	IN	Handshake	PID check error	–	Hold transferred data and re-transfer data[Note 3]
			Unsupported PID (other than ACK PID)	–	Hold transferred data and re-transfer data[Note 3]
			Timeout	–	Hold transferred data and re-transfer data[Note 3]

Notes 1. A STALL response is made to re-transfer by the host.

2. An ACK response is made if the transfer data is of less than MaxPacketSize and the data received in the status stage is discarded. If MaxPacketSize is exceeded, no response is made, the SNDSTL bit of the UF0SDS register is set to 1, and the received data is discarded.

3. If an OUT transaction indicating a change from the data stage to the status stage is received during control transfer, an error is not handled and it is assumed that reception has been correctly completed.

Cautions 1. It is judged by the Alternative Setting number currently set whether the target Endpoint is valid or invalid.

2. For the response to the request included in control transfer to/from Endpoint0, see 21.5 Requests.

21.8 Register Values in Specific Status

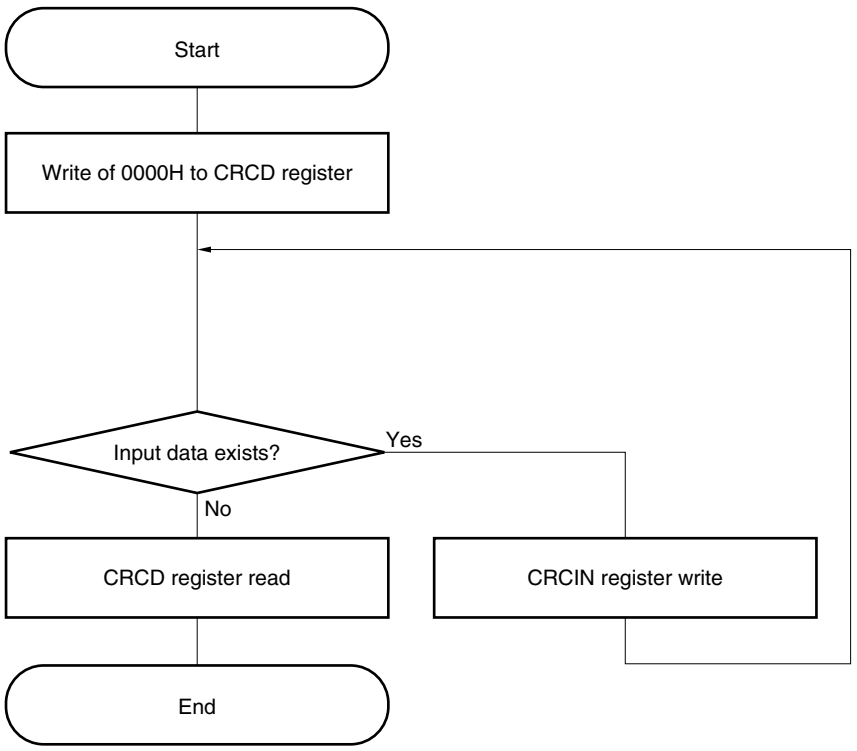
Table 21-8. Register Values in Specific Status (1/2)

Register Name	After CPU Reset ($\overline{\text{RESET}}$)	After Bus Reset
UF0E0N register	00H	Value is held.
UF0E0NA register	00H	Value is held.
UF0EN register	00H	Value is held.
UF0ENM register	00H	Value is held.
UF0SDS register	00H	Value is held.
UF0CLR register	00H	Value is held.
UF0SET register	00H	Value is held.
UF0EPS0 register	00H	Value is held.
UF0EPS1 register	00H	Value is held.
UF0EPS2 register	00H	Value is held.
UF0IS0 register	00H	Value is held.
UF0IS1 register	00H	Value is held.
UF0IS2 register	00H	Value is held.
UF0IS3 register	00H	Value is held.
UF0IS4 register	00H	Value is held.
UF0IM0 register	00H	Value is held.
UF0IM1 register	00H	Value is held.
UF0IM2 register	00H	Value is held.
UF0IM3 register	00H	Value is held.
UF0IM4 register	00H	Value is held.
UF0IC0 register	FFH	Value is held.
UF0IC1 register	FFH	Value is held.
UF0IC2 register	FFH	Value is held.
UF0IC3 register	FFH	Value is held.
UF0IC4 register	FFH	Value is held.
UF0IDR register	00H	Value is held.
UF0DMS0 register	00H	Value is held.
UF0DMS1 register	00H	Value is held.
UF0FIC0 register	00H	Value is held.
UF0FIC1 register	00H	Value is held.
UF0DEND register	00H	Value is held.
UF0GPR register	00H	Value is held.
UF0MODC register	00H	Value is held.
UF0MODS register	00H	Bit 2 (CONF): Cleared (0), Other bits: Value is held.
UF0AIFN register	00H	Value is held.
UF0AAS register	00H	Value is held.
UF0ASS register	00H	00H
UF0E1IM register	00H	Value is held.
UF0E2IM register	00H	Value is held.

29.5 Usage Method

How to use the CRC logic circuit is described below.

Figure 29-3. CRC Operation Flow



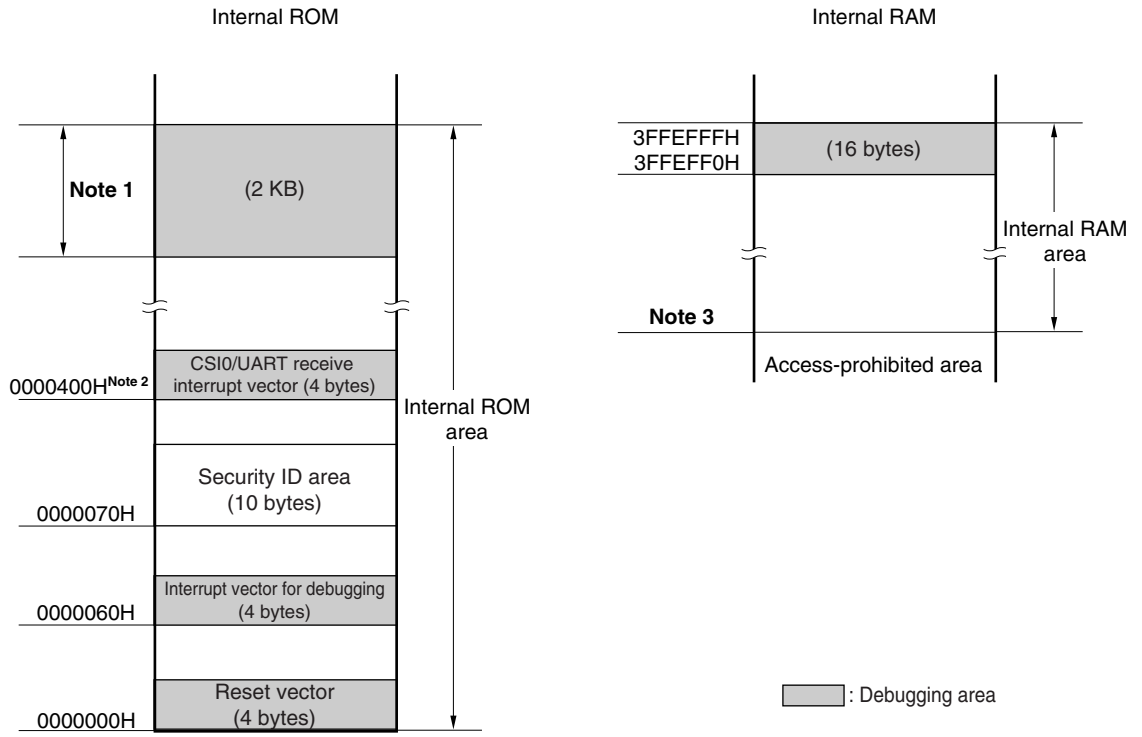
[Basic usage method]

<1> Write 0000H to the CRCD register.

<2> Write the required quantity of data to the CRCIN register.

<3> Read the CRCD register.

Figure 32-4. Memory Spaces Where Debug Monitor Programs Are Allocated



Notes 1. Address values vary depending on the product.

	Internal ROM Size	Address Value
μPD70F3760, 70F3765, 70F3770, 70F3771	256 KB	003F800H to 003FFFFH
μPD70F3761, 70F3766	384 KB	005F800H to 003FFFFH
μPD70F3762, 70F3767	512 KB	007F800H to 007FFFFH

2. This is the address when CSIF0 is used. It starts at 0000406H when CSIF3 is used, and at 00004A0H when UARTC0 is used.

3. Address values vary depending on the product.

	Internal RAM Size	Address Value
μPD70F3760, 70F3765, 70F3770, 70F3771	32 KB	3FF7000H
μPD70F3761, 70F3766	40 KB	3FF5000H
μPD70F3762, 70F3767	48 KB	3FF3000H

(3/4)

Edition	Description	Chapter
2nd	Modification of **3.4.4 (2) (d) Data-only RAM (8 KB)**	**CHAPTER 3 CPU FUNCTION**
	Addition of **Caution** to **3.4.4 (2) (d) Data-only RAM (8 KB)**	
	Modification of **Figure 3-10. Data only RAM (8 KB)**	
	Modification of **3.4.4 (4) External memory area**	
	Modification of **3.4.6 Peripheral I/O registers**	
	Modification of **Figure 7-23. (d) TAAn I/O control register 2 (TAAnIOC2)**	**CHAPTER 7 16-BIT TIMER/EVENT COUNTER AA (TAA)**
	Modification of **Figure 7-27. (d) TAAn I/O control register 2 (TAAnIOC2)**	
	Modification of **7.8 Cascade Connection**	
	Modification of **Table 12-1 Configuration of Real-Time Counter**	**CHAPTER 12 REAL-TIME COUNTER**
	Modification of **Figure 12-1. Block Diagram of Real-Time Counter**	
	Addition of **12.3 (17) Prescaler mode register 0 (PRSM0)**	
	Addition of **12.3 (18) Prescaler compare register 0 (PRSCM0)**	
	Addition of **Note 2** to **18.4 (2) CSIFn control register 1 (CFnCTL1)**	**CHAPTER 18 3-WIRE VARIABLE-LENGTH SERIAL I/O (CSIF)**
	Modification of **Table 19-4. Extension Code Bit Definitions**	**CHAPTER 19 I2C BUS**
	Modification of **Figure 19-23. Example of Master to Slave Communication (When 9-Clock Wait Is Selected for Both Master and Slave)**	
	Modification of **Figure 19-24. Example of Slave to Master Communication (When 8-Clock Wait for Master and 9-Clock Wait for Slave Are Selected)**	
	Modification of **Figure 21-1. Block Diagram of USB Function Controller**	**CHAPTER 21 USB FUNCTION CONTROLLER (USBF)**
	Addition of **22.3 (7) External DMA request enable register (EXDRQEN)**	**CHAPTER 22 DMA FUNCTION (DMA CONTROLLER)**
	Modification of **Table 25-10. Operating Status in Subclock Operation Mode**	**CHAPTER 25 STANDBY FUNCTION**
	Modification of **Figure 28-1. Block Diagram of Low-Voltage Detector**	**CHAPTER 28 LOW-VOLTAGE DETECTOR (LVI)**
	Modification of **33.5.1 I/O level**	**CHAPTER 33 ELECTRICAL SPECIFICATIONS**
	Modification of **33.7.2 (1) (a) Read/write cycle (CLKOUT asynchronous)**	
	Modification of **33.7.2 (1) (b) Read/write cycle (CLKOUT synchronous): In multiplexed bus mode/separate bus mode**	
	Modification of **33.7.2 (2) (a) CLKOUT asynchronous**	
	33.7.2 (2) (b) CLKOUT synchronous	
	Modification of **33.7.2 (6) (a) Master mode**	
	Modification of **33.7.2 (6) (b) Slave mode**	
	Modification of **33.8 (10) A/D converter**	
	Addition of **APPENDIX E REVISION HISTORY**	**APPENDIX E REVISION HISTORY**