Renesas Electronics America Inc - UPD70F3765GF-GAT-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3765gf-gat-ax

(11/14)

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
FFFFFA24H	UARTC2 status register	UC2STR	R/W	√	√		00H
FFFFFA26H	UARTC2 receive data register	UC2RX	R			√	01FFH
FFFFFA26H	UARTC2 receive data register L	UC2RXL			√		FFH
FFFFFA28H	UARTC2 transmit data register	UC2TX	R/W			√	01FFH
FFFFFA28H	UARTC2 transmit data register L	UC2TXL			√		FFH
FFFFFA2AH	UARTC2 option control register 1	UC2OPT1		√	√		00H
FFFFFA30H	UARTC3 control register 0	UC3CTL0		√	√		10H
FFFFFA31H	UARTC3 control register 1	UC3CTL1			√		00H
FFFFFA32H	UARTC3 control register 2	UC3CTL2			√		FFH
FFFFFA33H	UARTC3 option control register 0	UC3OPT0		√	√		14H
FFFFFA34H	UARTC3 status register	UC3STR		√	√		00H
FFFFFA36H	UARTC3 receive data register	UC3RX	R			√	01FFH
FFFFFA36H	UARTC3 receive data register L	UC3RXL			√		FFH
FFFFFA38H	UARTC3 transmit data register	UC3TX	R/W			√	01FFH
FFFFFA38H	UARTC3 transmit data register L	UC3TXL			√		FFH
FFFFFA3AH	UARTC3 option control register 1	UC3OPT1		√	√		00H
FFFFFA40H	UARTC4 control register 0	UC4CTL0		√	√		10H
FFFFFA41H	UARTC4 control register 1	UC4CTL1			√		00H
FFFFFA42H	UARTC4 control register 2	UC4CTL2			√		FFH
FFFFFA43H	UARTC4 option control register 0	UC4OPT0		√	√		14H
FFFFFA44H	UARTC4 status register	UC4STR		√	√		00H
FFFFFA46H	UARTC4 receive data register	UC4RX	R			√	01FFH
FFFFFA46H	UARTC4 receive data register L	UC4RXL			√		FFH
FFFFFA48H	UARTC4 transmit data register	UC4TX	R/W			√	01FFH
FFFFFA48H	UARTC4 transmit data register L	UC4TXL			√		FFH
FFFFFA4AH	UARTC4 option control register 1	UC4OPT1		√	√		00H
FFFFFA80H	TMM0 control register 0	TM0CTL0		√	√		00H
FFFFFA84H	TMM0 compare register 0	TM0CMP0				√	0000H
FFFFFA90H	TMM1 control register 0	TM1CTL0		√	√		00H
FFFFFA94H	TMM1 compare register 0	TM1CMP0				√	0000H
FFFFFAA0H	TMM2 control register 0	TM2CTL0		√	√		00H
FFFFFAA4H	TMM2 compare register 0	TM2CMP0				√	0000H
FFFFFAB0H	TMM3 control register 0	TM3CTL0		√	√		00H
FFFFFAB4H	TMM3 compare register 0	TM3CMP0				√	0000H
FFFFFAD0H	Sub-count register	RC1SUBC	R			√	0000H
FFFFFAD2H	Second count register	RC1SEC	R/W		√		00H
FFFFFAD3H	Minute count register	RC1MIN			√		00H
FFFFFAD4H	Hour count register	RC1HOUR			√		12H
FFFFFAD5H	Week count register	RC1WEEK			√		00H
FFFFFAD6H	Day count register	RC1DAY			√		01H
FFFFFAD7H	Month count register	RC1MONTH			√		01H
FFFFFAD8H	Year count register	RC1YEAR			√		00H
FFFFFAD9H	Time error correction register	RC1SUBU		√	√		00H

4.3.7 Port 6

Port 6 is a 6-bit port for which I/O settings can be controlled in 1-bit units.

Port 6 includes the following alternate-function pins.

Table 4-12. Port 6 Alternate-Function Pins

Pin Name	Pin No.		Alternate-Function Pin Name	I/O	Remark
	V850ES/JG3-H	V850ES/JH3-H			
P60	65	90	TOAB1T1/TOAB11/TIAB11 /$\overline{\text{WAIT}}$Note	I/O	–
P61	66	91	TOAB1B1/TOAB10/TIAB10 /$\overline{\text{RD}}$Note	I/O	
P62	67	92	TOAB1T2/TOAB12/TIAB12 /ASTBNote	I/O	
P63	68	93	TOAB1B2/TRGAB1/$\overline{\text{CS0}}$Note	I/O	
P64	69	94	TOAB1T3/TOAB13/TIAB13 /$\overline{\text{CS2}}$Note	I/O	
P65	70	95	TOAB1B3/EVTAB1/$\overline{\text{CS3}}$Note	I/O	

Note V850ES/JG3-H only

Caution The P60 to P65 pins have hysteresis characteristics in the input mode of the alternate-function pin, but do not have the hysteresis characteristics in the port mode.

(1) Port 6 register (P6)

After reset: 00H (output latch) R/W Address: FFFFF40CH

	7	6	5	4	3	2	1	0
P6	0	0	P65	P64	P63	P62	P61	P60

P6n	Output data control (in output mode) (n = 0 to 5)
0	Outputs 0.
1	Outputs 1.

7.4 Registers

The registers that control TAAn are as follows.

- TAAn control register 0 (TAAnCTL0)
- TAAn control register 1 (TAAnCTL1)
- TAAn I/O control register 0 (TAAmIOC0)
- TAAn I/O control register 1 (TAAmIOC1)
- TAAn I/O control register 2 (TAAmIOC2)
- TAAn I/O control register 4 (TAAmIOC4)
- TAAn option register 0 (TAAmOPT0)
- TAAn option register 1 (TAAmOPT1)
- TAAn capture/compare register 0 (TAAnCCR0)
- TAAn capture/compare register 1 (TAAnCCR1)
- TAAn counter read buffer register (TAAnCNT)
- TAA noise elimination control register (TANFC)

Remarks 1. When using the functions of the TIAAm0, TIAAm1, TOAAm0, and TOAAm1 pins, see **Table 4-20 Using Port Pin as Alternate-Function Pin**.

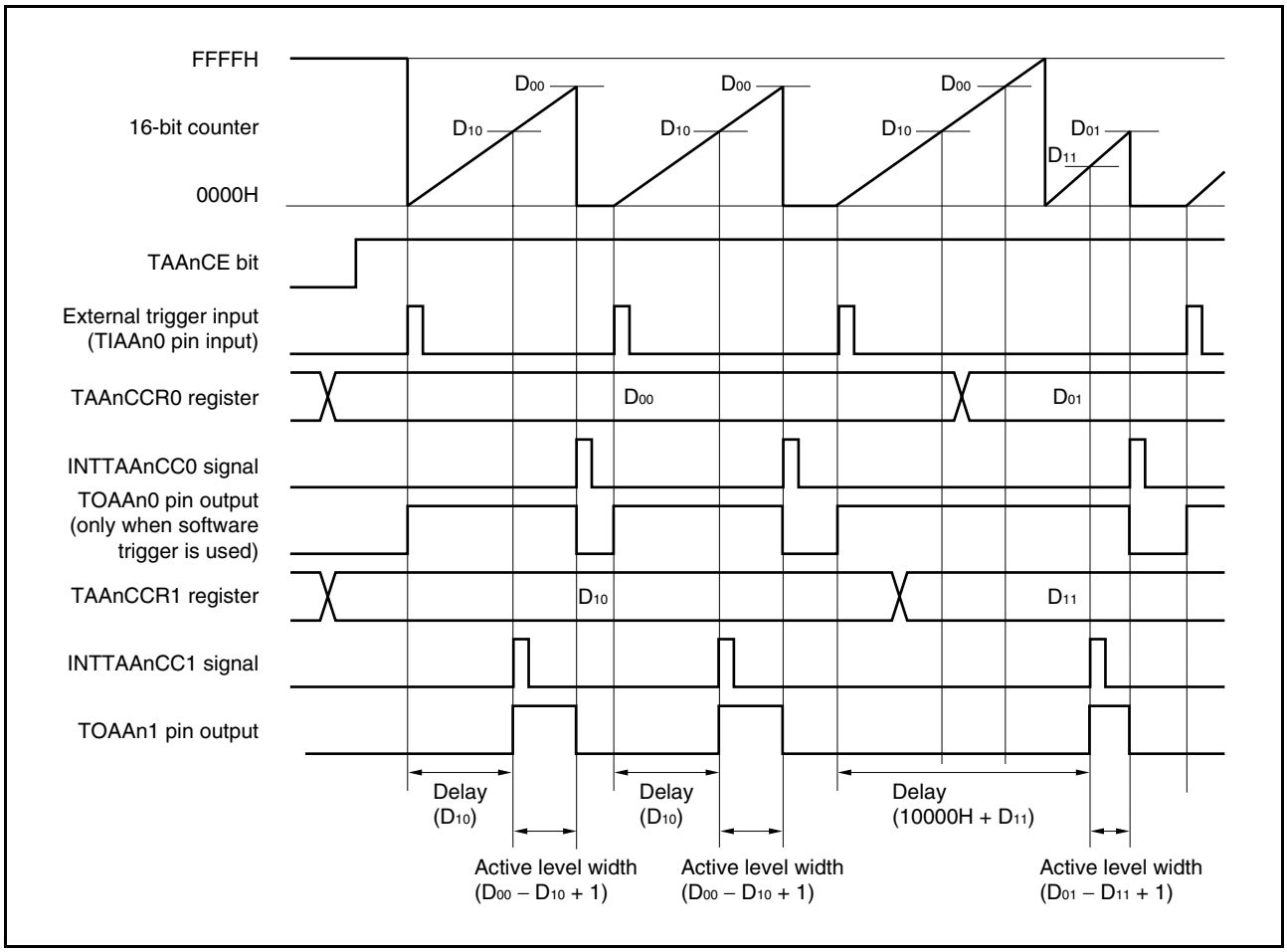
2. n = 0 to 5, m = 0 to 3, 5

(2) Operation timing in one-shot pulse output mode

(a) Note on rewriting TAAnCCRm register

To change the set value of the TAAnCCRm register to a smaller value, stop counting once, and then change the set value.

If the value of the TAAnCCRm register is rewritten to a smaller value during counting, the 16-bit counter may overflow.



When the TAAnCCR0 register is rewritten from D_{00} to D_{01} and the TAAnCCR1 register from D_{10} to D_{11} where $D_{00} > D_{01}$ and $D_{10} > D_{11}$, if the TAAnCCR1 register is rewritten when the count value of the 16-bit counter is greater than D_{11} and less than D_{10} and if the TAAnCCR0 register is rewritten when the count value is greater than D_{01} and less than D_{00}, each set value is reflected as soon as the register has been rewritten and compared with the count value. The counter counts up to FFFFH and then counts up again from 0000H. When the count value matches D_{11}, the counter generates the INTTAAnCC1 signal and asserts the TOAAn1 pin. When the count value matches D_{01}, the counter generates the INTTAAnCC0 signal, deasserts the TOAAn1 pin, and stops counting.

Therefore, the counter may output a pulse with a delay period or active period different from that of the one-shot pulse that is originally expected.

Remark n = 0 to 3, 5
m = 0, 1

7.6.1 Free-running timer mode (during timer-tuned operation)

This section explains the free-running timer mode of the timer-tuned operation. For the combination of timer-tuned operations, see **Table 7-7**. In this section, an example of timer-tuned operation using TAA1 and TAA0 is shown.

(i) Selecting capture/compare registers

When the free-running timer mode of the timer-tuned operation is used with TAA1 and TAA0 connected to each other, the two capture/compare registers of TAA1 and two capture/compare registers of TAA0 can be used in combination.

How the capture and compare registers are combined is not restricted and can be selected by using the TAAnCCSn bit of the master or slave timer. When the compare register is selected, the set value of the compare register can be rewritten during operation and the rewriting method is anytime write (n = 0, 1).

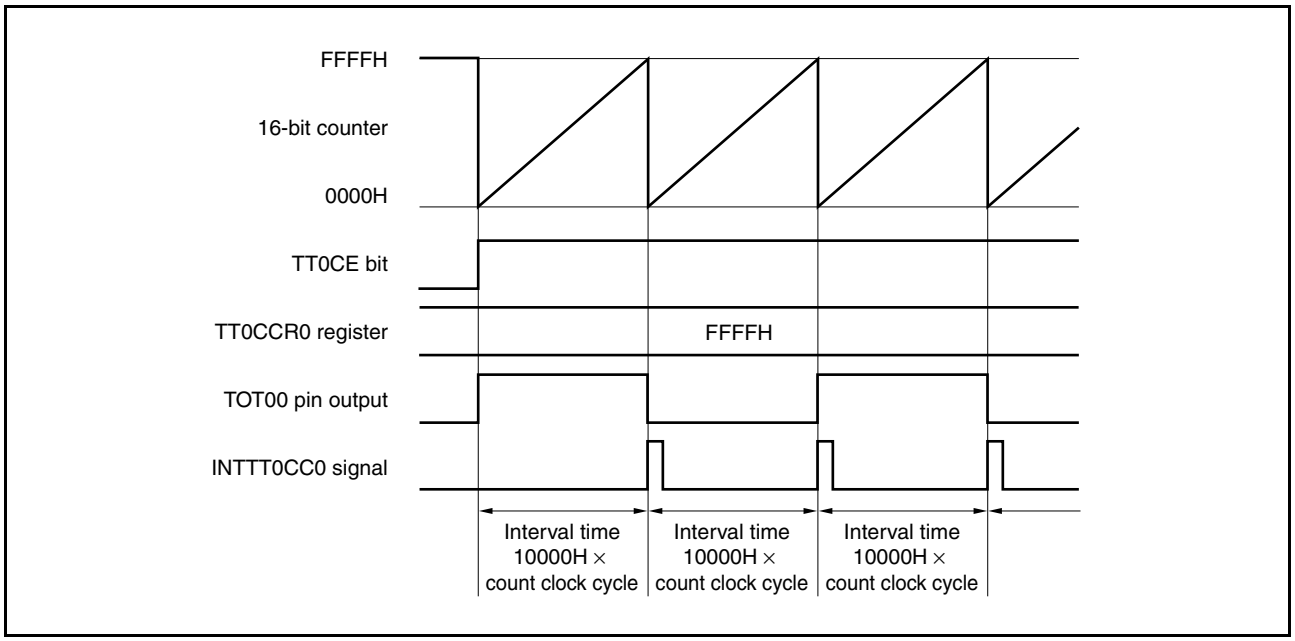
(ii) Overflow

If the counter overflows, an overflow interrupt (INTTAA1OV) of the master timer is generated and the overflow flag (TAA1OVF) is set to “1”.

The overflow interrupt (INTTAA0OV) and overflow flag (TAA0OVF) of the slave timer do not operate and are always at the low level.

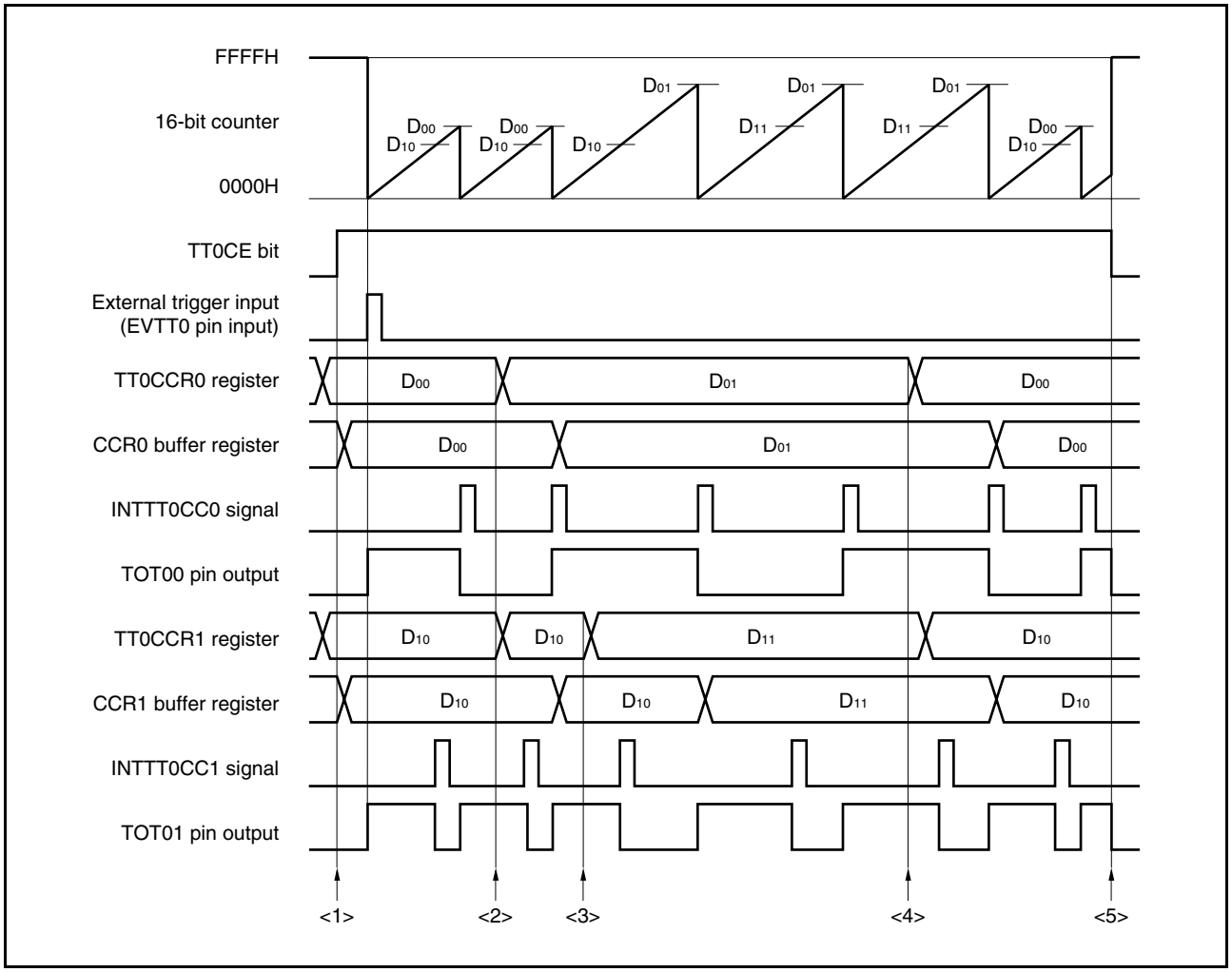
(b) Operation if TT0CCR0 register is set to FFFFH

If the TT0CCR0 register is set to FFFFH, the 16-bit counter counts up to FFFFH. The counter is cleared to 0000H in synchronization with the next count-up timing. The INTTT0CC0 signal is generated and the output of the TOT00 pin is inverted. At this time, an overflow interrupt request signal (INTTT0OV) is not generated, nor is the overflow flag (TT0OPT0.TT0OVF bit) set to 1.



(1) Operation flow in external trigger pulse output mode

Figure 9-24. Software Processing Flow in External Trigger Pulse Output Mode (1/2)



CHAPTER 11 MOTOR CONTROL FUNCTION

11.1 Functional Overview

Timer AB1 (TAB1) and the TMQ0 option (TMQOP0) can be used as an inverter function that controls a motor. It performs a tuning operation with timer AA4 (TAA4) and A/D conversion of the A/D converter can be started when the value of TAB1 matches the value of TAA4. The following operations can be performed as motor control functions.

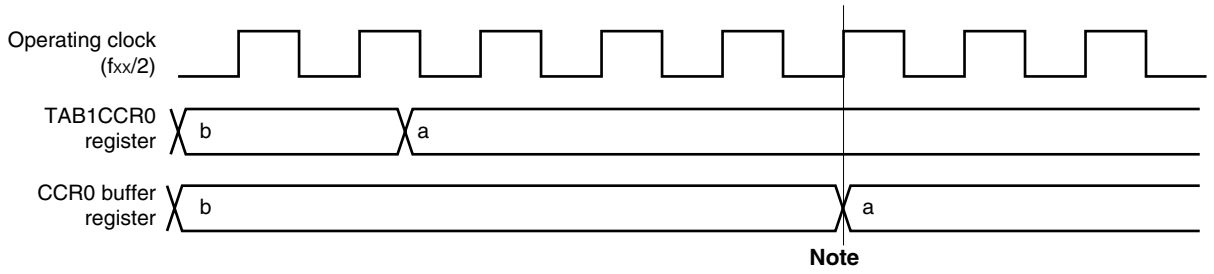
- 6-phase PWM output function with 16-bit accuracy
- Timer tuning operation function (tunable with TAA4)
- Cycle setting function (cycle can be changed during operation of crest or valley interrupt)
- Compare register rewriting: Anytime rewrite, batch rewrite, or intermittent rewrite (selectable during TAB1 operation)
- Interrupt and transfer culling functions
- Dead-time setting function
- A/D trigger timing function of the A/D converter
- 0% output and 100% output available
- 0% output and 100% output selectable by crest interrupt and valley interrupt
- Forcible output stop function
  - When valid edge detected by external pin input (TOAB1OFF, TOAA1OFF)
  - When main clock oscillation stop detected by clock monitor function

(1) Anytime rewrite mode

This mode is set by setting the TAB1OPT0.TAB1CMS bit to 1. The setting of the TAB1OPT2.TAB1RDE bit is ignored.

In this mode, the value written to each register with a transfer function is immediately transferred to an internal buffer register and compared with the value of the counter. If a register with transfer function is rewritten in this mode after the count value of the 16-bit counter matches the value of the TAB1CCRm register, the rewritten value is not reflected because the next match is ignored after the first match has occurred. If the register is rewritten during counting up, the new register value becomes valid after the counter has started counting down.

Figure 11-21. Timing of Reflecting Rewritten Value

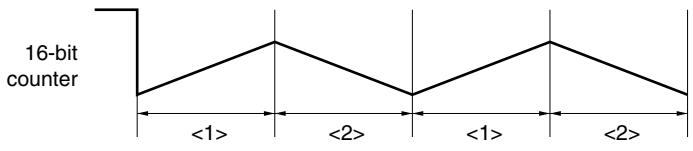


Note After the register (TAB1CCR0, TAB1CCR2, TAB1CCR3, TAB1OPT1, TAA4CCR0, or TAA4CCR1) has been written, the written value is transferred to an internal buffer register after four clocks of the operating clock. However, the value of the TAB1CCR1 register is transferred after 5 clocks.

(a) Rewriting TAB1CCR0 register

Even if the TAB1CCR0 register is rewritten in the anytime rewrite mode, the new value may not be reflected in some cases.

Figure 11-22. Example of Rewriting TAB1CCR0 Register



Rewriting during period <1> (rewriting during counting up)

If the newly rewritten value is greater than the value of the 16-bit counter, there is no problem because it will match the value of the 16-bit counter. If the new value is less than the value of the 16-bit counter, it will not match the value of the counter. As a result, the 16-bit counter overflows and continues counting up from 0000H until it matches the register value again, and the correct PWM waveform is not output.

Rewriting during period <2> (rewriting during counting down)

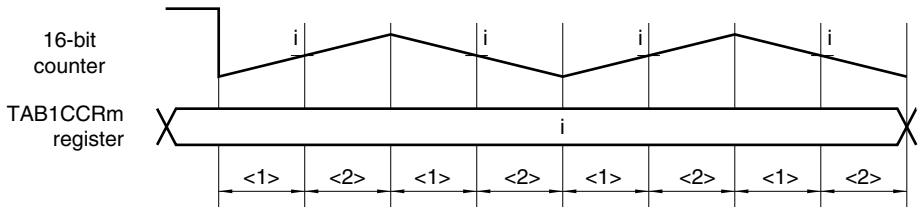
A match with the value of the 16-bit counter is ignored during counting down. Therefore, the rewritten period value is reflected as the match point starting from counting up in the next cycle.

(b) Rewriting TAB1CCRm register

Figure 11-24 shows the timing of rewriting before the value of the 16-bit counter matches the value of the TAB1CCRm register (<1> in Figure 11-23), and Figure 11-25 shows the timing of rewriting after the value of the 16-bit counter matches the value of the TAB1CCRm register (<2> in Figure 11-23).

Figure 11-23. Basic Operation of 16-Bit Counter and TAB1CCRm Register

(a) Basic figure



Remarks 1. i = Set value of TAB1CCRm register

2. m = 1 to 3

(14) Alarm minute setting register (RC1ALM)

The RC1ALM register (8-bit) is used to set minutes of alarm.

This register can be read or written in 8-bit units.

Reset sets this register to 00H.

Caution Set a decimal value of 00 to 59 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

After reset: 00H R/W Address: FFFFFADAH

	7	6	5	4	3	2	1	0
RC1ALM	0							

(15) Alarm hour setting register (RC1ALH)

The RC1ALH register (8-bit) is used to set hours of alarm.

This register can be read or written in 8-bit units.

Reset sets this register to 12H.

Cautions 1. Set a decimal value of 00 to 23, 01 to 12, or 21 to 32 to this register in BCD code. If a value outside the range is set, the alarm is not detected.

2. Bit 5 of the RC1ALH register indicates a.m. (0) or p.m. (1) if the AMPM bit = 0 (12-hour system) is selected.

After reset: 12H R/W Address: FFFFFADBH

	7	6	5	4	3	2	1	0
RC1ALH	0	0						

To set the baud rate, perform the following calculation for setting the UCnCTL1 and UCnCTL2 registers (when using internal clock).

<1> Set k to fxx/2/(2 × target baud rate) and m to 0.
<2> If k is 256 or greater (k ≥ 256), reduce k to half (k/2) and increment m by 1 (m + 1).
<3> Repeat Step <2> until k becomes less than 256 (k < 256).
<4> Round off the first decimal point of k to the nearest whole number.
If k becomes 256 after round-off, perform Step <2> again to set k to 128.
<5> Set the value of m to UCnCTL1 register and the value of k to the UCnCTL2 register.

Example: When fxx = 48 MHz and target baud rate = 153,600 bps
<1> k = 480,000,000/2/(2 × 153,600) = 78.125…, m = 0
<2>, <3> k = 78.125… < 256, m = 0
<4> Set value of UCnCTL2 register: k = 78 = 4EH, set value of UCnCTL1 register: m = 0

Actual baud rate = 48,000,000/2/(2 × 78)
= 153,846 [bps]

Baud rate error = {48,000,000/2/(2 × 78 × 153,600) − 1} × 100
= 0.160 [%]

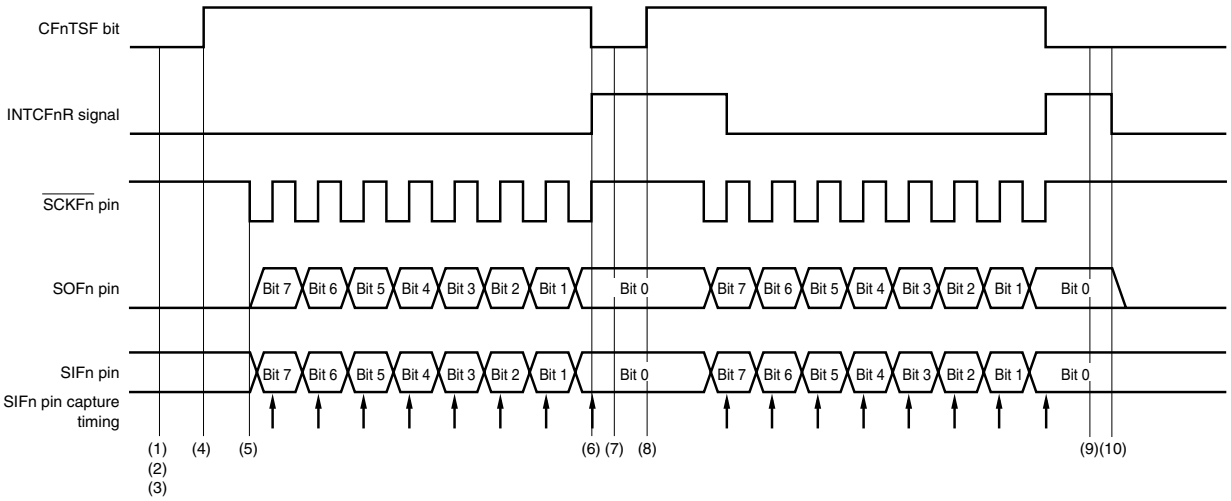
The representative examples of baud rate settings are shown below.

Table 17-4. Baud Rate Generator Setting Data

Baud Rate (bps)	fxx = 48 MHz			fxx = 32 MHz			fxx = 24 MHz		
	UCnCTL1	UCnCTL2	ERR (%)	UCnCTL1	UCnCTL2	ERR (%)	UCnCTL1	UCnCTL2	ERR (%)
300	08H	9CH	0.16	07H	D0H	0.16	07H	9CH	−2.3
600	07H	9CH	0.16	06H	D0H	0.16	06H	9CH	0.16
1,200	06H	9CH	0.16	05H	D0H	0.16	05H	9CH	0.16
2,400	05H	9CH	0.16	04H	D0H	0.16	04H	9CH	0.16
4,800	04H	9CH	0.16	03H	D0H	0.16	03H	9CH	0.16
9,600	03H	9CH	0.16	02H	D0H	0.16	02H	9CH	0.16
19,200	02H	9CH	0.16	01H	D0H	0.16	01H	9CH	0.16
31,250	01H	C0H	0.00	01H	80H	0.00	00H	C0H	0.00
38,400	01H	9CH	0.16	00H	D0H	0.16	00H	9CH	0.16
76,800	00H	9CH	0.16	00H	68H	0.16	00H	4EH	0.16
153,600	00H	4EH	0.16	00H	34H	0.16	00H	27H	0.16
312,500	00H	26H	1.05	00H	1AH	−1.54	00H	13H	1.05
625,000	00H	13H	1.05	00H	0DH	−1.54	00H	0AH	−4.00
1,000,000	00H	0CH	0.00	00H	08H	0.00	00H	06H	0.00
1,250,000	00H	0AH	−4.00	Setting prohibited			00H	05H	−4.00
2,000,000	00H	06H	0.00	00H	04H	0.00	Setting prohibited		
2,500,000	00H	05H	−4.00	Setting prohibited					
3,000,000	00H	04H	0.00						

Remark fxx: Main clock frequency
ERR: Baud rate error (%)

(2) Operation timing



(1) Write 00H to the CFnCTL1 register, and select communication type 1, communication clock (f_{CCLK}) = f_{XX}/2 or f_{XX}/3, and master mode.

(2) Write 00H to the CFnCTL2 register, and set the transfer data length to 8 bits.

(3) Write E1H to the CFnCTL0 register, and select the transmission/reception mode and MSB first at the same time as enabling the operation of the communication clock (f_{CCLK}).

(4) Set the CFnSTR.CFnTSF bit to 1 by writing the transmit data to the CFnTX register, and start transmission/reception.

(5) When transmission/reception is started, output the serial clock to the $\overline{\text{SCKFn}}$ pin, output the transmit data to the SOFn pin in synchronization with the serial clock, and capture the receive data of the SIFn pin.

(6) When transmission/reception of the transfer data length set by the CFnCTL2 register is completed, stop the serial clock output, transmit data output, and data capturing, generate the reception completion interrupt request signal (INTCFnR) at the last edge of the serial clock, and clear the CFnTSF bit to 0.

(7) Read the CFnRX register.

(8) To continue transmission/reception, write the transmit data to the CFnTX register again.

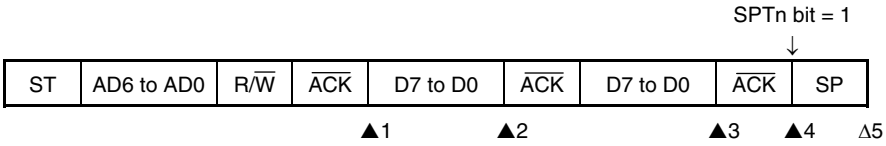
(9) Read the CFnRX register.

(10) To end transmission/reception, write CFnCTL0.CFnPWR bit = 0, CFnCTL0.CFnTXE bit = 0, and CFnCTL0.CFnRXE bit = 0.

Remark n = 0 to 4

(3) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

<1> When WTIMn bit = 0



▲1: IICSn register = 1010X110B

▲2: IICSn register = 1010X000B

▲3: IICSn register = 1010X000B (WTIMn bit = 1)

▲4: IICSn register = 1010XX00B

Δ 5: IICSn register = 00000001B

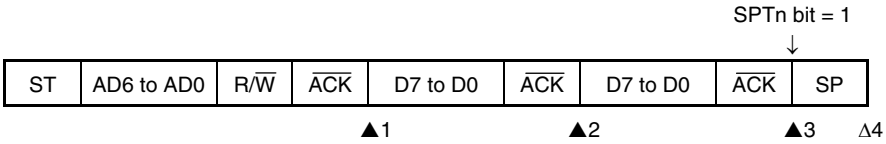
Remarks 1. ▲: Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

2. n = 0 to 2

<2> When WTIMn bit = 1



▲1: IICSn register = 1010X110B

▲2: IICSn register = 1010X100B

▲3: IICSn register = 1010XX00B

Δ 4: IICSn register = 00000001B

Remarks 1. ▲: Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

2. n = 0 to 2

(9/13)

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
00200302H	UF0 configuration/interface/endpoint descriptor register 158	UF0CIE158	R/W		√		Undefined
00200304H	UF0 configuration/interface/endpoint descriptor register 159	UF0CIE159	R/W		√		Undefined
00200306H	UF0 configuration/interface/endpoint descriptor register 160	UF0CIE160	R/W		√		Undefined
00200308H	UF0 configuration/interface/endpoint descriptor register 161	UF0CIE161	R/W		√		Undefined
0020030AH	UF0 configuration/interface/endpoint descriptor register 162	UF0CIE162	R/W		√		Undefined
0020030CH	UF0 configuration/interface/endpoint descriptor register 163	UF0CIE163	R/W		√		Undefined
0020030EH	UF0 configuration/interface/endpoint descriptor register 164	UF0CIE164	R/W		√		Undefined
00200310H	UF0 configuration/interface/endpoint descriptor register 165	UF0CIE165	R/W		√		Undefined
00200312H	UF0 configuration/interface/endpoint descriptor register 166	UF0CIE166	R/W		√		Undefined
00200314H	UF0 configuration/interface/endpoint descriptor register 167	UF0CIE167	R/W		√		Undefined
00200316H	UF0 configuration/interface/endpoint descriptor register 168	UF0CIE168	R/W		√		Undefined
00200318H	UF0 configuration/interface/endpoint descriptor register 169	UF0CIE169	R/W		√		Undefined
0020031AH	UF0 configuration/interface/endpoint descriptor register 170	UF0CIE170	R/W		√		Undefined
0020031CH	UF0 configuration/interface/endpoint descriptor register 171	UF0CIE171	R/W		√		Undefined
0020031EH	UF0 configuration/interface/endpoint descriptor register 172	UF0CIE172	R/W		√		Undefined
00200320H	UF0 configuration/interface/endpoint descriptor register 173	UF0CIE173	R/W		√		Undefined
00200322H	UF0 configuration/interface/endpoint descriptor register 174	UF0CIE174	R/W		√		Undefined
00200324H	UF0 configuration/interface/endpoint descriptor register 175	UF0CIE175	R/W		√		Undefined
00200326H	UF0 configuration/interface/endpoint descriptor register 176	UF0CIE176	R/W		√		Undefined
00200328H	UF0 configuration/interface/endpoint descriptor register 177	UF0CIE177	R/W		√		Undefined
0020032AH	UF0 configuration/interface/endpoint descriptor register 178	UF0CIE178	R/W		√		Undefined
0020032CH	UF0 configuration/interface/endpoint descriptor register 179	UF0CIE179	R/W		√		Undefined

(4) Bridge register

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
00200400H	Bridge interrupt control register	BRGINTT	R/W			√	0000H
00200402H	Bridge interrupt enable register	BRGINTE	R/W			√	0000H
00200404H	EPC macro control register	EPCCLT	R/W			√	0000H
00200408H	CPU I/F bus control register	CPUBCTL	R/W			√	0000H

(5) DMA register

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
00200500H	EP1 DMA control register 1	UF0E1DC1	R/W			√	0000H
00200502H	EP1 DMA control register 2	UF0E1DC2	R/W			√	0000H
00200504H	EP2 DMA control register 1	UF0E2DC1	R/W			√	0000H
00200506H	EP2 DMA control register 2	UF0E2DC2	R/W			√	0000H
00200508H	EP3 DMA control register 1	UF0E3DC1	R/W			√	0000H
0020050AH	EP3 DMA control register 2	UF0E3DC2	R/W			√	0000H
0020050CH	EP4 DMA control register 1	UF0E4DC1	R/W			√	0000H
0020050EH	EP4 DMA control register 2	UF0E4DC2	R/W			√	0000H

(6) Bulk-in register

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
00201000H	UF0 EP1 bulk-in transfer data register	UF0EP1BI	W			√	0000H
00202000H	UF0 EP3 bulk-in transfer data register	UF0EP3BI	W			√	0000H

(7) Bulk-out register

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
00210000H	UF0 EP2 bulk-out transfer data register	UF0EP2BO	R		√	√	0000H
00220000H	UF0 EP4 bulk-out transfer data register	UF0EP4BO	R		√	√	0000H

(8) Peripheral control register

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
00240000H	USBF DMA request enable register	UFDRQEN	R/W		√	√	0000H

(11) UF0 interrupt 1 register (UF0INT1)

The UF0INT1 register is an 8-byte FIFO that stores data for Endpoint7 (to be passed to SIE).

This register is write-only, in 8-bit units. When this register is read, 00H is read.

The hardware transmits data to the USB bus in synchronization with the IN token for Endpoint7 only when the IT1NK bit of the UF0EN register is set to 1 (when NAK is not transmitted). When the data is transmitted and the host correctly receives it, the IT1NK bit of the UF0EN register is automatically cleared to 0 by hardware. A short packet is transmitted when data is written to the UF0INT1 register and the IT1DEND bit of the UF0DEND register is set to 1 (IT1 bit of the UF0EPS0 register = 1 (data exists)). A Null packet is transmitted when the UF0INT1 register is cleared and the IT1DEND bit of the UF0DEND register is set to 1 (IT1 bit of the UF0EPS0 register = 1 (data exists)).

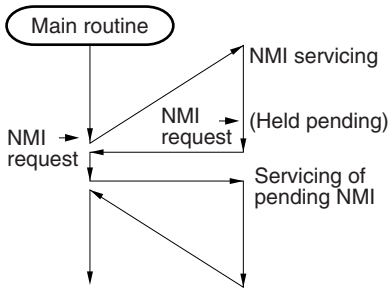
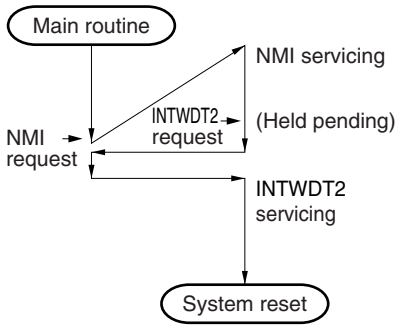
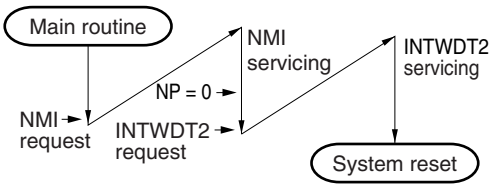
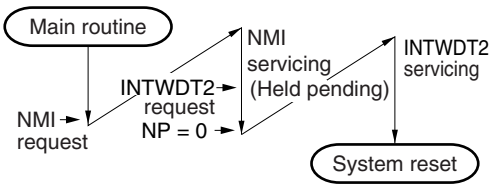
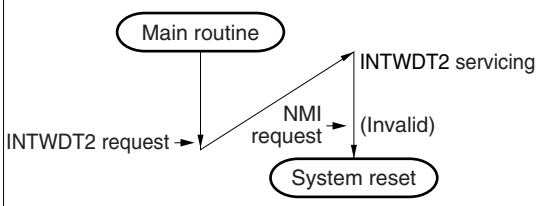
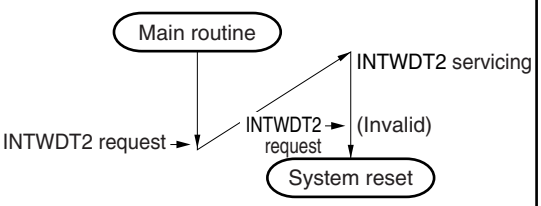
	7	6	5	4	3	2	1	0	Address	After reset
UF0INT1	IT17	IT16	IT15	IT14	IT13	IT12	IT11	IT10	00200114H	Undefined

Bit position	Bit name	Function
7 to 0	IT17 to IT10	These bits store data for Endpoint7.

The operation of the UF0INT1 register is illustrated below.

Figure 23-1. Non-Maskable Interrupt Request Signal Acknowledgment Operation (2/2)

(b) Non-maskable interrupt request signal generated during non-maskable interrupt servicing

Non-maskable interrupt being serviced	Non-maskable interrupt request signal generated during non-maskable interrupt servicing	
	NMI	INTWDT2
NMI	• NMI request generated during NMI servicing 	• INTWDT2 request generated during NMI servicing (NP bit = 1 retained before INTWDT2 request)  • INTWDT2 request generated during NMI servicing (NP bit = 0 set before INTWDT2 request)  • INTWDT2 request generated during NMI servicing (NP = 0 set after INTWDT2 request) 
INTWDT2	• NMI request generated during INTWDT2 servicing 	• INTWDT2 request generated during INTWDT2 servicing 

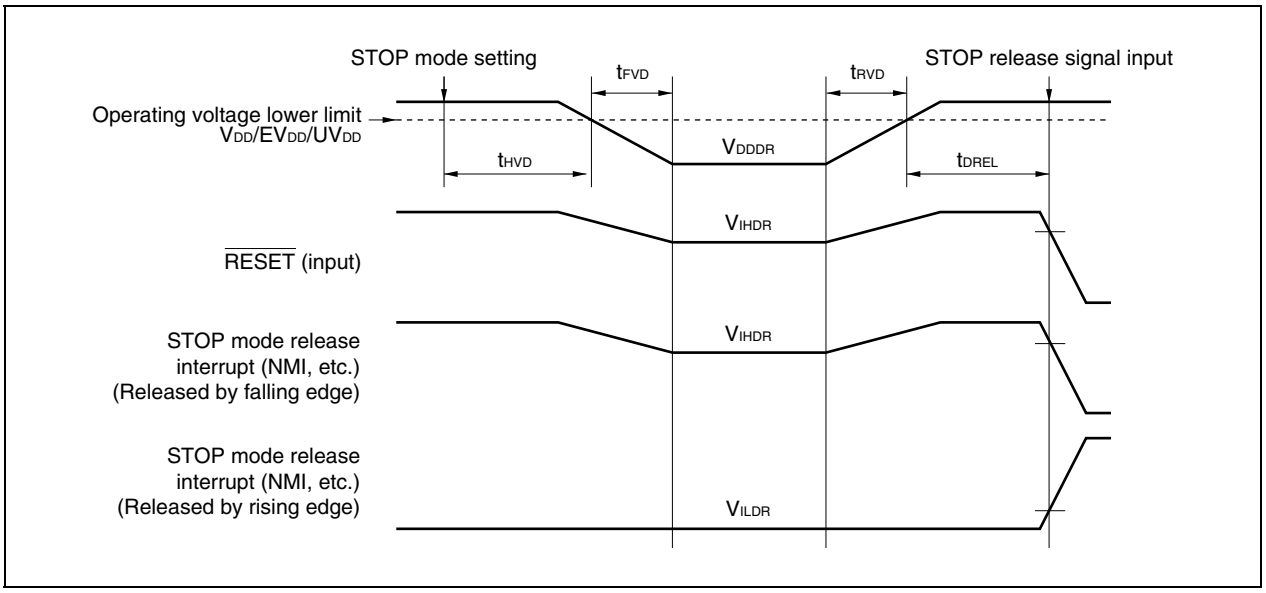
33.6 Data Retention Characteristics

(1) In STOP mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = UV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode (all functions stopped)	1.9		3.6	V
Data retention current	I_{DDDR}	STOP mode (all functions stopped), V_{DDDR} = 2.0 V		10	90	μA
Supply voltage rise time	t_{RVD}		200			μs
Supply voltage fall time	t_{FVD}		200			μs
Supply voltage retention time	t_{HVD}	After STOP mode setting	0			ms
STOP release signal input time	t_{DREL}	After V_{DD} reaches 2.85 V (MIN.)	0			ms
Data retention input voltage, high	V_{IHDR}	V_{DD} = EV_{DD} = UV_{DD} = V_{DDDR}	0.9V_{DDDR}		V_{DDDR}	V
Data retention input voltage, low	V_{ILDR}	V_{DD} = EV_{DD} = UV_{DD} = V_{DDDR}	0		0.1V_{DDDR}	V

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.



<5> QB-V850ESJX3H[Note] In-circuit emulator	The in-circuit emulator serves to debug hardware and software when developing application systems using the V850ES/JG3-H or V850ES/JH3-H. It supports the integrated debugger ID850QB. This emulator should be used in combination with a power supply unit and emulation probe. Use the USB interface cable to connect this emulator to the host machine.
<3> USB interface cable	Cable to connect the host machine and the QB-V850ESJX3H.
<4> AC adapter	100 to 240 V can be supported by replacing the AC plug.
<9> QB-100GC-EA-04S QB-128GF-EA-01S QB-100GC-EA-05T QB-128GF-EA-02T Exchange adapter	Adapter to perform pin conversion. • QB-100GC-EA-04S: 100-pin plastic LQFP (GC-UEU type) • QB-128GF-EA-01S: 128-pin plastic LQFP (GF-GAT type) • QB-100GC-EA-05T: 100-pin plastic LQFP (GC-UEU type) • QB-128GF-EA-02T: 128-pin plastic LQFP (GC-GAT type)
<10> QB-100-CA-01S QB-128-CA-01S (S type only) Check pin adapter	Adapter used in waveform monitoring using the oscilloscope, etc. • QB-100-CA-01S: 100-pin plastic LQFP (GC-UEU type) • QB-128-CA-01S: 128-pin plastic LQFP (GF-GAT type)
<11> QB-100-SA-01S QB-144-SA-01S QB-100GC-YS-01T QB-128GF-YS-01T Space adapter	Adapter to adjust the height. • QB-100-SA-01S: 100-pin plastic LQFP (GC-UEU type) • QB-144-SA-01S: 128-pin plastic LQFP (GF-GAT type) • QB-100GC-YS-01T: 100-pin plastic LQFP (GC-UEU type) • QB-128GF-YS-01T: 128-pin plastic LQFP (GF-GAT type)
<12> QB-100GC-YQ-01T QB-128GF-YQ-01T (T type only) YQ connector	Conversion adapter to connect target connector and exchange adapter • QB-100GC-YQ-01T: 100-pin plastic LQFP (GC-UEU type) • QB-128GF-YQ-01T: 128-pin plastic LQFP (GF-GAT type)
<13> QB-100GC-MA-01S QB-128GF-MA-01S QB-100GC-HQ-01T QB-128GF-HQ-01T Mount adapter	Adapter to mount the V850ES/JG3-H or V850ES/JH3-H on a socket. • QB-100GC-MA-01S: 100-pin plastic LQFP (GC-UEU type) • QB-128GF-MA-01S: 128-pin plastic LQFP (GF-GAT type) • QB-100GC-HQ-01T: 100-pin plastic LQFP (GC-UEU type) • QB-128GF-HQ-01T: 128-pin plastic LQFP (GF-GAT type)
<14> QB-100GC-TC-01S QB-128GF-TC-01S QB-100GC-NQ-01T QB-128GF-NQ-01T Target connector	Connector to solder on the target system. • QB-100GC-TC-01S: 100-pin plastic LQFP (GC-UEU type) • QB-128GF-TC-01S: 128-pin plastic LQFP (GF-GAT type) • QB-100GC-NQ-01T: 100-pin plastic LQFP (GC-UEU type) • QB-128GF-NQ-01T: 128-pin plastic LQFP (GF-GAT type)

Note The QB-V850ESJX3H is supplied with a power supply unit, USB interface cable, and flash memory programmer (MINICUBE2). It is also supplied with integrated debugger ID850QB as control software.

Remark The numbers in the angle brackets correspond to the numbers in Figure A-2.