Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564l54l3bcfqr

Table 1. SPC56ELx/SPC564Lx device summary (continued)

Feature		SPC56EL60	SPC56EL54
Modules	Interrupt Controller (INTC)	16 interrupt levels, replicated module	
	Periodic Interrupt Timer (PIT)	1 × 4 channels	
	System Timer Module (STM)	1 × 4 channels, replicated module	
	Software Watchdog Timer (SWT)	Yes, replicated module	
	eDMA	16 channels, replicated module	
	FlexRay	1 × 64 message buffers, dual channel	
	FlexCAN	2 × 32 message buffers	
	LINFlexD (UART and LIN with DMA support)	2	
	Clock out	Yes	
	Fault Collection and Control Unit (FCCU)	Yes	
	Cross Triggering Unit (CTU)	Yes	
	eTimer	3 × 6 channels(1)	
	FlexPWM	2 Module 4 × (2 + 1) channels(2)	
	Analog-to-Digital Converter (ADC)	2 × 12-bit ADC, 16 channels per ADC (3 internal, 4 shared and 9 external)	
	Sine Wave Generator (SWG)	32 point	
Modules (cont.)	Deserial Serial Peripheral Interface (DSPI)	3 × DSPI as many as 8 chip selects	
	Cyclic Redundancy Checker (CRC) unit	Yes	
	Junction temperature sensor (TSENS)	Yes, replicated module	
	Digital I/Os	≥ 16	
Supply	Device power supply	3.3 V with integrated bypassable ballast transistor External ballast transistor not needed for bare die	
	Analog reference voltage	3.0 V – 3.6 V and 4.5 V – 5.5 V	
Clocking	Frequency-modulated phase-locked loop (FMPLL)	2	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4 – 40 MHz	
Debug	Nexus	Level 3+	
Packages	LQFP	100 pins 144 pins	
	LBGA(3)	LBGA257	

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the FMPLL
- RC oscillator is used as the default system clock during startup and can be used as back-up input source of FMPLL(s) in case XOSC fails

1.5.17 Clock, reset, power, mode and test control modules (MC_CGM, MC_RGM, MC_PCU, and MC_ME)

These modules provide the following:

- Clock gating and clock distribution control
- Halt, stop mode control
- Flexible configurable system and auxiliary clock dividers
- Various execution modes
  - HALT and STOP mode as reduced activity low power mode
  - Reset, Idle, Test, Safe
  - Various RUN modes with software selectable powered modules
  - No stand-by mode implemented (no internal switchable power domains)

1.5.18 Periodic Interrupt Timer Module (PIT)

The PIT module implements the following features:

- 4 general purpose interrupt timers
- 32-bit counter resolution
- Can be used for software tick or DMA trigger operation

1.5.19 System Timer Module (STM)

The STM implements the following features:

- Up-counter with 4 output compare registers
- OS task protection and hardware tick implementation per AUTOSAR[(a)] requirement

The STM is replicated for each processor.

1.5.20 Software Watchdog Timer (SWT)

This module implements the following features:

- Fault tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation
- Allows a high level of safety (SIL3 monitor)

a. Automotive Open System Architecture.

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
C9	I[0]	SIUL	GPIO[128]	GPIO[128]
		eTimer_2	ETC[0]	ETC[0]
		DSPI_0	CS4	—
		FlexPWM_1	—	FAULT[0]
C10	JCOMP	—	—	JCOMP
C11	H[11]	SIUL	GPIO[123]	GPIO[123]
		FlexPWM_1	A[2]	A[2]
C12	I[1]	SIUL	GPIO[129]	GPIO[129]
		eTimer_2	ETC[1]	ETC[1]
		DSPI_0	CS5	—
		FlexPWM_1	—	FAULT[1]
C13	F[14]	SIUL	GPIO[94]	GPIO[94]
		LINFlexD_1	TXD	—
C14	B[1]	SIUL	GPIO[17]	GPIO[17]
		eTimer_1	ETC[3]	ETC[3]
		SSCM	DEBUG[1]	—
		FlexCAN_0	—	RXD
		FlexCAN_1	—	RXD
		SIUL	—	EIRQ[16]
C15	$V_{SS\_HV\_IO\_RING}$	—		
C16	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]
C17	F[12]	SIUL	GPIO[92]	GPIO[92]
		eTimer_1	ETC[3]	ETC[3]
		SIUL	—	EIRQ[30]
D1	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
D2	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
G14	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
G15	H[13]	SIUL	GPIO[125]	GPIO[125]
		FlexPWM_1	X[3]	X[3]
		eTimer_2	ETC[3]	ETC[3]
G16	H[9]	SIUL	GPIO[121]	GPIO[121]
		FlexPWM_1	B[1]	B[1]
		DSPI_0	CS7	—
G17	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
H1	G[13]	SIUL	GPIO[109]	GPIO[109]
		NPC	MDO[10]	—
H2	$V_{SS\_HV\_IO\_RING}$	—		
H3	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
H4	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
H6	V_{DD_LV}	—		
H7	V_{SS_LV}	—		
H8	V_{SS_LV}	—		
H9	V_{SS_LV}	—		
H10	V_{SS_LV}	—		
H11	V_{SS_LV}	—		
H12	V_{DD_LV}	—		
H14	V_{SS_LV}	—		
H15	$V_{DD\_HV\_REG\_1}$	—		
H16	$V_{DD\_HV\_FLA}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
R12	C[0]	SIUL	—	GPIO[32]
		ADC_1	—	AN[3]
R13	BCTRL	—		
R14	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
R15	$V_{SS\_HV\_IO\_RING}$	—		
R16	D[11]	SIUL	GPIO[59]	GPIO[59]
		FlexPWM_0	B[0]	B[0]
		eTimer_0	—	ETC[1]
R17	G[9]	SIUL	GPIO[105]	GPIO[105]
		FlexRay	DBG1	—
		DSPI_1	CS1	—
		FlexPWM_0	—	FAULT[1]
		SIUL	—	EIRQ[29]
T1	$V_{SS\_HV\_IO\_RING}$	—		
T2	$V_{DD\_HV\_IO\_RING}$	—		
T3	Not connected	—		
T4	C[1]	SIUL	—	GPIO[33]
		ADC_0	—	AN[2]
T5	E[5]	SIUL	—	GPIO[69]
		ADC_0	—	AN[8]
T6	E[7]	SIUL	—	GPIO[71]
		ADC_0	—	AN[6]
T7	$V_{SS\_HV\_ADR0}$	—		
T8	B[11]	SIUL	—	GPIO[27]
		ADC_0 ADC_1	—	AN[13]
T9	$V_{SS\_HV\_ADR1}$	—		
T10	E[9]	SIUL	—	GPIO[73]
		ADC_1	—	AN[7]
T11	E[10]	SIUL	—	GPIO[74]
		ADC_1	—	AN[8]

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
B[13]	PCR[29]	SIUL	—	ALT0	GPI[29]	—	—	—	—	43	60	R10
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=0						
		ADC_1	—	—	AN[0](3)	—						
B[14]	PCR[30]	SIUL	—	ALT0	GPI[30]	—	—	—	—	44	64	P11
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=2						
		SIUL	—	—	EIRQ[19]	—						
		ADC_1	—	—	AN[1](3)	—						
B[15]	PCR[31]	SIUL	—	ALT0	GPI[31]	—	—	—	—	—	62	R11
		SIUL	—	—	EIRQ[20]	—						
		ADC_1	—	—	AN[2](3)	—						
Port C												
C[0]	PCR[32]	SIUL	—	ALT0	GPI[32]	—	—	—	—	45	66	R12
		ADC_1	—	—	AN[3](3)	—						
C[1]	PCR[33]	SIUL	—	ALT0	GPI[33]	—	—	—	—	—	41	T4
		ADC_0	—	—	AN[2](3)	—						
C[2]	PCR[34]	SIUL	—	ALT0	GPI[34]	—	—	—	—	—	45	U5
		ADC_0	—	—	AN[3](3)	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
C[15]	PCR[47]	SIUL	GPIO[47]	ALT0	GPIO[47]	—	—	SYM	S	85	124	A8
		FlexRay	CA_TR_EN	ALT1	—	—						
		eTimer_1	ETC[0]	ALT2	ETC[0]	PSMI[9]; PADSEL=1						
		FlexPWM_0	A[1]	ALT3	A[1]	PSMI[21]; PADSEL=1						
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=1						
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=1						
Port D												
D[0]	PCR[48]	SIUL	GPIO[48]	ALT0	GPIO[48]	—	—	SYM	S	86	125	B8
		FlexRay	CA_TX	ALT1	—	—						
		eTimer_1	ETC[1]	ALT2	ETC[1]	PSMI[10]; PADSEL=1						
		FlexPWM_0	B[1]	ALT3	B[1]	PSMI[25]; PADSEL=1						
D[1]	PCR[49]	SIUL	GPIO[49]	ALT0	GPIO[49]	—	—	M	S	3	3	E3
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=2						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexRay	—	—	CA_RX	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
E[14]	PCR[78]	SIUL	GPIO[78]	ALT0	GPIO[78]	—	—	M	S	—	119	B12
		eTimer_1	ETC[5]	ALT1	ETC[5]	PSMI[14]; PADSEL=3						
		SIUL	—	—	EIRQ[26]	—						
E[15]	PCR[79]	SIUL	GPIO[79]	ALT0	GPIO[79]	—	—	M	S	—	121	B11
		DSPI_0	CS1	ALT1	—	—						
		SIUL	—	—	EIRQ[27]	—						
Port F												
F[0]	PCR[80]	SIUL	GPIO[80]	ALT0	GPIO[80]	—	—	M	S	—	133	D7
		FlexPWM_0	A[1]	ALT1	A[1]	PSMI[21]; PADSEL=2						
		eTimer_0	—	—	ETC[2]	PSMI[37]; PADSEL=1						
		SIUL	—	—	EIRQ[28]	—						
F[3]	PCR[83]	SIUL	GPIO[83]	ALT0	GPIO[83]	—	—	M	S	—	139	B5
		DSPI_0	CS6	ALT1	—	—						
F[4]	PCR[84]	SIUL	GPIO[84]	ALT0	GPIO[84]	—	—	F	S	—	4	D2
		NPC	MDO[3]	ALT2	—	—						
F[5]	PCR[85]	SIUL	GPIO[85]	ALT0	GPIO[85]	—	—	F	S	—	5	D1
		NPC	MDO[2]	ALT2	—	—						
F[6]	PCR[86]	SIUL	GPIO[86]	ALT0	GPIO[86]	—	—	F	S	—	8	E2
		NPC	MDO[1]	ALT2	—	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
G[6]	PCR[102]	SIUL	GPIO[102]	ALT0	GPIO[102]	—	—	M	S	—	98	G17
		FlexPWM_0	A[3]	ALT1	A[3]	PSMI[23]; PADSEL=3						
G[7]	PCR[103]	SIUL	GPIO[103]	ALT0	GPIO[103]		—	M	S	—	83	P17
		FlexPWM_0	B[3]	ALT1	B[3]	PSMI[27]; PADSEL=3						
G[8]	PCR[104]	SIUL	GPIO[104]	ALT0	GPIO[104]	—	—	M	S	—	81	P16
		FlexRay	DBG0	ALT1	—	—						
		DSPI_0	CS1	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=2						
		SIUL	—	—	EIRQ[21]	—						
G[9]	PCR[105]	SIUL	GPIO[105]	ALT0	GPIO[105]	—	—	M	S	—	79	R17
		FlexRay	DBG1	ALT1	—	—						
		DSPI_1	CS1	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=2						
		SIUL	—	—	EIRQ[29]	—						
G[10]	PCR[106]	SIUL	GPIO[106]	ALT0	GPIO[106]	—	—	M	S	—	77	P15
		FlexRay	DBG2	ALT1	—	—						
		DSPI_2	CS3	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=1						

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 120 MHz. The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

The “Symbol” column of the electrical parameter and timings tables contains an additional column containing “SR”, “CC”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the input voltage of a voltage regulator.
- “CC” identifies controller characteristics—indicating the characteristics and timing of the signals that the chip provides.
- “P”, “C”, “T”, or “D” apply only to controller characteristics—specifications that define normal device operation. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Min	Max	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	–0.3	4.5(2), (3)	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	–0.3	4.5 (2), (3)	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	–0.3	4.5 (2), (3)	V
$V_{SS\_HV\_FLA}$	SR	Flash memory ground	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	–0.3	4.5 (2), (3)	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADR0}$ (2)(3) $V_{DD\_HV\_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	–0.3	6.4 (2)	V

3.5 Thermal characteristics

Table 12. Thermal characteristics for LQFP100 package(1)

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance, junction-to-ambient natural convection(2)	Single layer board – 1s	46	°C/W
			Four layer board – 2s2p	34	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	36	°C/W
			Four layer board – 2s2p	28	
$R_{\theta JB}$	D	Thermal resistance junction-to-board(3)	—	19	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case(4)	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection(5)	—	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 13. Thermal characteristics for LQFP144 package(1)

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance, junction-to-ambient natural convection(2)	Single layer board – 1s	44	°C/W
			Four layer board – 2s2p	36	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	35	°C/W
			Four layer board – 2s2p	30	
$R_{\theta JB}$	D	Thermal resistance junction-to-board(3)	—	24	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case(4)	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection(5)	—	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 17. ESD ratings[1], [2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production.

3.8 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 18. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	SR	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.9 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator HPREG1 (internal ballast to support core current)
- High power regulator HPREG2 (external NPN to support core current)
- Low voltage detector (LVD_MAIN_1) for 3.3 V supply to IO (V_{DDIO})
- Low voltage detector (LVD_MAIN_2) for 3.3 V supply (V_{DDREG})
- Low voltage detector (LVD_MAIN_3) for 3.3 V flash supply ($V_{DDFLASH}$)
- Low voltage detector (LVD_DIG_MAIN) for 1.2 V digital core supply (HPV_{DD})
- Low voltage detector (LVD_DIG_BKUP) for the self-test of LVD_DIG_MAIN
- High voltage detector (HVD_DIG_MAIN) for 1.2 V digital CORE supply (HPV_{DD})
- High voltage detector (HVD_DIG_BKUP) for the self-test of HVD_DIG_MAIN.
- Power on Reset (POR)

HPREG1 uses an internal ballast to support the core current. HPREG2 is used only when external NPN transistor is present on board to supply core current. The SPC56XL60/54 always powers up using HPREG1 if an external NPN transistor is present. Then the

3.18 SWG electrical characteristics

Table 31. SPC56XL60/54 SWG Specifications

Symbol	Parameter	Value		
		Minimum	Typical	Maximum
T	Input clock	12 MHz	16 MHz	20 MHz
T	Frequency Range	1 kHz	—	50 kHz
T	Peak to Peak(1)	0.4 V	—	2.0V
T	Peak to Peak variation(2)	-6%	—	6%
T	Common Mode(3)	—	1.3 V	—
T	Common Mode variation	-6%	—	6%
T	SiNAD(4)	45 dB	—	—
T	Load C	25 pF	—	100 pF
T	Load I	0 µA	—	100 µA
T	ESD Pad Resistance(5)	230 Ω	—	360 Ω

1. Peak to Peak value is measured with no R or I load.
2. Peak to Peak excludes noise, SiNAD must be considered.
3. Common mode value is measured with no R or I load.
4. SiNAD is measured at Max Peak to Peak voltage.
5. Internal device routing resistance. ESD pad resistance is in series and must be considered for max Peak to Peak voltages, depending on application I load and/or R load.

3.19 AC specifications

3.19.1 Pad AC specifications

Table 32. Pad AC specifications (3.3 V, IPP_HVE = 0)(1)

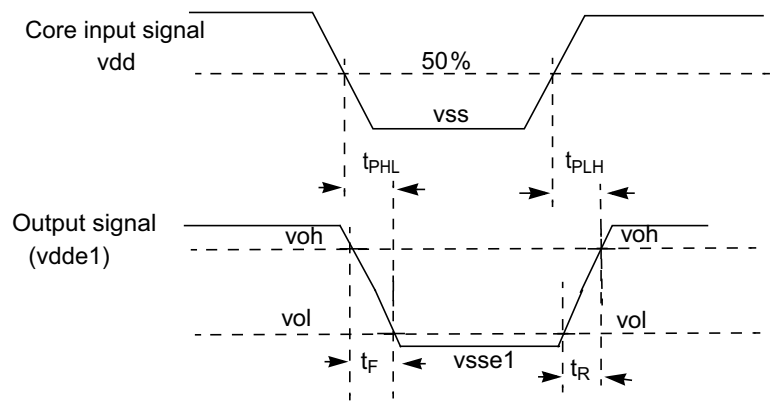
No.	Pad		Tswitchon(1)(ns)			Rise/Fall(2) (ns)			Frequency (MHz)			Current slew(3) (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	T	3	—	40	—	—	40	—	—	4	0.01	—	2	25
			3	—	40	—	—	50	—	—	2	0.01	—	2	50
			3	—	40	—	—	75	—	—	2	0.01	—	2	100
			3	—	40	—	—	100	—	—	2	0.01	—	2	200
2	Medium	T	1	—	15	—	—	12	—	—	40	2.5	—	7	25
			1	—	15	—	—	25	—	—	20	2.5	—	7	50
			1	—	15	—	—	40	—	—	13	2.5	—	7	100
			1	—	15	—	—	70	—	—	7	2.5	—	7	200

Table 32. Pad AC specifications (3.3 V, IPP_HVE = 0)(1) (continued)

No.	Pad		Tswitchon(1)(ns)			Rise/Fall(2) (ns)			Frequency (MHz)			Current slew(3) (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
3	Fast	T	1	—	6	—	—	4	—	—	72	3	—	40	25
			1	—	6	—	—	7	—	—	55	7	—	40	50
			1	—	6	—	—	12	—	—	40	7	—	40	100
			1	—	6	—	—	18	—	—	25	7	—	40	200
4	Symmetric	T	1	—	8	—	—	5	—	—	50	3	—	25	25

1. Propagation delay from $V_{DD\_HV\_IOx}/2$ of internal signal to Pchannel/Nchannel switch-on condition (i.e. t_PHL and t_PLH in *Figure 13: Pad output delay*).
2. Slope at rising/falling edge (i.e. t_F and t_R in *Figure 13: Pad output delay*).
3. Data based on characterization results, not tested in production.

Figure 13. Pad output delay



[1] t_F and t_R are transient times at the FAR END.
[2] t_{PHL} and t_{PLH} are measured at the pad.
[3] Core input slew = 1ns (0 to vdd).

3.20 Reset sequence

This section shows the duration for different reset sequences. It describes the different reset sequences and it specifies the start conditions and the end indication for the reset sequences.

3.20.1 Reset sequence duration

Table 33 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in *Section 3.20.2*.

Table 33. RESET sequences

No.	Symbol		Parameter	Conditions	T_{Reset}			Unit
					Min	Typ	Max(1)	
1	T_{DRB}	CC	Destructive Reset Sequence, BIST enabled		28	34	39	ms
2	T_{DR}	CC	Destructive Reset Sequence, BIST disabled	—	500	4200	5000	µs
3	T_{ERLB}	CC	External Reset Sequence Long, BIST enabled		28	32	37	ms
4	T_{FRL}	CC	Functional Reset Sequence Long	—	35	150	400	µs
5	T_{FRS}	CC	Functional Reset Sequence Short	—	1	4	10	µs

1. The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of $\overline{\text{RESET}}$ by an external reset generator.

3.20.2 Reset sequence description

The figures in this section show the internal states of the chip during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in *Table 33*. The start point and end point conditions as well as the reset trigger mapping to the different reset sequences are specified in *Section 3.20.3*.

With the beginning of DRUN mode the first instruction is fetched and executed. At this point application execution starts and the internal reset sequence is finished.

The figures below show the internal states of the chip during the execution of the reset sequence and the possible states of the signal pin $\overline{\text{RESET}}$.

Note: $\overline{\text{RESET}}$ is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the chip internal reset circuitry. A high level on this pin can only be generated by an external pull up resistor which is strong enough to overdrive the weak internal pull down resistor. The rising edge on $\overline{\text{RESET}}$ in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in table Table 33 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping $\overline{\text{RESET}}$ asserted low beyond the last PHASE3.

Figure 14. Destructive Reset Sequence, BIST enabled

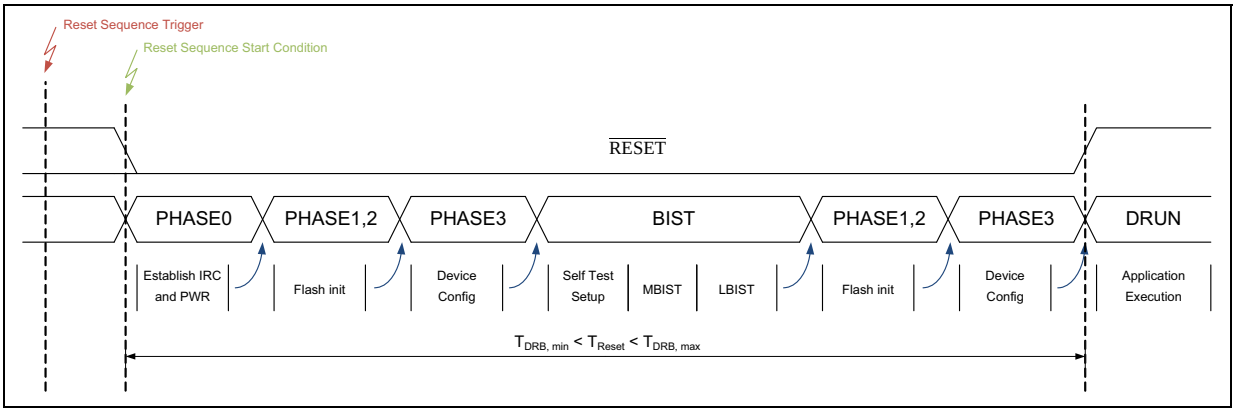


Figure 15. Destructive Reset Sequence, BIST disabled

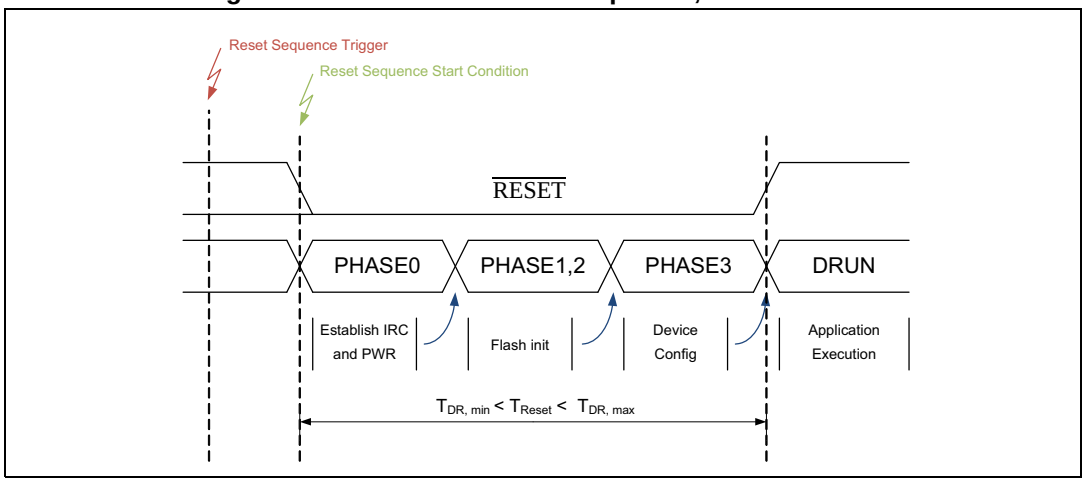


Figure 16. External Reset Sequence Long, BIST enabled

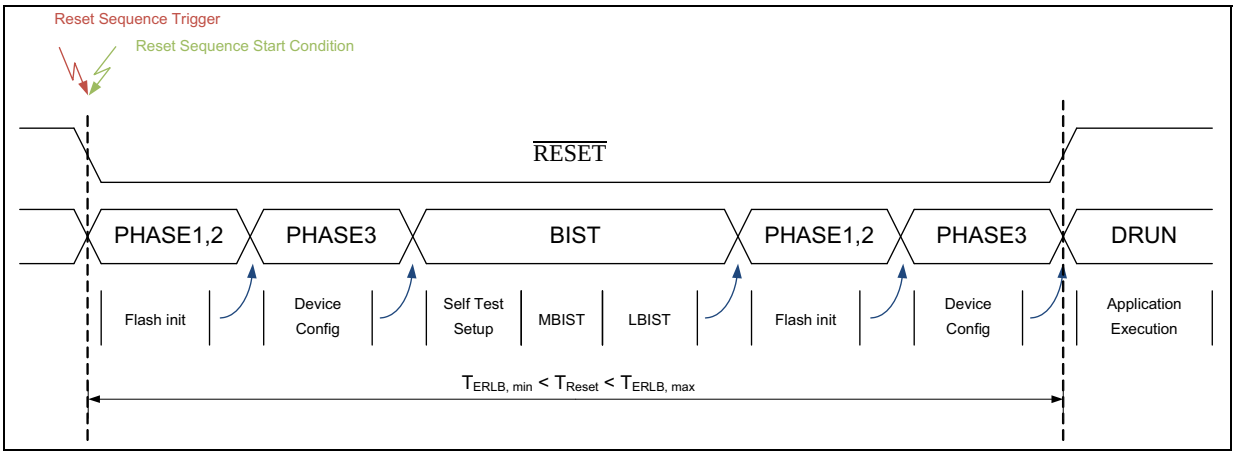


Figure 17. Functional Reset Sequence Long

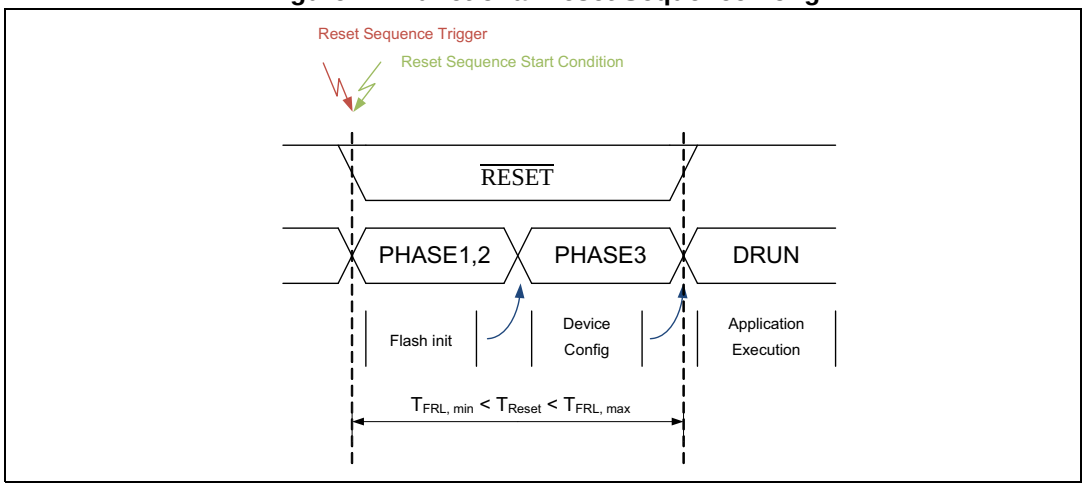


Figure 22. Start-up reset requirements

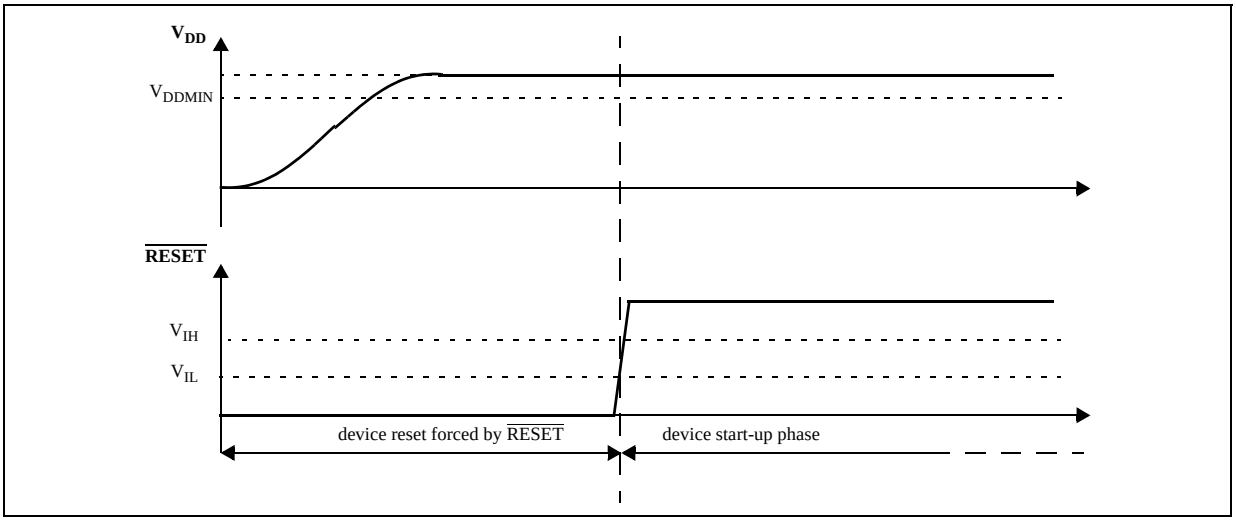


Figure 23. Noise filtering on reset signal

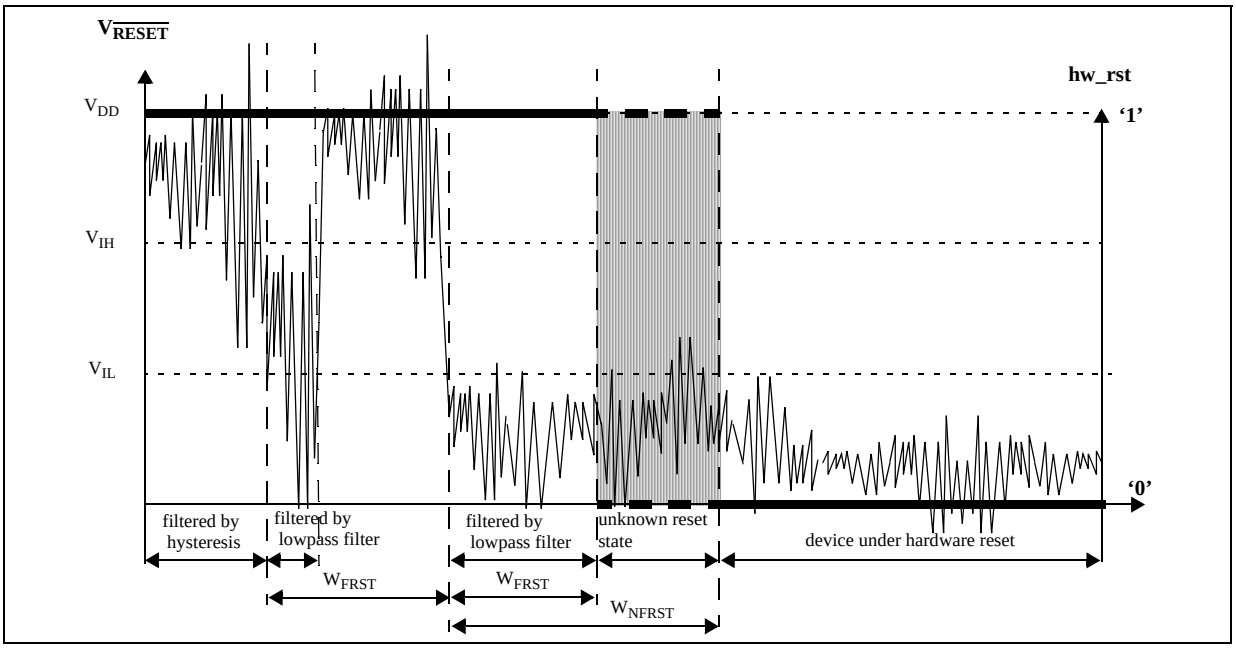


Table 36. RESET electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	nRESET input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	nRESET input not filtered pulse	—	500	—	—	ns

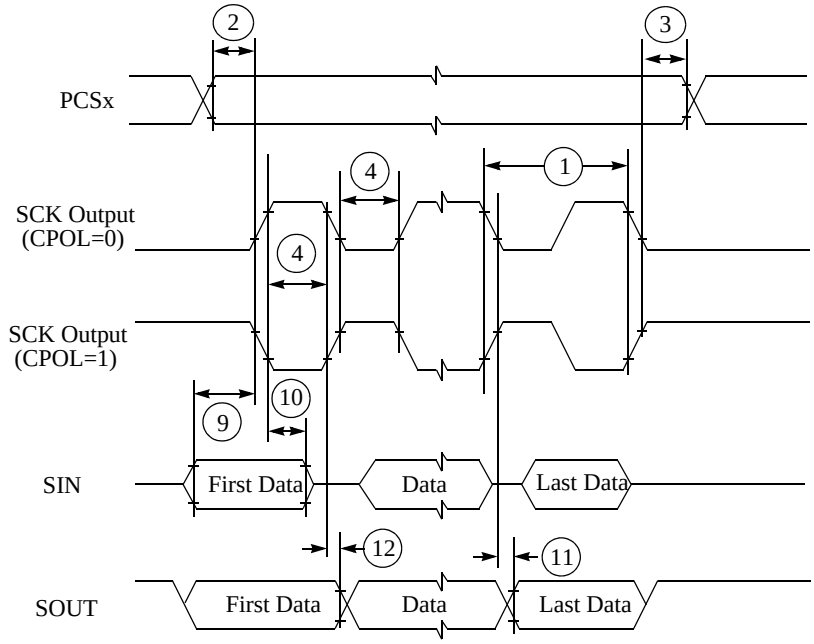
1. V_{DD} = 3.3 V ± 10%, T_J = –40 to +150 °C, unless otherwise specified.

Table 41. DSPI timing (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
12	t_{HO}	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
				Slave	6	—	
				Master (MTFE = 1, CPHA = 0)	6	—	
				Master (MTFE = 1, CPHA = 1)	–2	—	

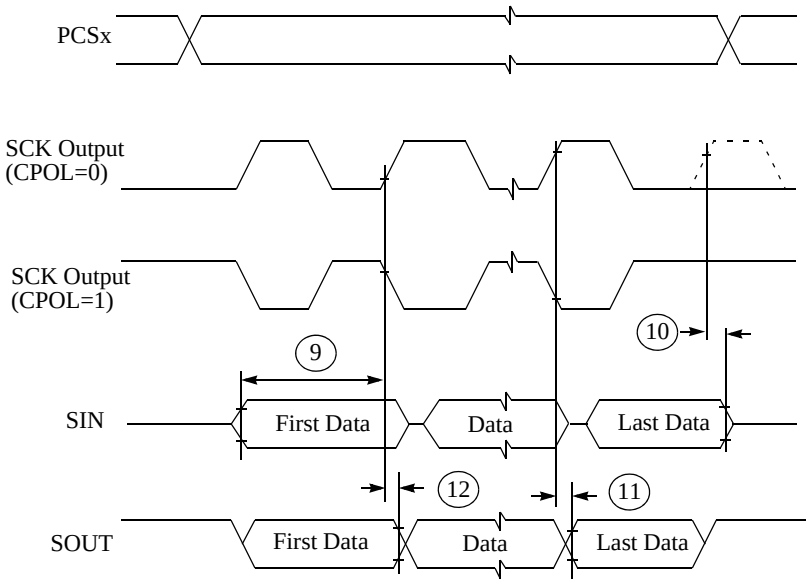
1. Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.

Figure 32. DSPI classic SPI timing — master, CPHA = 0



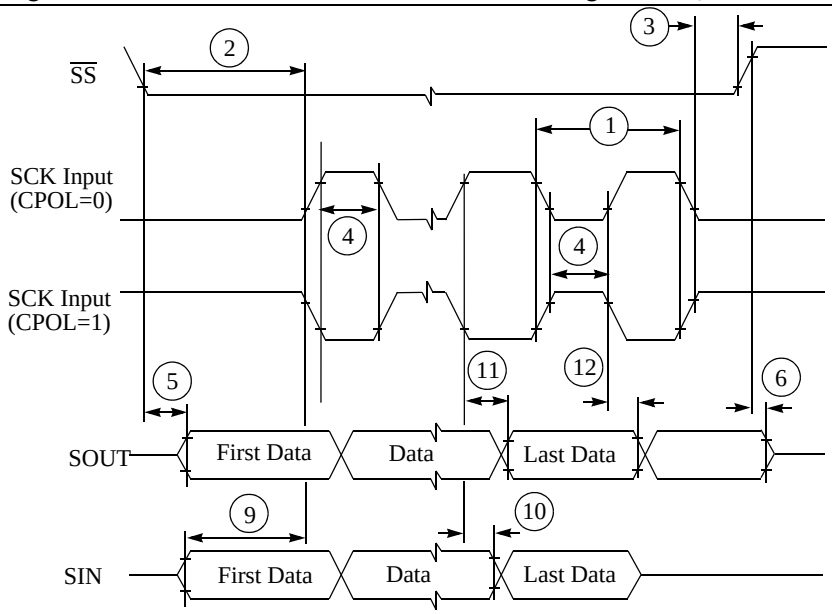
Note: The numbers shown are referenced in *Table 41*.

Figure 37. DSPI modified transfer format timing — master, CPHA = 1



Note: The numbers shown are referenced in *Table 41*.

Figure 38. DSPI modified transfer format timing – slave, CPHA = 0



Note: The numbers shown are referenced in *Table 41*.

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

Figure 41. LQFP100 package mechanical drawing