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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564l54l3bcfqy

1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

This document provides electrical specifications, pin assignments, and package diagrams for the SPC56ELx/SPC564Lx series of microcontroller units (MCUs). For functional characteristics, see the *SPC56ELx/SPC564Lx Microcontroller Reference Manual*. For use of the SPC56ELx/SPC564Lx in a fail-safe system according to safety standard ISO26262, see the *Safety Application Guide for SPCEL60.*

1.2 Description

The SPC56ELx/SPC564Lx series microcontrollers are system-on-chip devices that are built on Power Architecture technology and contain enhancements that improve the architecture's fit in embedded applications, include additional instruction support for digital signal processing (DSP) and integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system.

The SPC56ELx/SPC564Lx family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address electrical hydraulic power steering (EHPS), electric power steering (EPS) and airbag applications. The advanced and cost-efficient host processor core of the SPC56ELx/SPC564Lx automotive controller family complies with the Power Architecture embedded category. It operates at speeds as high as 120 MHz and offers high-performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users' implementations.

1.5.11 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.12 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

1.5.14 Frequency-Modulated Phase-Locked Loop (FMPLL)

Each device has two FMPLLs.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio are all software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 kHz nominal rate
- Option to switch modulation on and off via software interface
- Output divider (ODF) for reduced frequency operation without re-lock
- 3 modes of operation
  - Bypass mode
  - Normal FMPLL mode with crystal reference (default)
  - Normal FMPLL mode with external reference
- Lock monitor circuitry with lock status
- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers and jitter-free control
  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows to run motor control periphery at different (precisely lower, equal or higher as required) frequency than the system to ensure higher resolution

1.5.15 Main oscillator

The main oscillator provides these features:

- Input frequency range 4–40 MHz
- Crystal input mode
- External reference clock (3.3 V) input mode
- FMPLL reference

1.5.16 Internal Reference Clock (RC) oscillator

The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared to the stable bandgap reference voltage. The RC oscillator is the device safe clock.

- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high- and low-limit registers
- DMA support

1.5.31 eTimer module

The SPC56ELx provides three eTimer modules (on the LQFP package eTimer_2 is available internally only without any external I/O access). Six 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Maximum clock frequency of 120 MHz
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (Quad decoder mode)
- Maximum count rate
  - Equals peripheral clock divided by 2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use
- DMA support

1.5.32 Sine Wave Generator (SWG)

A digital-to-analog converter is available to generate a sine wave based on 32 stored values for external devices (ex: resolver).

Figure 4. SPC56ELx/SPC564Lx LFBGA257 pinout (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	H[2]	H[0]	G[14]	D[3]	C[15]	$V_{DD\_HV\_IO}$	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
B	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	$V_{SS\_HV\_IO}$	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
C	$V_{DD\_HV\_IO}$	NC(1)	$V_{SS\_HV\_IO}$	FCCU_F[1]	D[2]	A[13]	$V_{DD\_HV\_REG\_2}$	$V_{DD\_HV\_REG\_2}$	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	$V_{SS\_HV\_IO}$	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$	F[0]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	A[11]	E[13]	F[15]	$V_{DD\_HV\_IO}$	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]		$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$	$V_{DD\_LV\_COR}$		NC	C[13]	I[2]	G[4]
G	H[3]	$V_{DD\_HV\_IO}$	C[5]	A[6]		$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_LV\_COR}$		D[12]	H[13]	H[9]	G[6]
H	G[13]	$V_{SS\_HV\_IO}$	C[4]	A[5]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{SS_LV}	$V_{DD\_HV\_REG\_1}$	$V_{DD\_HV\_FLA}$	H[6]
J	F[7]	G[15]	$V_{DD\_HV\_REG\_0}$	$V_{DD\_HV\_REG\_0}$		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		V_{DD_LV}	$V_{DD\_HV\_REG\_1}$	$V_{SS\_HV\_FLA}$	H[15]
K	F[9]	F[8]		C[7]		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC		V_{DD_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{SS_LV}	V_{DD_LV}		NC	TCK	H[4]	B[4]
M	$V_{DD\_HV\_OSC}$	$V_{DD\_HV\_IO}$	D[8]	NC		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		C[11]	B[5]	TMS	H[5]
N	XTAL	$V_{SS\_HV\_IO}$	D[5]	$V_{SS\_LV\_PLL}$										NC	C[12]	A[2]	G[5]
P	$V_{SS\_HV\_OSC}$	RESET	D[6]	$V_{DD\_LV\_PLL}$	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	B[8]	NC	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	B[14]	$V_{DD\_LV\_COR}$	$V_{SS\_LV\_COR}$	$V_{DD\_HV\_IO}$	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	$V_{SS\_HV\_IO}$	D[7]	B[7]	E[6]	$V_{DD\_HV\_ADR0}$	B[10]	$V_{DD\_HV\_ADR1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	$V_{SS\_HV\_IO}$	D[11]	G[9]
T	$V_{SS\_HV\_IO}$	$V_{DD\_HV\_IO}$	NC	C[1]	E[5]	E[7]	$V_{SS\_HV\_ADR0}$	B[11]	$V_{SS\_HV\_ADR1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	$V_{DD\_HV\_IO}$	$V_{SS\_HV\_IO}$
U	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$	NC	E[4]	C[2]	E[2]	B[9]	B[12]	$V_{DD\_HV\_ADV}$	$V_{SS\_HV\_ADV}$	E[11]	NC	NC	$V_{DD\_HV\_PMU}$	G[11]	$V_{SS\_HV\_IO}$	$V_{SS\_HV\_IO}$
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

1. NC = Not connected (the pin is physically not connected to anything on the device).

Table 3, *Table 4*, and *Table 5* provide the pin function summaries for the 100-pin, 144-pin, and 257-pin packages, respectively, listing all the signals multiplexed to each pin.

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
83	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
84	JCOMP	—	—	JCOMP
85	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
86	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
87	$V_{DD\_HV\_IO}$	—		
88	$V_{SS\_HV\_IO}$	—		
89	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
90	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
91	$V_{DD\_HV\_REG\_2}$	—		
92	$V_{DD\_LV\_COR}$	—		
93	$V_{SS\_LV\_COR}$	—		
94	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
A5	H[0]	SIUL	GPIO[112]	GPIO[112]
		NPC	MDO[7]	—
A6	G[14]	SIUL	GPIO[110]	GPIO[110]
		NPC	MDO[9]	—
A7	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
A8	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
A9	$V_{DD\_HV\_IO\_RING}$	—		
A10	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
A11	H[10]	SIUL	GPIO[122]	GPIO[122]
		FlexPWM_1	X[2]	X[2]
		eTimer_2	ETC[2]	ETC[2]
A12	H[14]	SIUL	GPIO[126]	GPIO[126]
		FlexPWM_1	A[3]	A[3]
		eTimer_2	ETC[4]	ETC[4]
A13	A[10]	SIUL	GPIO[10]	GPIO[10]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[0]	B[0]
		FlexPWM_0	X[2]	X[2]
		SIUL	—	EIRQ[9]
A14	B[2]	SIUL	GPIO[18]	GPIO[18]
		LINFlexD_0	TXD	—
		SSCM	DEBUG[2]	—
		SIUL	—	EIRQ[17]

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
C9	I[0]	SIUL	GPIO[128]	GPIO[128]
		eTimer_2	ETC[0]	ETC[0]
		DSPI_0	CS4	—
		FlexPWM_1	—	FAULT[0]
C10	JCOMP	—	—	JCOMP
C11	H[11]	SIUL	GPIO[123]	GPIO[123]
		FlexPWM_1	A[2]	A[2]
C12	I[1]	SIUL	GPIO[129]	GPIO[129]
		eTimer_2	ETC[1]	ETC[1]
		DSPI_0	CS5	—
		FlexPWM_1	—	FAULT[1]
C13	F[14]	SIUL	GPIO[94]	GPIO[94]
		LINFlexD_1	TXD	—
C14	B[1]	SIUL	GPIO[17]	GPIO[17]
		eTimer_1	ETC[3]	ETC[3]
		SSCM	DEBUG[1]	—
		FlexCAN_0	—	RXD
		FlexCAN_1	—	RXD
		SIUL	—	EIRQ[16]
C15	$V_{SS\_HV\_IO\_RING}$	—		
C16	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]
C17	F[12]	SIUL	GPIO[92]	GPIO[92]
		eTimer_1	ETC[3]	ETC[3]
		SIUL	—	EIRQ[30]
D1	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
D2	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
C[15]	PCR[47]	SIUL	GPIO[47]	ALT0	GPIO[47]	—	—	SYM	S	85	124	A8
		FlexRay	CA_TR_EN	ALT1	—	—						
		eTimer_1	ETC[0]	ALT2	ETC[0]	PSMI[9]; PADSEL=1						
		FlexPWM_0	A[1]	ALT3	A[1]	PSMI[21]; PADSEL=1						
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=1						
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=1						
Port D												
D[0]	PCR[48]	SIUL	GPIO[48]	ALT0	GPIO[48]	—	—	SYM	S	86	125	B8
		FlexRay	CA_TX	ALT1	—	—						
		eTimer_1	ETC[1]	ALT2	ETC[1]	PSMI[10]; PADSEL=1						
		FlexPWM_0	B[1]	ALT3	B[1]	PSMI[25]; PADSEL=1						
D[1]	PCR[49]	SIUL	GPIO[49]	ALT0	GPIO[49]	—	—	M	S	3	3	E3
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=2						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexRay	—	—	CA_RX	—						

Table 9. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Min	Max	Unit
$V_{SS\_HV\_ADR0}$ $V_{SS\_HV\_ADR1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD\_HV\_ADV}$	SR	3.3 V ADC supply voltage	—	–0.3	4.5 (4), (3)	V
$V_{SS\_HV\_ADV}$	SR	3.3 V ADC supply ground	—	–0.1	0.1	V
TV_{DD}	SR	Supply ramp rate	—	3.0×10^{-6} (3.0 V/sec)	0.5 V/µs	V/µs
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$) or $V_{ss\_HV\_ADRx}$	Valid only for ADC pins	–0.3	6.0 (4)	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3(4), (5)	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability or cause permanent damage to the device.
2. Any voltage between operating condition and absolute max rating can be sustained for maximum cumulative time of 10 hours.
3. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
4. Internal structures hold the input voltage less than the maximum voltage on all pads powered by VDDE supplies, if the maximum injection current specification is met and VDDE is within the operating voltage specifications.
5. V_{DD} has to be considered equal to $V_{DD\_HV\_ADRx}$ in case of ADC pins, whilst it is $V_{DD\_HV\_IOx}$ for any other pin.

3.3 Recommended operating conditions

Table 10. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Min(1)	Max	Unit
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.63	V
$V_{DD\_HV\_IOx}$	SR	3.3 V input/output supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FLA}$	SR	3.3 V flash supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_FLA}$	SR	Flash memory ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.63	V
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_ADR0}$(2), (3) $V_{DD\_HV\_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	4.5 to 5.5 or 3.0 to 3.63		V

Table 17. ESD ratings[1], [2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
3. Data based on characterization results, not tested in production.

3.8 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 18. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	SR	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.9 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator HPREG1 (internal ballast to support core current)
- High power regulator HPREG2 (external NPN to support core current)
- Low voltage detector (LVD_MAIN_1) for 3.3 V supply to IO (V_{DDIO})
- Low voltage detector (LVD_MAIN_2) for 3.3 V supply (V_{DDREG})
- Low voltage detector (LVD_MAIN_3) for 3.3 V flash supply ($V_{DDFLASH}$)
- Low voltage detector (LVD_DIG_MAIN) for 1.2 V digital core supply (HPV_{DD})
- Low voltage detector (LVD_DIG_BKUP) for the self-test of LVD_DIG_MAIN
- High voltage detector (HVD_DIG_MAIN) for 1.2 V digital CORE supply (HPV_{DD})
- High voltage detector (HVD_DIG_BKUP) for the self-test of HVD_DIG_MAIN.
- Power on Reset (POR)

HPREG1 uses an internal ballast to support the core current. HPREG2 is used only when external NPN transistor is present on board to supply core current. The SPC56XL60/54 always powers up using HPREG1 if an external NPN transistor is present. Then the

Table 21. DC electrical characteristics(1) (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = -1.5 mA	$V_{DD\_HV\_IOx}$ - 0.8	—	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = -2 mA	$V_{DD\_HV\_IOx}$ - 0.8	—	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 11 mA	—	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = -11 mA	$V_{DD\_HV\_IOx}$ - 0.8	—	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = -1.5 mA	$V_{DD\_HV\_IOx}$ - 0.8	—	—	V
I_{INJ}	T	DC injection current per pin (all bi-directional ports)	—	–1	—	1	mA
I_{PU}	P	Equivalent pull-up current	$V_{IN} = V_{IL}$	–130	—	—	µA
			$V_{IN} = V_{IH}$	—	—	–10	
I_{PD}	P	Equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	—	µA
			$V_{IN} = V_{IH}$	—	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_J = -40 to +150 °C	-1	—	1	µA
		Input leakage current (all ADC input-only ports)(4)		-0.25	—	0.25	
		Input leakage current (shared ADC input-only ports)		-0.3	—	0.3	
V_{ILR}	P	$\overline{\text{RESET}}$, low level input voltage	—	–0.1(2)	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IHR}	P	$\overline{\text{RESET}}$, high level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	$V_{DD\_HV\_IOx}$+0.1(2)	V
V_{HYSR}	D	$\overline{\text{RESET}}$, Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	—	V
V_{OLR}	D	$\overline{\text{RESET}}$, low level output voltage	I_{OL} = 2 mA	—	—	0.5	V
I_{PD}	D	$\overline{\text{RESET}}$, equivalent pull-down current	$V_{IN} = V_{IL}$	10	—	—	µA
			$V_{IN} = V_{IH}$	—	—	130	

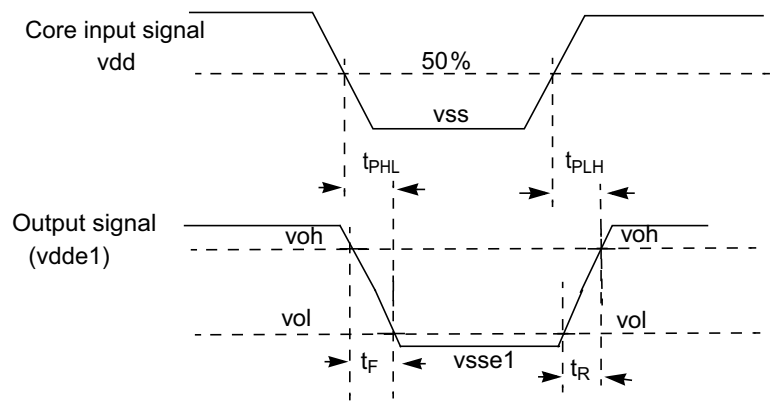
1. These specifications are design targets and subject to change per device characterization.

Table 32. Pad AC specifications (3.3 V, IPP_HVE = 0)(1) (continued)

No.	Pad		Tswitchon(1)(ns)			Rise/Fall(2) (ns)			Frequency (MHz)			Current slew(3) (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
3	Fast	T	1	—	6	—	—	4	—	—	72	3	—	40	25
			1	—	6	—	—	7	—	—	55	7	—	40	50
			1	—	6	—	—	12	—	—	40	7	—	40	100
			1	—	6	—	—	18	—	—	25	7	—	40	200
4	Symmetric	T	1	—	8	—	—	5	—	—	50	3	—	25	25

1. Propagation delay from $V_{DD\_HV\_IOx}/2$ of internal signal to Pchannel/Nchannel switch-on condition (i.e. t_PHL and t_PLH in *Figure 13: Pad output delay*).
2. Slope at rising/falling edge (i.e. t_F and t_R in *Figure 13: Pad output delay*).
3. Data based on characterization results, not tested in production.

Figure 13. Pad output delay



[1] t_F and t_R are transient times at the FAR END.
[2] t_{PHL} and t_{PLH} are measured at the pad.
[3] Core input slew = 1ns (0 to vdd).

3.20 Reset sequence

This section shows the duration for different reset sequences. It describes the different reset sequences and it specifies the start conditions and the end indication for the reset sequences.

3.20.1 Reset sequence duration

Table 33 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in *Section 3.20.2*.

Figure 22. Start-up reset requirements

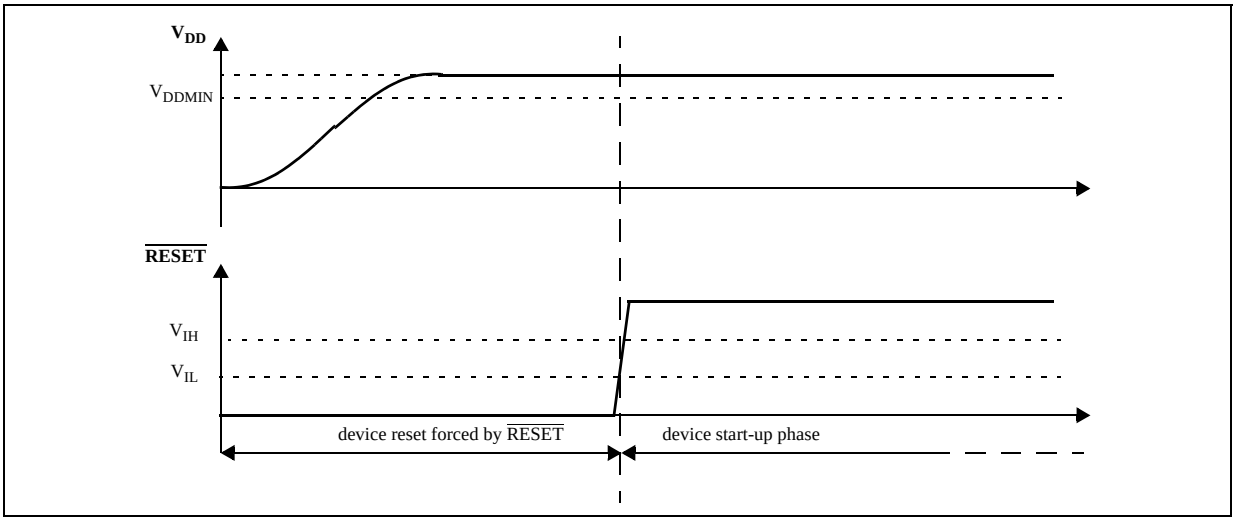


Figure 23. Noise filtering on reset signal

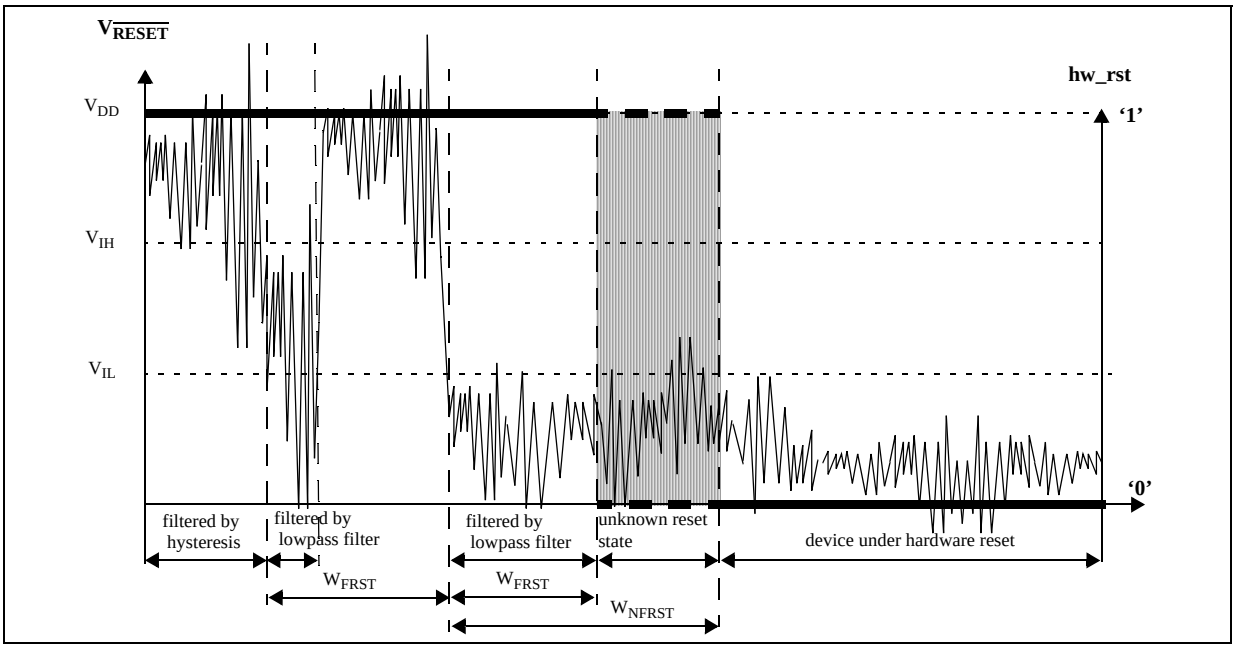
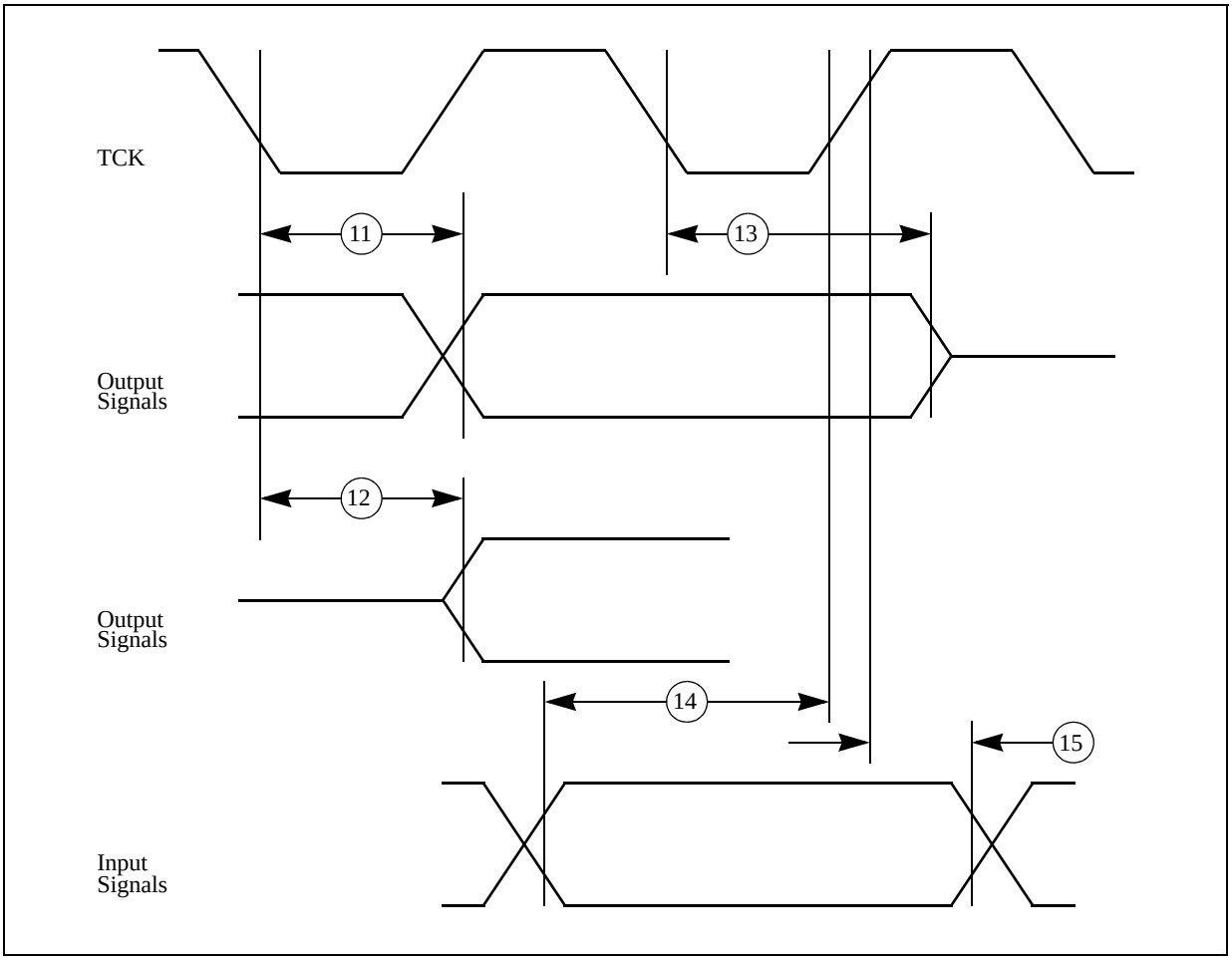


Table 36. RESET electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	nRESET input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	nRESET input not filtered pulse	—	500	—	—	ns

1. V_{DD} = 3.3 V ± 10%, T_J = –40 to +150 °C, unless otherwise specified.

Figure 26. JTAG boundary scan timing

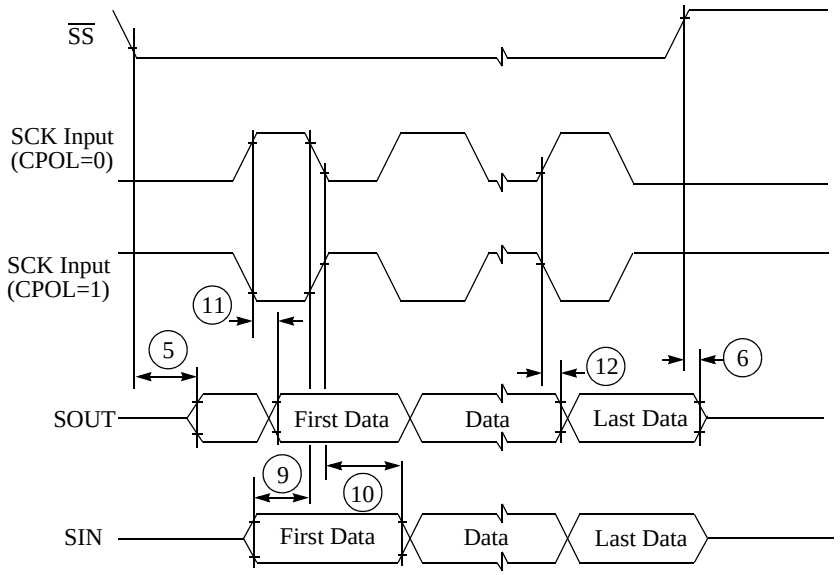


3.21.4 Nexus timing

Table 39. Nexus debug port timing(1)

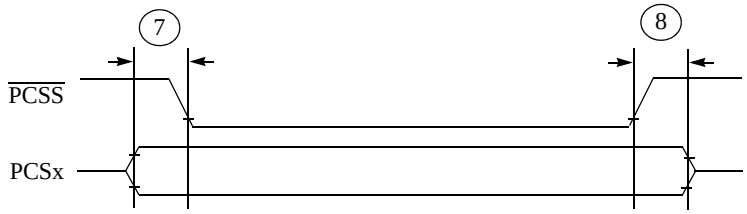
No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	D	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	D	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	D	MCKO Low to MDO, $\overline{MSEO}$, $\overline{EVTO}$ Data Valid(2)	—	–0.1	0.25	t_{MCYC}
4	t_{EVTIPW}	D	$\overline{EVTI}$ Pulse Width	—	4.0	—	t_{TCYC}
5	t_{EVTOPW}	D	$\overline{EVTO}$ Pulse Width	—	1		t_{MCYC}
6	t_{TCYC}	D	TCK Cycle Time(3)	—	62.5	—	ns
7	t_{TDC}	D	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	D	TDI, TMS Data Setup Time	—	8	—	ns

Figure 39. DSPI modified transfer format timing — slave, CPHA = 1



Note: The numbers shown are referenced in *Table 41*.

Figure 40. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing



Note: The numbers shown are referenced in *Table 41*.

4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

Figure 41. LQFP100 package mechanical drawing

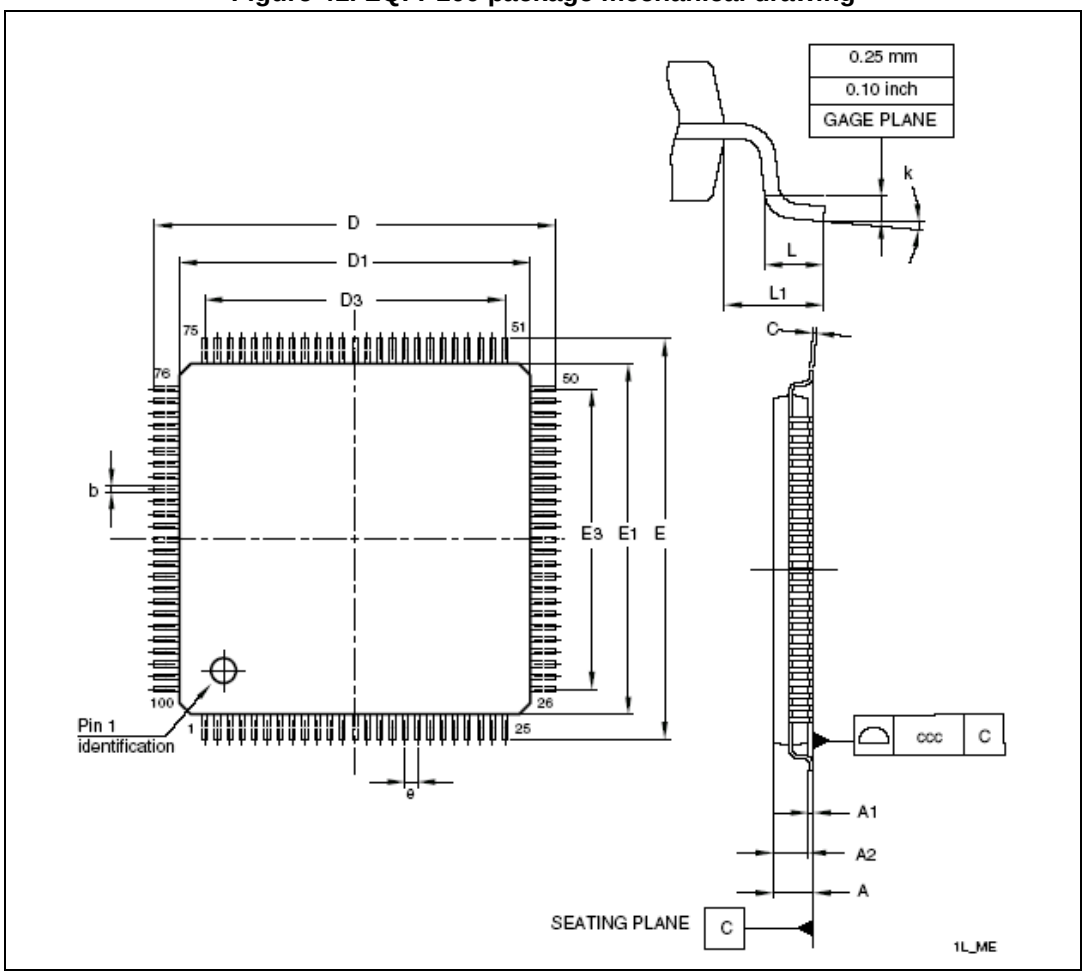


Table 42. LQFP100 mechanical data

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0 °	3.5 °	7.0 °	0.0 °	3.5 °	7.0 °
Tolerance	mm			inches		
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

5 Ordering information

Figure 44. Commercial product code structure