Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4d
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.63V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564l54l3bcoqr

  - FlexRay module (V2.1 Rev. A) with 2 channels, 64 message buffers and data rates up to 10 Mbit/s
- Two 12-bit analog-to-digital converters (ADCs)
  - 16 input channels
  - Programmable cross triggering unit (CTU) to synchronize ADCs conversion with timer and PWM
- Sine wave generator (D/A with low pass filter)
- On-chip CAN/UART bootstrap loader
- Single 3.0 V to 3.6 V voltage supply
- Ambient temperature range –40 °C to 125 °C
- Junction temperature range –40 °C to 150 °C

- Extensive system development and tracing support via Nexus debug port

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port, although one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions.

The crossbar provides the following features:

- 4 masters and 3 slaves supported per each replicated crossbar
  - Masters allocation for each crossbar: e200z4d core with two independent bus interface units (BIU) for I and D access (2 masters), one eDMA, one FlexRay
  - Slaves allocation for each crossbar: a redundant flash-memory controller with 2 slave ports to guarantee maximum flexibility to handle Instruction and Data array, one redundant SRAM controller with 1 slave port each and 1 redundant peripheral bus bridge
- 32-bit address bus and 64-bit data bus
- Programmable arbitration priority
  - Requesting masters can be treated with equal priority and are granted access to a slave port in round-robin method, based upon the ID of the last master to be granted access or a priority order can be assigned by software at application run time
- Temporary dynamic priority elevation of masters

The XBAR is replicated for each processing channel.

1.5.3 Memory Protection Unit (MPU)

The Memory Protection Unit splits the physical memory into 16 different regions. Each master (eDMA, FlexRay, CPU) can be assigned different access rights to each region.

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

The memory protection unit is replicated for each processing channel.

1.5.4 Enhanced Direct Memory Access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is used to minimize the overall block size.

1.5.11 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.12 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

Table 3. LQFP100 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
48	$V_{DD\_LV\_COR}$	—		
49	$V_{SS\_LV\_COR}$	—		
50	$V_{DD\_HV\_PMU}$	—		
51	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]
52	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
53	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
54	D[11]	SIUL	GPIO[59]	GPIO[59]
		FlexPWM_0	B[0]	B[0]
		eTimer_0	—	ETC[1]
55	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—
56	C[12]	SIUL	GPIO[44]	GPIO[44]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
57	A[2]	SIUL	GPIO[2]	GPIO[2]
		eTimer_0	ETC[2]	ETC[2]
		FlexPWM_0	A[3]	A[3]
		DSPI_2	—	SIN
		MC_RGM	—	ABS[0]
		SIUL	—	EIRQ[2]
58	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
59	TMS	—		
60	TCK	—		
61	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
15	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
16	$V_{DD\_HV\_REG\_0}$	—		
17	$V_{SS\_LV\_COR}$	—		
18	$V_{DD\_LV\_COR}$	—		
19	F[7]	SIUL	GPIO[87]	GPIO[87]
		NPC	MCKO	—
20	F[8]	SIUL	GPIO[88]	GPIO[88]
		NPC	MSEO[1]	—
21	$V_{DD\_HV\_IO}$	—		
22	$V_{SS\_HV\_IO}$	—		
23	F[9]	SIUL	GPIO[89]	GPIO[89]
		NPC	MSEO[0]	—
24	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	EVTO	—
25	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	—	EVTI
26	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
27	$V_{DD\_HV\_OSC}$	—		
28	$V_{SS\_HV\_OSC}$	—		
29	XTAL	—		
30	EXTAL	—		
31	RESET	—		
32	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]
33	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]

Table 4. LQFP144 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
34	D[6]	SIUL	GPIO[54]	GPIO[54]
		DSPI_0	CS2	—
		FlexPWM_0	X[3]	X[3]
		FlexPWM_0	—	FAULT[1]
35	$V_{SS\_LV\_PLL0\_PLL1}$	—		
36	$V_{DD\_LV\_PLL0\_PLL1}$	—		
37	D[7]	SIUL	GPIO[55]	GPIO[55]
		DSPI_1	CS3	—
		DSPI_0	CS4	—
		SWG	analog output	—
38	FCCU_F[0]	FCCU	F[0]	F[0]
39	$V_{DD\_LV\_COR}$	—		
40	$V_{SS\_LV\_COR}$	—		
41	C[1]	SIUL	—	GPIO[33]
		ADC_0	—	AN[2]
42	E[4]	SIUL	—	GPIO[68]
		ADC_0	—	AN[7]
43	B[7]	SIUL	—	GPIO[23]
		LINFlexD_0	—	RXD
		ADC_0	—	AN[0]
44	E[5]	SIUL	—	GPIO[69]
		ADC_0	—	AN[8]
45	C[2]	SIUL	—	GPIO[34]
		ADC_0	—	AN[3]
46	E[6]	SIUL	—	GPIO[70]
		ADC_0	—	AN[4]
47	B[8]	SIUL	—	GPIO[24]
		eTimer_0	—	ETC[5]
		ADC_0	—	AN[1]
48	E[7]	SIUL	—	GPIO[71]
		ADC_0	—	AN[6]
49	E[2]	SIUL	—	GPIO[66]
		ADC_0	—	AN[5]
50	$V_{DD\_HV\_ADR0}$	—		
51	$V_{SS\_HV\_ADR0}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
A5	H[0]	SIUL	GPIO[112]	GPIO[112]
		NPC	MDO[7]	—
A6	G[14]	SIUL	GPIO[110]	GPIO[110]
		NPC	MDO[9]	—
A7	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
A8	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
A9	$V_{DD\_HV\_IO\_RING}$	—		
A10	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
A11	H[10]	SIUL	GPIO[122]	GPIO[122]
		FlexPWM_1	X[2]	X[2]
		eTimer_2	ETC[2]	ETC[2]
A12	H[14]	SIUL	GPIO[126]	GPIO[126]
		FlexPWM_1	A[3]	A[3]
		eTimer_2	ETC[4]	ETC[4]
A13	A[10]	SIUL	GPIO[10]	GPIO[10]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[0]	B[0]
		FlexPWM_0	X[2]	X[2]
		SIUL	—	EIRQ[9]
A14	B[2]	SIUL	GPIO[18]	GPIO[18]
		LINFlexD_0	TXD	—
		SSCM	DEBUG[2]	—
		SIUL	—	EIRQ[17]

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
B11	E[15]	SIUL	GPIO[79]	GPIO[79]
		DSPI_0	CS1	—
		SIUL	—	EIRQ[27]
B12	E[14]	SIUL	GPIO[78]	GPIO[78]
		eTimer_1	ETC[5]	ETC[5]
		SIUL	—	EIRQ[26]
B13	B[3]	SIUL	GPIO[19]	GPIO[19]
		SSCM	DEBUG[3]	—
		LINFlexD_0	—	RXD
B14	F[13]	SIUL	GPIO[93]	GPIO[93]
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[31]
B15	B[0]	SIUL	GPIO[16]	GPIO[16]
		FlexCAN_0	TXD	—
		eTimer_1	ETC[2]	ETC[2]
		SSCM	DEBUG[0]	—
		SIUL	—	EIRQ[15]
B16	$V_{DD\_HV\_IO\_RING}$	—		
B17	$V_{SS\_HV\_IO\_RING}$	—		
C1	$V_{DD\_HV\_IO\_RING}$	—		
C2	Not connected	—		
C3	$V_{SS\_HV\_IO\_RING}$	—		
C4	FCCU_F[1]	FCCU	F[1]	F[1]
C5	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
C6	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
C7	$V_{DD\_HV\_REG\_2}$	—		
C8	$V_{DD\_HV\_REG\_2}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
G14	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
G15	H[13]	SIUL	GPIO[125]	GPIO[125]
		FlexPWM_1	X[3]	X[3]
		eTimer_2	ETC[3]	ETC[3]
G16	H[9]	SIUL	GPIO[121]	GPIO[121]
		FlexPWM_1	B[1]	B[1]
		DSPI_0	CS7	—
G17	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
H1	G[13]	SIUL	GPIO[109]	GPIO[109]
		NPC	MDO[10]	—
H2	$V_{SS\_HV\_IO\_RING}$	—		
H3	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
H4	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
H6	V_{DD_LV}	—		
H7	V_{SS_LV}	—		
H8	V_{SS_LV}	—		
H9	V_{SS_LV}	—		
H10	V_{SS_LV}	—		
H11	V_{SS_LV}	—		
H12	V_{DD_LV}	—		
H14	V_{SS_LV}	—		
H15	$V_{DD\_HV\_REG\_1}$	—		
H16	$V_{DD\_HV\_FLA}$	—		

Table 5. LFBGA257 pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
K9	V_{SS_LV}	—		
K10	V_{SS_LV}	—		
K11	V_{SS_LV}	—		
K12	V_{DD_LV}	—		
K14	Not connected	—		
K15	H[8]	SIUL	GPIO[120]	GPIO[120]
		FlexPWM_1	A[1]	A[1]
		DSPI_0	CS6	—
K16	H[7]	SIUL	GPIO[119]	GPIO[119]
		FlexPWM_1	X[1]	X[1]
		eTimer_2	ETC[1]	ETC[1]
K17	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
L1	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	EVTO	—
L2	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	—	EVTI
L3	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
L4	Not connected	—		
L6	V_{DD_LV}	—		
L7	V_{SS_LV}	—		
L8	V_{SS_LV}	—		
L9	V_{SS_LV}	—		
L10	V_{SS_LV}	—		
L11	V_{SS_LV}	—		
L12	V_{DD_LV}	—		
L14	Not connected	—		
L15	TCK	—		

Table 8. Pin muxing

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
Port A												
A[0]	PCR[0]	SIUL	GPIO[0]	ALT0	GPIO[0]	—	—	M	S	51	73	T14
		eTimer_0	ETC[0]	ALT1	ETC[0]	PSMI[35]; PADSEL=0						
		DSPI_2	SCK	ALT2	SCK	PSMI[1]; PADSEL=0						
		SIUL	—	—	EIRQ[0]	—						
A[1]	PCR[1]	SIUL	GPIO[1]	ALT0	GPIO[1]	—	—	M	S	52	74	R14
		eTimer_0	ETC[1]	ALT1	ETC[1]	PSMI[36]; PADSEL=0						
		DSPI_2	SOUT	ALT2	—	—						
		SIUL	—	—	EIRQ[1]	—						
A[2]	PCR[2]	SIUL	GPIO[2]	ALT0	GPIO[2]	—	Pull down	M	S	57	84	N16
		eTimer_0	ETC[2]	ALT1	ETC[2]	PSMI[37]; PADSEL=0						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=0						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=0						
		MC_RGM	—	—	ABS[0]	—						
		SIUL	—	—	EIRQ[2]	—						

Table 8. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed(1)		Pin #		
								SRC = 1	SRC = 0	100 pkg	144 pkg	257 pkg
H[11]	PCR[123]	SIUL	GPIO[123]	ALT0	GPIO[123]	—	—	M	S	—	—	C11
		FlexPWM_1	A[2]	ALT1	A[2]	—						
H[12]	PCR[124]	SIUL	GPIO[124]	ALT0	GPIO[124]	—	—	M	S	—	—	B10
		FlexPWM_1	B[2]	ALT1	B[2]	—						
H[13]	PCR[125]	SIUL	GPIO[125]	ALT0	GPIO[125]	—	—	M	S	—	—	G15
		FlexPWM_1	X[3]	ALT1	X[3]	—						
		eTimer_2	ETC[3]	ALT2	ETC[3]	PSMI[42]; PADSEL=0						
H[14]	PCR[126]	SIUL	GPIO[126]	ALT0	GPIO[126]	—	—	M	S	—	—	A12
		FlexPWM_1	A[3]	ALT1	A[3]	—						
		eTimer_2	ETC[4]	ALT2	ETC[4]	—						
H[15]	PCR[127]	SIUL	GPIO[127]	ALT0	GPIO[127]	—	—	M	S	—	—	J17
		FlexPWM_1	B[3]	ALT1	B[3]	—						
		eTimer_2	ETC[5]	ALT2	ETC[5]	—						
Port I												
I[0]	PCR[128]	SIUL	GPIO[128]	ALT0	GPIO[128]	—	—	M	S	—	—	C9
		eTimer_2	ETC[0]	ALT1	ETC[0]	PSMI[39]; PADSEL=1						
		DSPI_0	CS4	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[0]	—						

Table 22. Current consumption characteristics (continued)

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$[2]	T	Operating current	1.2V supplies Tj=105°C $V_{DD\_LV\_COR}$ = 1.2V LSM mode	—	—	275	mA
			1.2V supplies Tj=125°C $V_{DD\_LV\_COR}$ = 1.2V LSM mode	—	—	299	mA
$I_{DD\_LV\_TYP}$ + $I_{DD\_LV\_PLL}$[2]	T	Operating current	1.2V supplies Tj=105°C $V_{DD\_LV\_COR}$ = 1.2V DPM Mode	—	—	189	mA
			1.2V supplies Tj=125°C $V_{DD\_LV\_COR}$ = 1.2V DPM Mode	—	—	214	mA
			1.2V supplies Tj=150°C $V_{DD\_LV\_COR}$ = 1.2V DPM Mode	—	—	235	mA
$I_{DD\_LV\_STOP}$	T	Operating current in V_{DD} STOP mode	T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	20	mA
	T		T_J = 55 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	57	
	P		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	105	
$I_{DD\_LV\_HALT}$	T	Operating current in V_{DD} HALT mode	T_J = 25 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	25	mA
	T		T_J = 55 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	64	
	P		T_J = 150 °C $V_{DD\_LV\_COR}$ = 1.32 V	—	—	115	
$I_{DD\_HV\_ADC}$[3], [4]	T	Operating current	T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD\_HV\_ADC}$ = 3.6 V	—	—	10	mA

3.14 FMPLL electrical characteristics

Table 25. FMPLL electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$f_{REF\_CRYSTAL}$ f_{REF_EXT}	D	FMPLL reference frequency range(1)	Crystal reference	4	—	40	MHz
f_{PLL_IN}	D	Phase detector input frequency range (after pre-divider)	—	4	—	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	4	—	120(2)	MHz
f_{FREE}	P	Free running frequency	Measured using clock division (typically ÷16)	20	—	150	MHz
f_{sys}	D	On-chip FMPLL frequency(2)	—	16	—	120	MHz
t_{CYC}	D	System clock period	—	—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window(3)	Lower limit	1.6	—	3.7	MHz
			Upper limit	24	—	56	
f_{SCM}	D	Self-clocked mode frequency(4),(5)	—	20	—	150	MHz
t_{LOCK}	P	Lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}	—	—	200	µs
t_{lpll}	D	FMPLL lock time (6),(7)	—	—	—	200	µs
t_{dc}	D	Duty cycle of reference	—	40	—	60	%
C_{JITTER}	T	CLKOUT period jitter(8),(9),(10),(11)	Long-term jitter (avg. over 2 ms interval), $f_{FMPLLOUT}$ maximum	–6	—	6	ns
Δt_{PKJIT}	T	Single period jitter (peak to peak)	PHI @ 120 MHz, Input clock @ 4 MHz	—	—	175	ps
			PHI @ 100 MHz, Input clock @ 4 MHz	—	—	185	ps
			PHI @ 80 MHz, Input clock @ 4 MHz	—	—	200	ps
Δt_{LTJIT}	T	Long term jitter	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±6	ns
f_{LCK}	D	Frequency LOCK range	—	–6	—	6	% $f_{FMPLLOUT}$
f_{UL}	D	Frequency un-LOCK range	—	–18	—	18	% $f_{FMPLLOUT}$
f_{CS} f_{DS}	D	Modulation depth	Center spread	±0.25	—	±2.0	% $f_{FMPLLOUT}$
			Down spread	–0.5	—	-8.0	
f_{MOD}	D	Modulation frequency(12)	—	—	—	100	kHz

1. Considering operation with FMPLL not bypassed.

2. Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for <100 program/erase cycles, nominal supply values and operation at 25°C. These values are verified at production test.
3. Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.
4. Program times are actual hardware programming times and do not include software overhead.

Table 29. Flash memory timing

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
T_{RES}	D	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low	—	—	100	ns
T_{DONE}	D	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared	—	—	5	ns
T_{PSRT}	D	Time between program suspend resume and the next program suspend request.(1)	100	—	—	µs
T_{ESRT}	D	Time between erase suspend resume and the next erase suspend request.(2)	10			ms

1. Repeated suspends at a high frequency may result in the operation timing out, and the flash module will respond by completing the operation with a fail code (MCR[PEG] = 0), or the operation not able to finish (MCR[DONE] = 1 during Program operation). The minimum time between suspends to ensure this does not occur is T_{PSRT}.
2. If Erase suspend rate is less than T_{ESRT}, an increase of slope voltage ramp occurs during erase pulse. This improves erase time but reduces cycling figure due to overstress.

Table 30. Flash memory module life

No.	Symbol		Parameter	Value			Unit
				Minimum	Typical	Maximum	
1	P/E	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range(1)	100000	—	—	cycles
2	P/E	C	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range(1)	1000	100000 (2)	—	cycles
3	Retention	C	Minimum data retention at 85 °C average ambient temperature(3) Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	 20 10 5	 — — —	 — — —	years

1. Operating temperature range is T_J from –40 °C to 150 °C. Typical endurance is evaluated at 25 °C.
2. Typical P/E cycles is 100,000 cycles for 128 KB and 256 KB blocks.
3. Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

Table 34. Reset sequence trigger — reset sequence (continued)

Reset Sequence Trigger	Reset Sequence Start Condition	Reset Sequence End Indication	Reset Sequence				
			Destructive Reset Sequence, BIST enabled(1)	***Destructive Reset Sequence, BIST disabled***(1)	***External Reset Sequence Long, BIST enabled***	***Functional Reset Sequence Long***	***Functional Reset Sequence Short***
All internal functional reset sources configured for long reset	Sequence starts with internal reset trigger	Release of $\overline{\text{RESET}}$(7)	cannot trigger		cannot trigger	triggers	cannot trigger
All internal functional reset sources configured for short reset			cannot trigger		cannot trigger	cannot trigger	triggers

1. Whether BIST is executed or not depends on the chip configuration data stored in the shadow sector of the NVM.
2. End of the internal reset sequence (as specified in *Table 33*) can only be observed by release of $\overline{\text{RESET}}$ if it is not held low externally beyond the end of the internal sequence which would prolong the internal reset PHASE3 till $\overline{\text{RESET}}$ is released externally.
3. The assertion of $\overline{\text{RESET}}$ can only trigger a reset sequence if the device was running ($\overline{\text{RESET}}$ released) before. $\overline{\text{RESET}}$ does not gate a *Destructive Reset Sequence, BIST enabled* or a *Destructive Reset Sequence, BIST disabled*. However, it can prolong these sequences if $\overline{\text{RESET}}$ is held low externally beyond the end of the internal sequence (beyond PHASE3).
4. If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is enabled via chip configuration data stored in the shadow sector of the NVM.
5. If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is disabled via chip configuration data stored in the shadow sector of the NVM.
6. If $\overline{\text{RESET}}$ is configured for short reset
7. Internal reset sequence can only be observed by state of $\overline{\text{RESET}}$ if bidirectional $\overline{\text{RESET}}$ functionality is enabled for the functional reset source which triggered the reset sequence.

3.20.4 Reset sequence — start condition

The impact of the voltage thresholds on the starting point of the internal reset sequence becomes important if the voltage rails / signals ramp up with a very slow slew rate compared to the overall reset sequence duration.

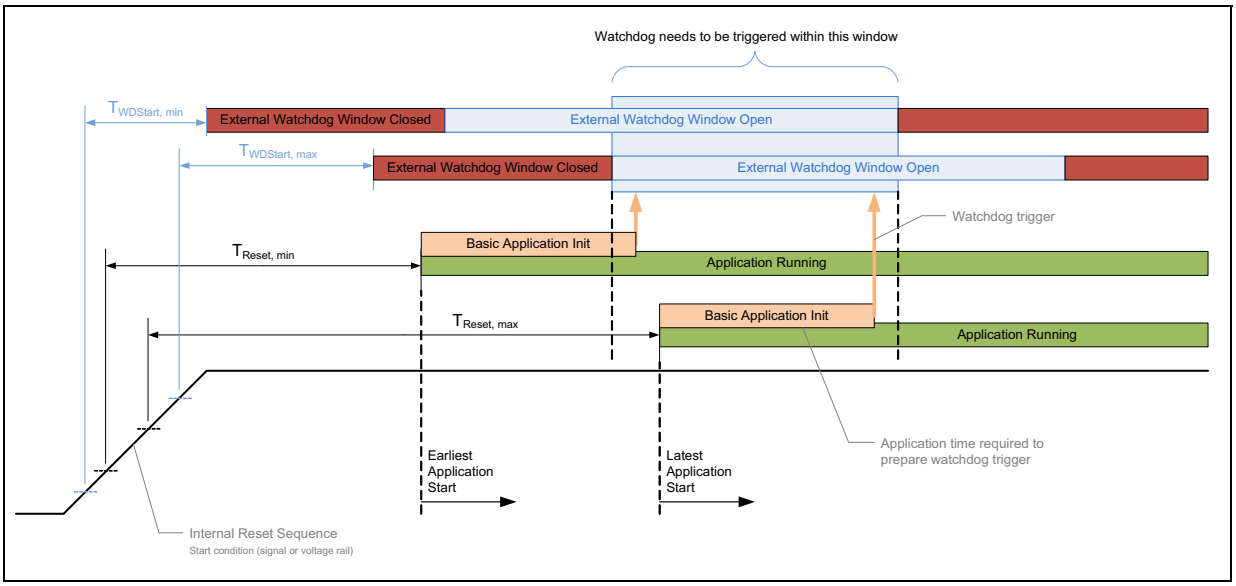
3.20.4.1 Destructive reset

Figure 19 shows the voltage threshold that determines the start of the *Destructive Reset Sequence, BIST enabled* and the start for the *Destructive Reset Sequence, BIST disabled*.

3.20.5 External watchdog window

If the application design requires the use of an external watchdog the data provided in *Section 3.20* can be used to determine the correct positioning of the trigger window for the external watchdog. *Figure 21* shows the relationships between the minimum and the maximum duration of a given reset sequence and the position of an external watchdog trigger window.

Figure 21. Reset sequence - External watchdog trigger window position



3.21 AC timing characteristics

AC Test Timing Conditions: Unless otherwise noted, all test conditions are as follows:

- TJ = –40 to 150 °C
- Supply voltages as specified in *Table 10*
- Input conditions: All Inputs: tr, tf = 1 ns
- Output Loading: All Outputs: 50 pF

3.21.1 $\overline{\text{RESET}}$ pin characteristics

The SPC56ELx/SPC564Lx implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 42. LQFP144 package mechanical drawing

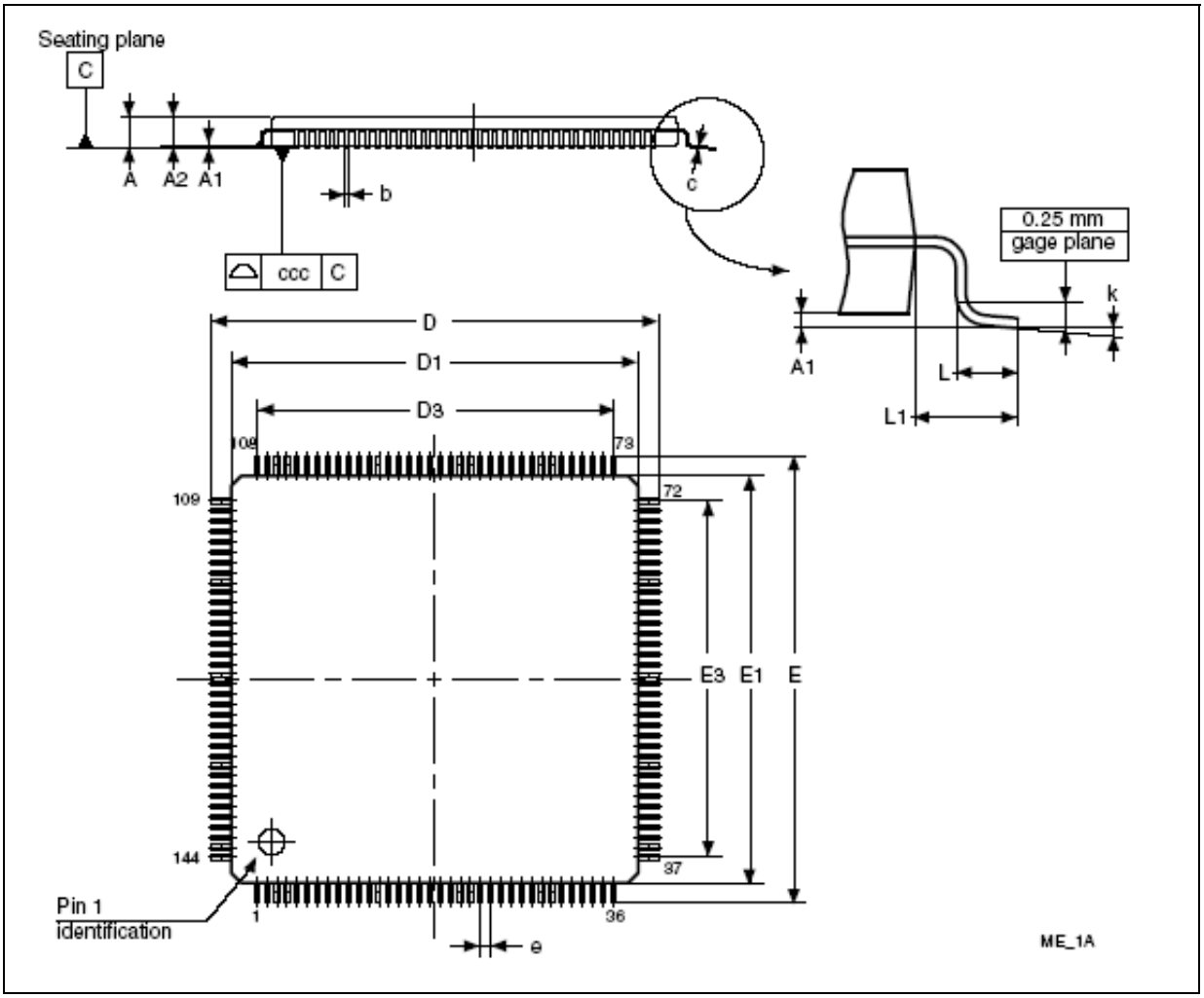


Table 43. LQFP144 mechanical data

Symbol	mm			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.6			0.0630
A1		0.05	0.15		0.0020	0.0059
A2	1.4	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.2		0.0035	0.0079
D	22	21.8	22.2	0.8661	0.8583	0.8740
D1	20	19.8	20.2	0.7874	0.7795	0.7953
D3	17.5			0.6890		
E	22	21.8	22.2	0.8661	0.8583	0.8740
E1	20	19.8	20.2	0.7874	0.7795	0.7953

Table 45. Document revision history

Date	Revision	Changes
01-Aug-2012	8 (cont.)	– In *Table 20: Voltage regulator electrical specifications*, changed the “Digital supply high voltage detector upper threshold low limit (After a destructive reset initialization phase completion)” from 1.43V to 1.38V. – Added *Table 20: Voltage regulator electrical specifications*. – Updated the IDD values in *Table 22: Current consumption characteristics*. Changed conditions text from “1.2 supplies during LBIST (full LBIST configuration)” to “1.2 V supplies” for all the IDD parameters except $I_{DD\_LV\_BIST}$+$I_{DD\_LV\_PLL}$. Added footnote in “Conditions” for the DPM mode. – Removed Cut references from the whole document. In *Table 27: ADC conversion characteristics*, changed the sampling frequency value from ‘1 MHz’ to ‘983.6 KHz’.
31-Jul-2013	9	– Updated *Table 20: Voltage regulator electrical specifications* (Voltage regulator electrical specifications) – Added Digital supply low voltage detector lower threshold and Digital supply low voltage detector upper threshold – Updated Main High Voltage Power-Low Voltage Detection value to 2.93 V – Replaced IEC with ISO26262 in *Section 1.1: Document overview*, – *Table 1* (SPC56XL60/54 device summary)-removed KGD – *Table 26* (16 MHz RC oscillator electrical characteristics) modified fRC values – Updated*Table 28* (Flash memory program and erase electrical specifications) – Updated *Table 27* (ADC conversion characteristics)-tconv to teval and associated footnote – Updated *Table 21* (DC electrical characteristics) – added VIH footnote – Updated IOL, IOH value for Fast pads – Updated *Table 33* (RESET sequences)-TDRB and TELRB – Updated *Table 20* (Voltage regulator electrical specifications)-combined ESR of external capacitor values – Updated *Section 3.16.1: Input Impedance and ADC Accuracy* -replaced fc by fs – *Table 7* (System pins)s-added footnote to RESET pin about weak pull down – Updated Injection current information in *Table 21* (DC electrical characteristics)-IINJ, *Table 9* (Absolute maximum ratings)-footnote 4 – Updated *Table 22* (Current consumption characteristics) for the following: – specified oscillator bypass mode and crystal oscillator mode – Updated STOP and HALT mode values – Added IDD_HV_PMU – footnote 2, footnote 3 – Added footnote $V_{DD\_HV\_ADRx}$ must always be applied and should be stable before LBIST starts. to *Table 10* (Recommended operating conditions (3.3 V)). – Added footnote to *Section 5: Ordering information* – Edit changes to *Section 3.6: Electromagnetic Interference (EMI) characteristics* – Updated *Equation 11*.